



STI23NM60ND

N-channel 600 V, 0.150 Ω typ., 19.5 A, FDmesh™ II Power MOSFET
(with fast diode) in a I²PAK package

Datasheet — production data

Features

Order code	V _{DSS} @ T _{Jmax}	R _{DS(on)} max	I _D
STI23NM60ND	650 V	< 0.180 Ω	19.5 A

- The worldwide best R_{DS(on)} * area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- High dv/dt and avalanche capabilities

Applications

- Switching applications

Description

These FDmesh™ II Power MOSFETs with intrinsic fast-recovery body diode are produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, these revolutionary devices feature extremely low on-resistance and superior switching performance. They are ideal for bridge topologies and ZVS phase-shift converters.

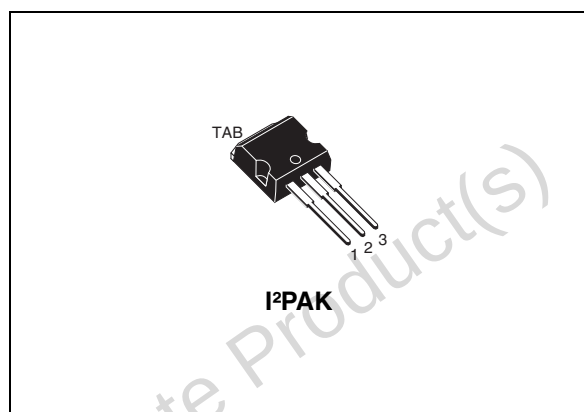


Figure 1. Internal schematic diagram

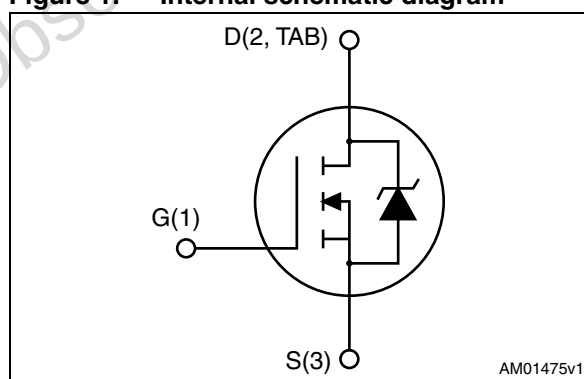


Table 1. Device summary

Order codes	Marking	Package	Packaging
STI23NM60ND	23NM60ND	TO-220FP	Tube

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Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	19.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	11.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	78	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	150	W
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	9	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	700	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 19.5\text{ A}$, $di/dt \leq 600\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS(peak)} < V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max ⁽¹⁾		$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$, $V_{GS} = 10\text{ V}$	30			V/ns
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$, $V_{DS} = 600\text{ V}$, $T_c = 125\text{ }^{\circ}\text{C}$			1 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.150	0.180	Ω

1. Characteristic value at turn off on inductive load

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2100 80 10	-	pF pF pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$, $V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 Test signal level=20 mV open drain	-	4	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480\text{ V}$, $I_D = 19.5\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 14)	-	69 13 35	-	nC nC nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	21	-	ns
t_r	Rise time			19		ns
$t_{d(off)}$	Turn-off delay time			92		ns
t_f	Fall time			42		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		19.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				78	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19.5\text{ A}$, $V_{GS}=0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 19.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 15)	-	190		ns
Q_{rr}	Reverse recovery charge			1.2		μC
I_{RRM}	Reverse recovery current			13		A
t_{rr}	Reverse recovery time	$V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $I_{SD} = 19.5\text{ A}$ $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15)	-	270		ns
Q_{rr}	Reverse recovery charge			2.0		μC
I_{RRM}	Reverse recovery current			15		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

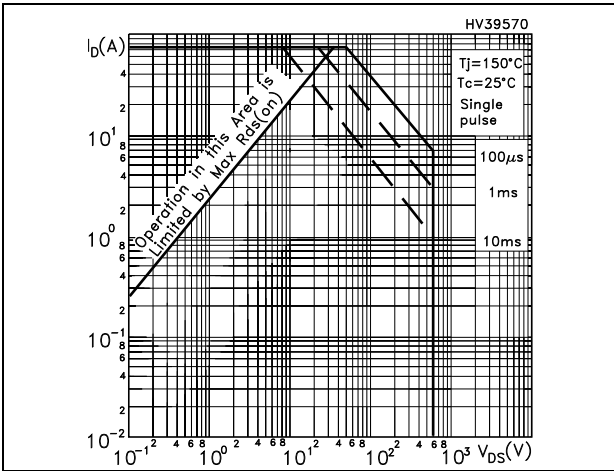


Figure 3. Thermal impedance

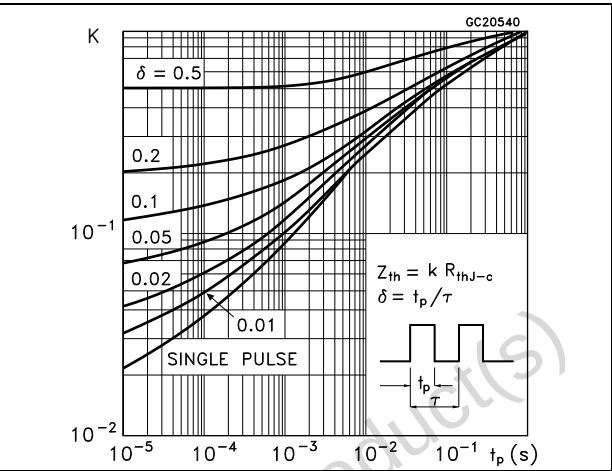


Figure 4. Output characteristics

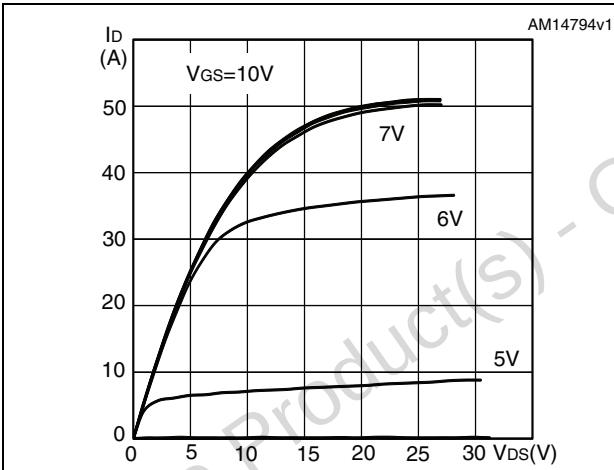


Figure 5. Transfer characteristics

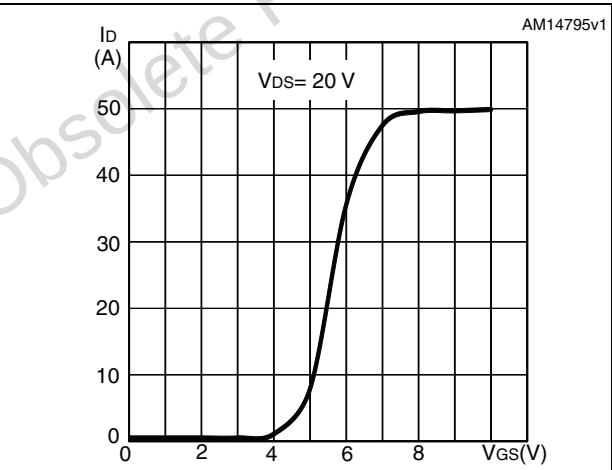


Figure 6. Static drain-source on resistance

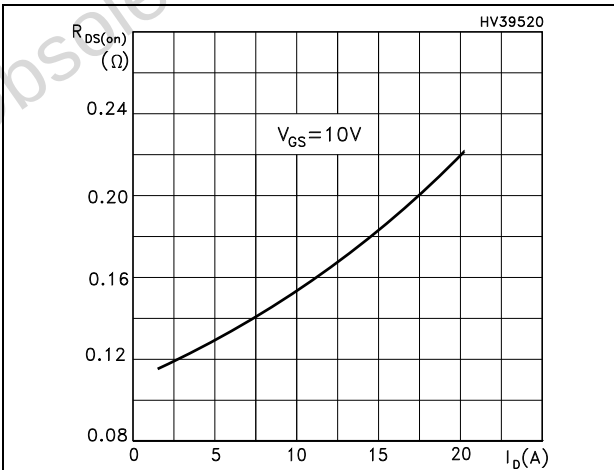


Figure 7. Gate charge vs gate-source voltage

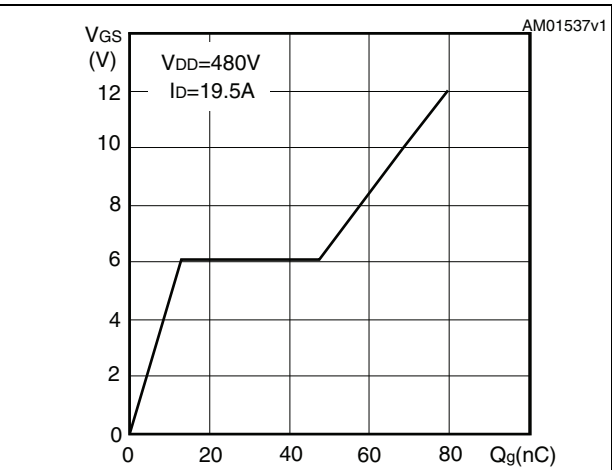


Figure 8. Capacitance variations

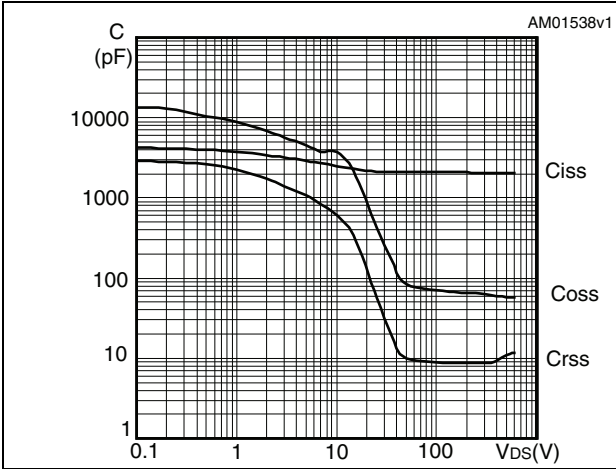


Figure 9. Normalized gate threshold voltage vs temperature

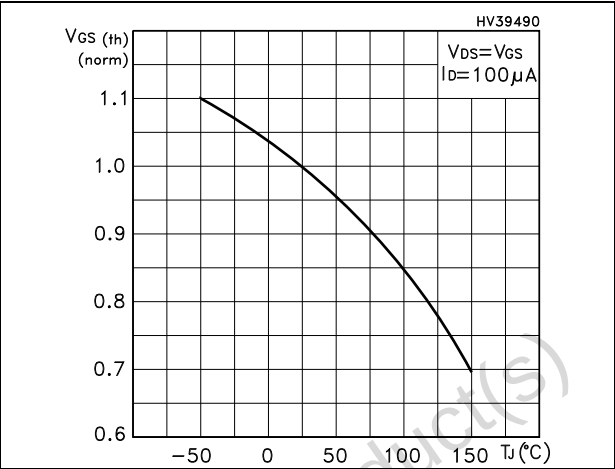


Figure 10. Normalized on-resistance vs temperature

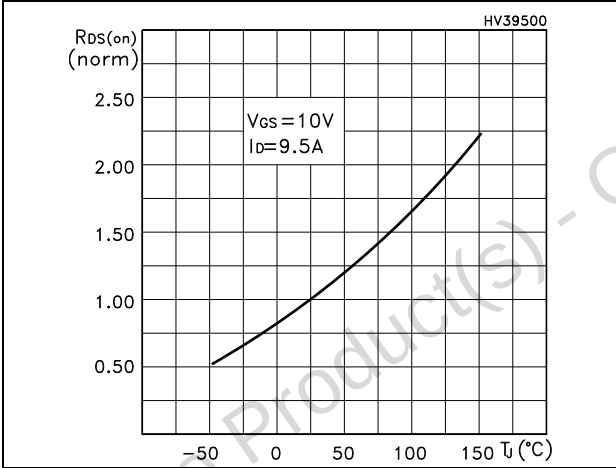


Figure 11. Source-drain diode forward characteristics

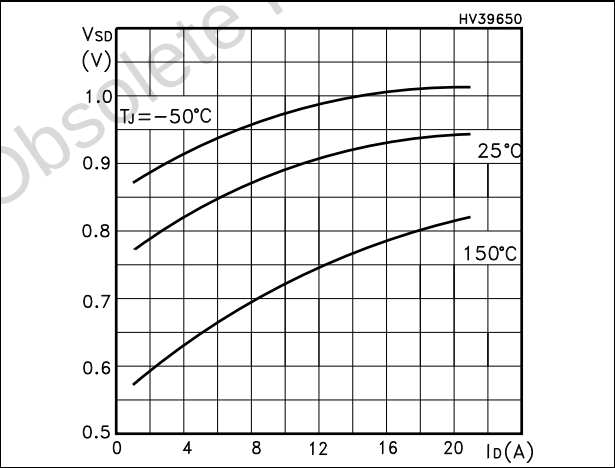
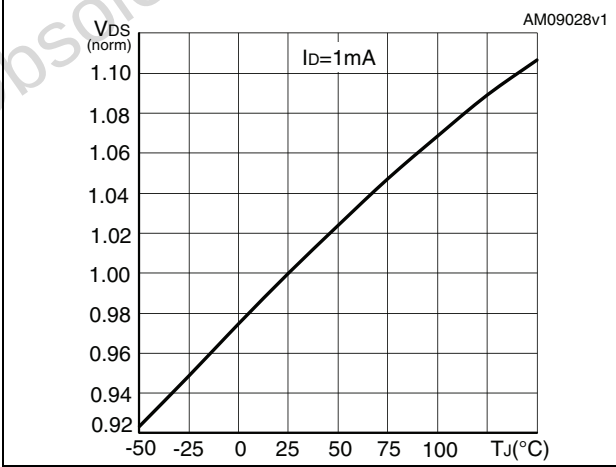


Figure 12. Normalized B_{VDS} vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

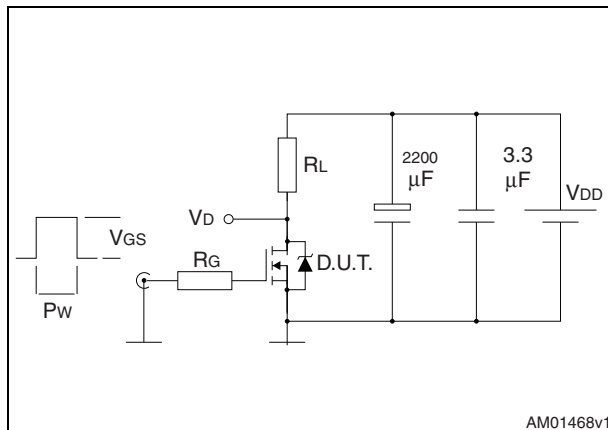


Figure 14. Gate charge test circuit

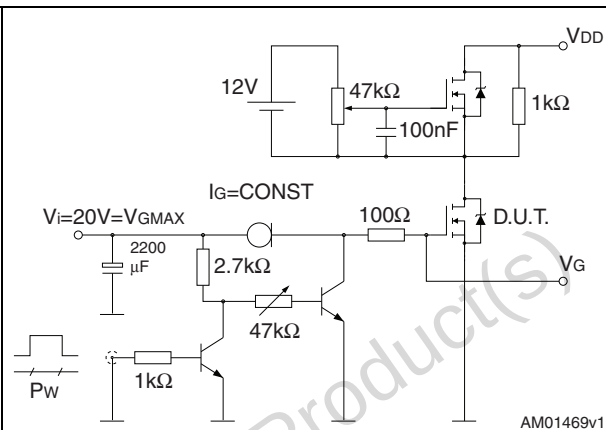


Figure 15. Test circuit for inductive load switching and diode recovery times

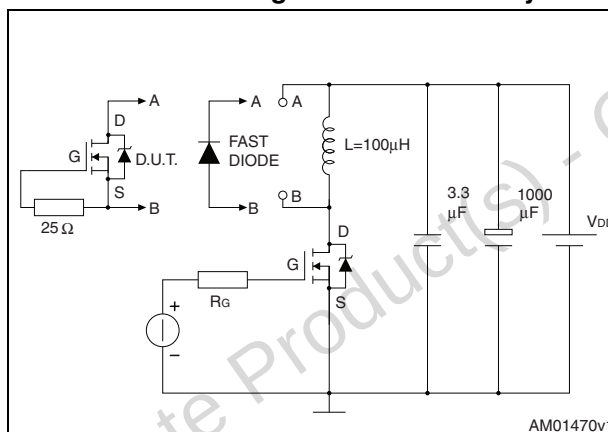


Figure 16. Unclamped inductive load test circuit

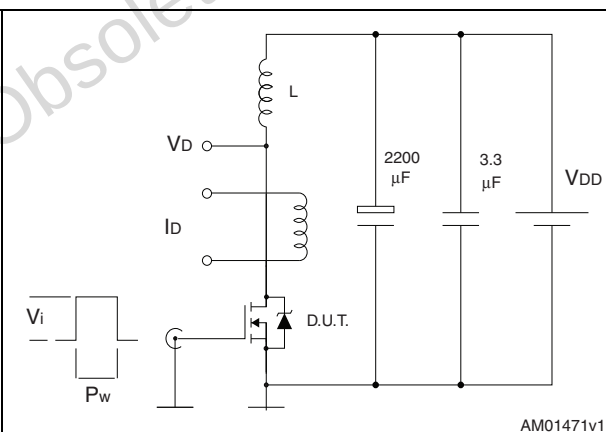


Figure 17. Unclamped inductive waveform

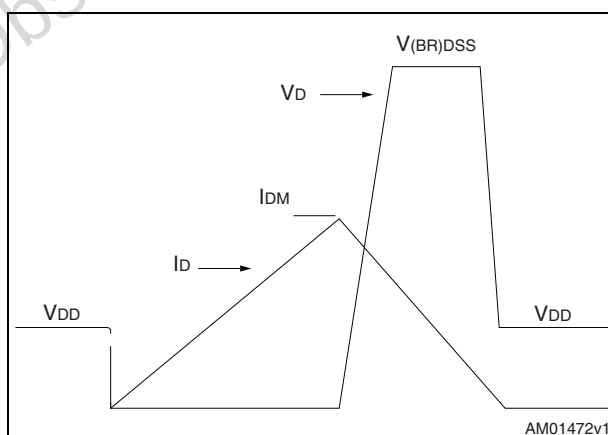
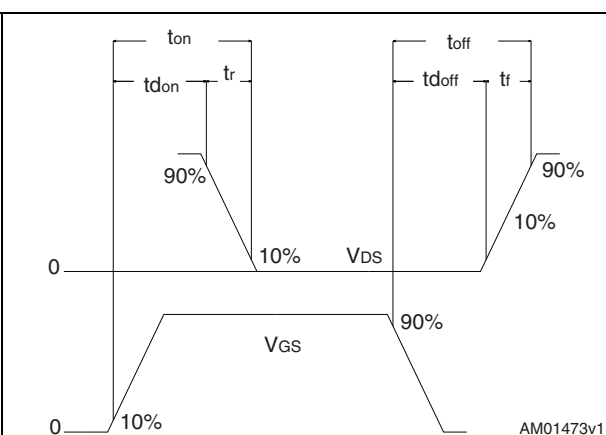


Figure 18. Switching time waveform



4 Package mechanical data

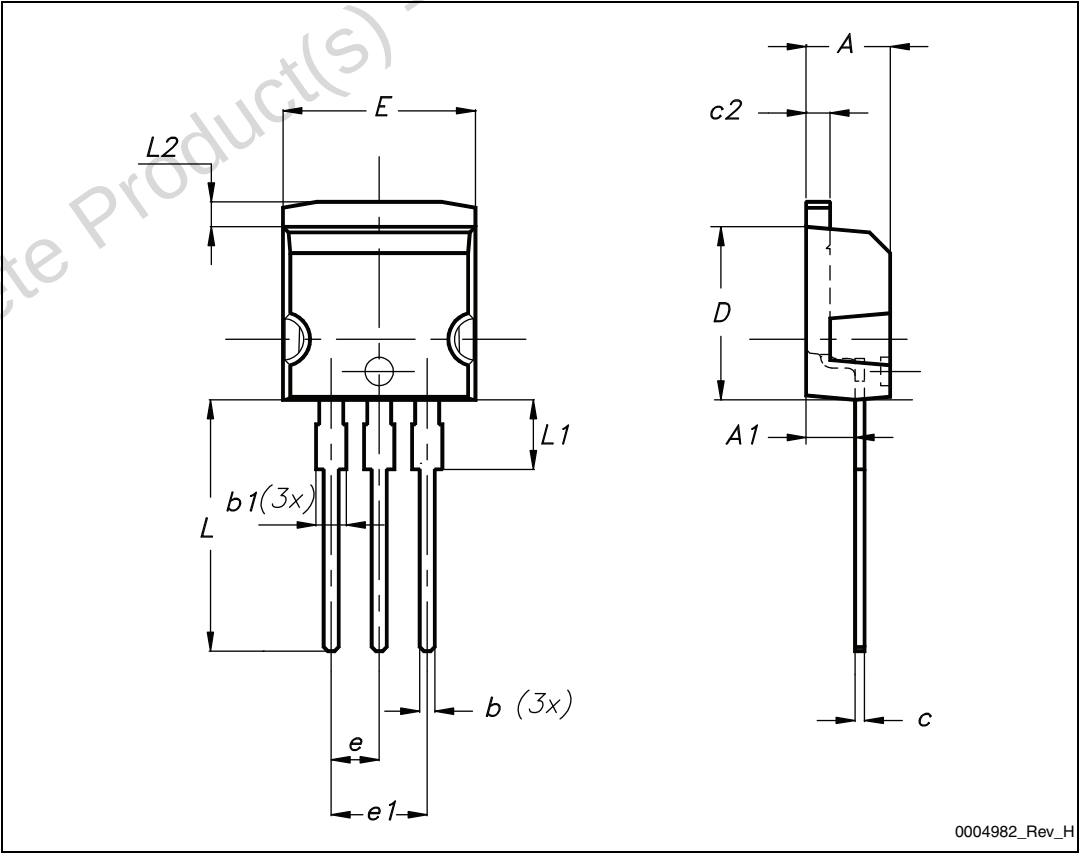
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Obsolete Product(s) - Obsolete Product(s)

Table 8. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 19. I²PAK (TO-262) drawing



0004982_Rev_H

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Jan-2013	1	Initial release. The part number STI23NM60ND previously included in datasheet CD00183341.

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