



STx8NM60N

N-channel 600 V, 0.56 Ω , 7 A MDmesh™ II Power MOSFET
TO-220, TO-220FP, IPAK, DPAK, D²PAK

Features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)} max	I _D
STB8NM60N	650 V	< 0.65 Ω	7 A
STD8NM60N	650 V	< 0.65 Ω	7 A
STD8NM60N-1	650 V	< 0.65 Ω	7 A
STF8NM60N	650 V	< 0.65 Ω	7 A ⁽¹⁾
STP8NM60N	650 V	< 0.65 Ω	7 A

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

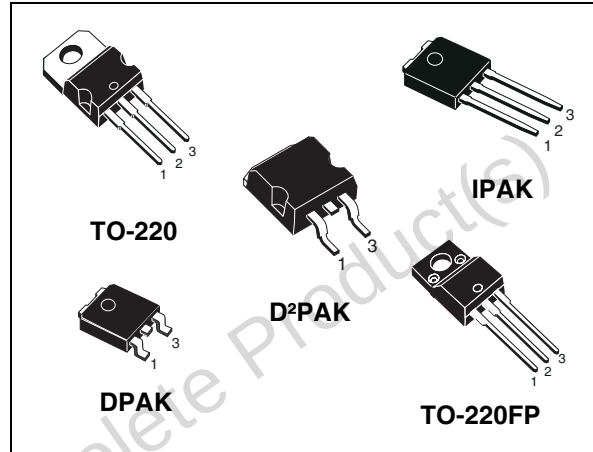
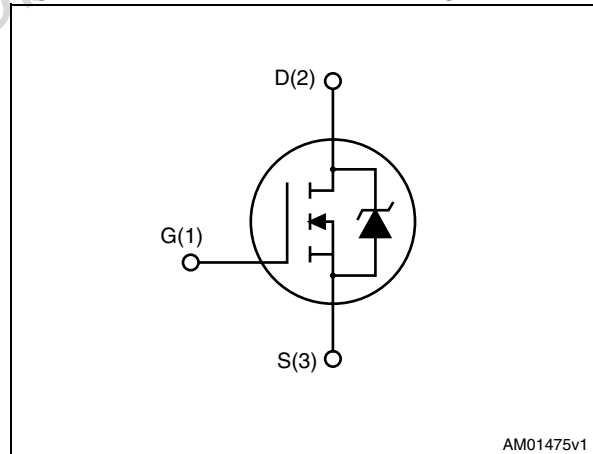


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB8NM60N	B8NM60N	D ² PAK	Tape and reel
STD8NM60N	D8NM60N	DPAK	Tape and reel
STD8NM60N-1	D8NM60N	IPAK	Tube
STF8NM60N	F8NM60N	TO-220FP	Tube
STP8NM60N	P8NM60N	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220, IPAK, DPAK, D ² PAK	TO-220FP	
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	600		V
V_{GS}	Gate-source voltage	± 25		V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	7	7 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	4.3	4.3 ⁽¹⁾	A
$I_{DM}^{(2)}$	Drain current (pulsed)	28	28 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	70	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)	--	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value					Unit
		TO-220	IPAK	DPAK	D ² PAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case	1.78				5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	62.5	100	--	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300					°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	600			V
dv/dt ⁽¹⁾	Drain-source voltage slope	V _{DD} = 480 V, I _D = 7 A, V _{GS} = 10 V	38			V/ns
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _c = 125 °C			1 100	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 3.5 A		0.56	0.65	Ω

1. Characteristics value at turn off on inductive load

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15 V, I _D = 3.5 A		15		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0		560 37 2		pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 480 V		153		pF
R _G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		6		Ω
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 480 V, I _D = 7 A V _{GS} = 10 V (see Figure 19)		19 3 10		nC nC nC

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 3.5\text{ A}$,		10		ns
t_r	Rise time	$R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$		12		ns
$t_{d(off)}$	Turn-off delay time	(see Figure 18),		40		ns
t_f	Fall time	(see Figure 23)		10		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100$		310		ns
Q_{rr}	Reverse recovery charge	$A/\mu s$, $V_{DD} = 30\text{ V}$, $T_j = 25$		2.40		μC
I_{RRM}	Reverse recovery current	$^{\circ}C$ (see Figure 20)		15		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100$		480		ns
Q_{rr}	Reverse recovery charge	$A/\mu s$, $V_{DD} = 30\text{ V}$,		3.50		μC
I_{RRM}	Reverse recovery current	$T_j = 150^{\circ}C$ (see Figure 20)		15		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220, D²PAK

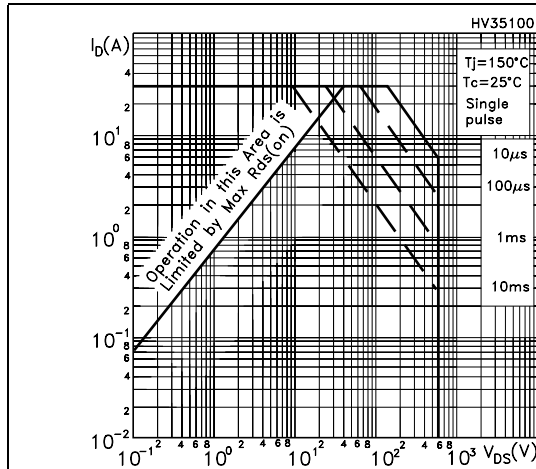


Figure 3. Thermal impedance for TO-220, D²PAK

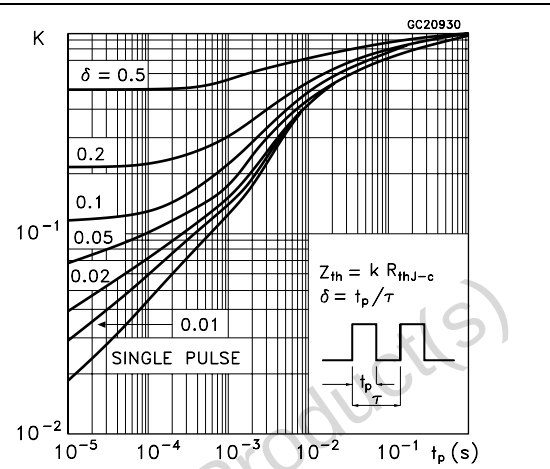


Figure 4. Safe operating area for DPAK, IPAK Figure 5. Thermal impedance for DPAK, IPAK

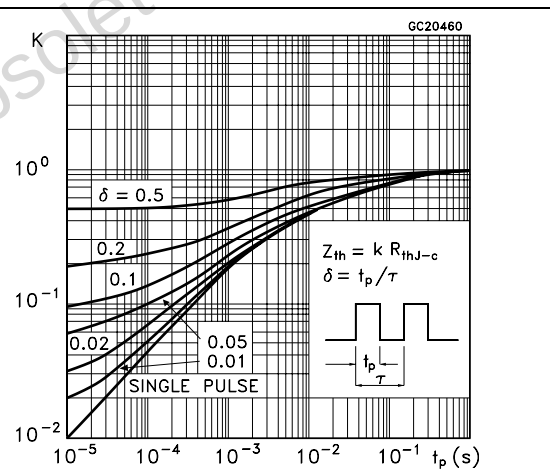
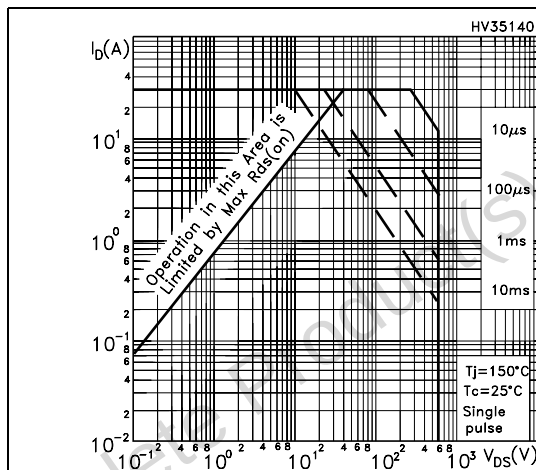


Figure 6. Safe operating area for TO-220FP Figure 7. Thermal impedance for TO-220FP

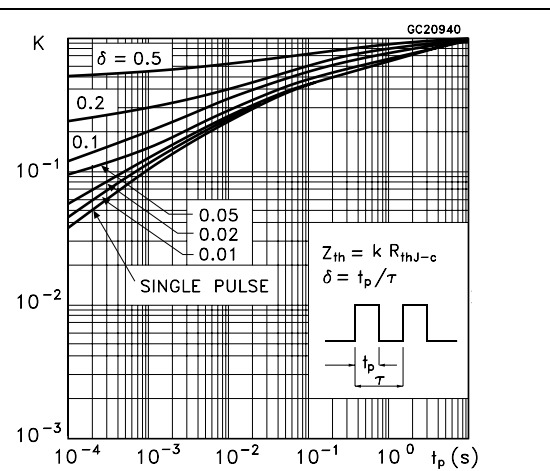
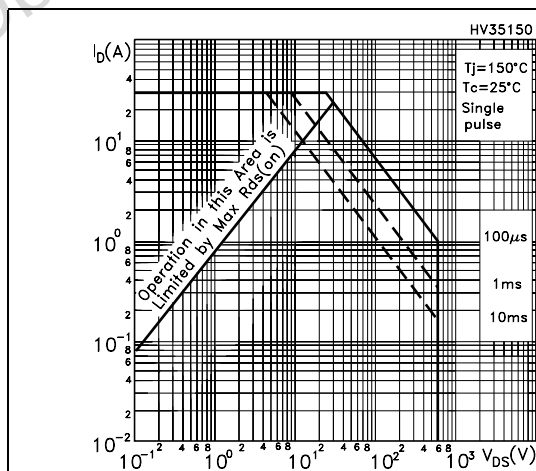


Figure 8. Output characteristics

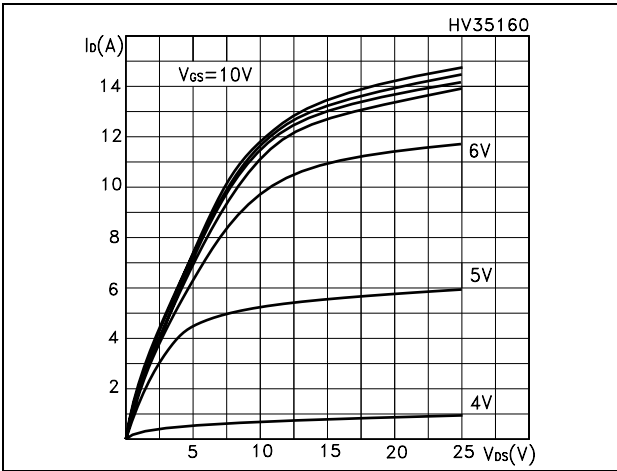


Figure 9. Transfer characteristics

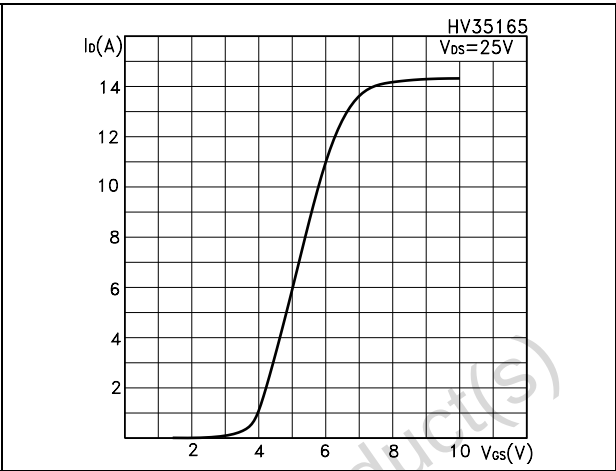


Figure 10. Transconductance

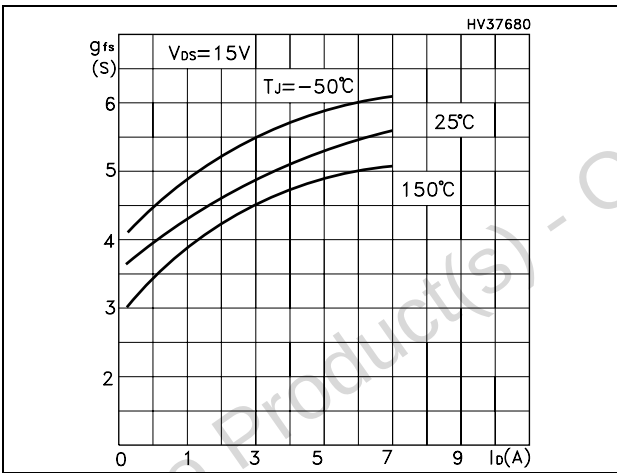


Figure 11. Static-drain source on resistance

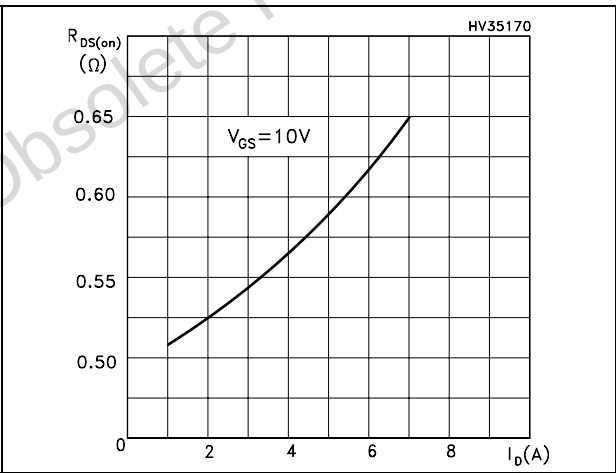


Figure 12. Gate charge vs gate-source voltage

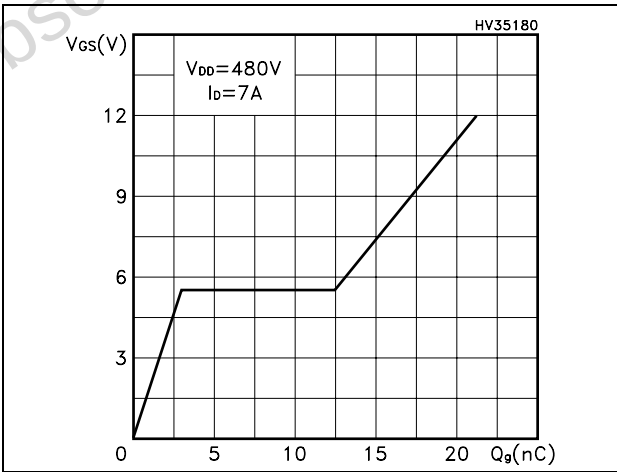


Figure 13. Capacitance variations

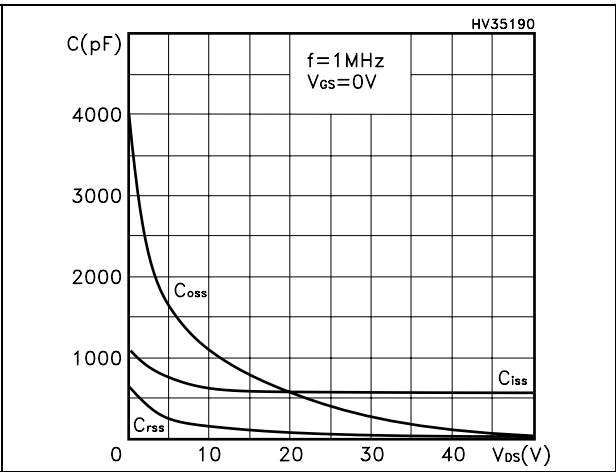


Figure 14. Normalized gate threshold voltage vs temperature

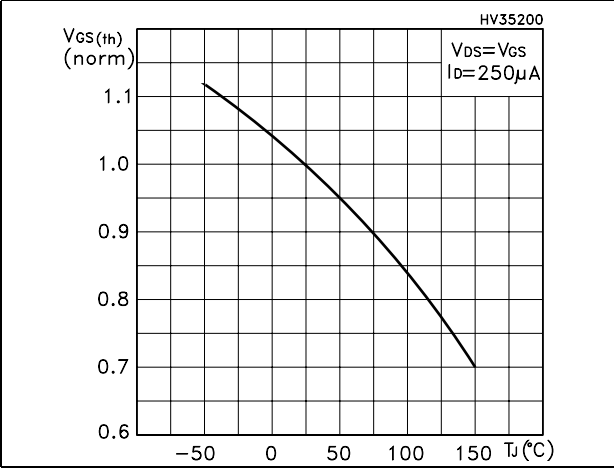


Figure 15. Normalized on resistance vs temperature

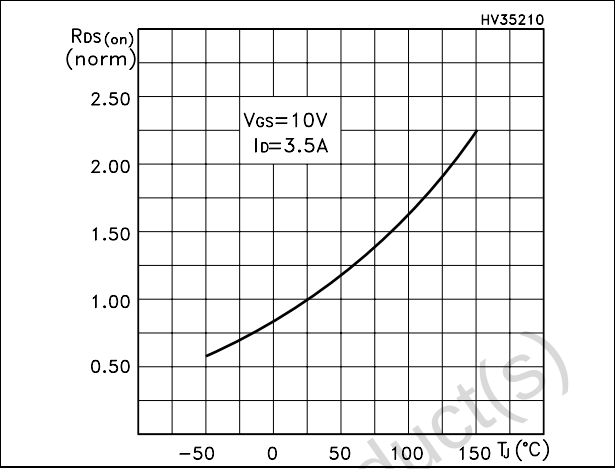


Figure 16. Source-drain diode forward characteristics

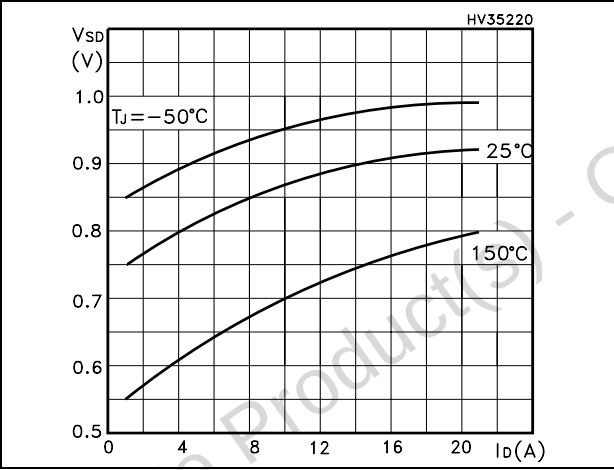
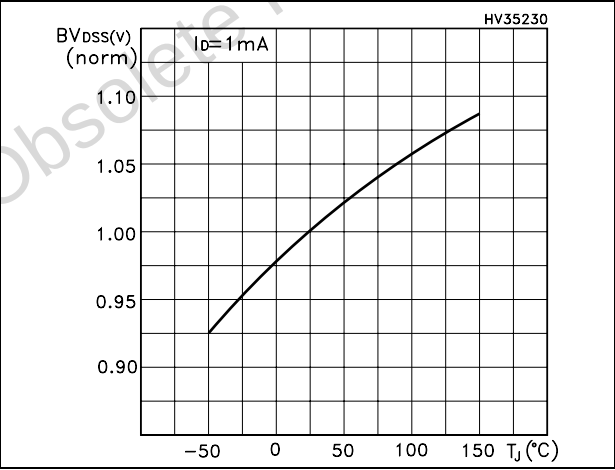


Figure 17. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 18. Switching times test circuit for resistive load

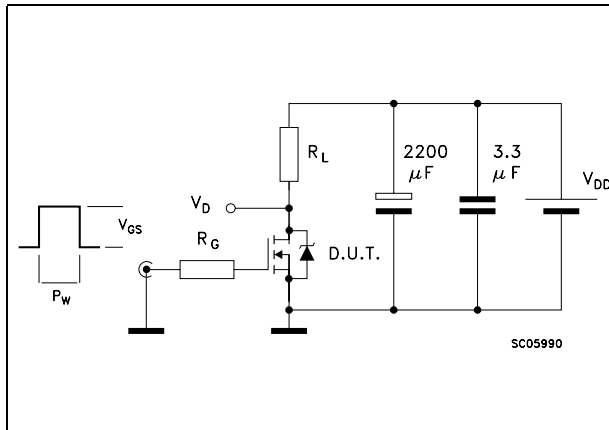


Figure 19. Gate charge test circuit

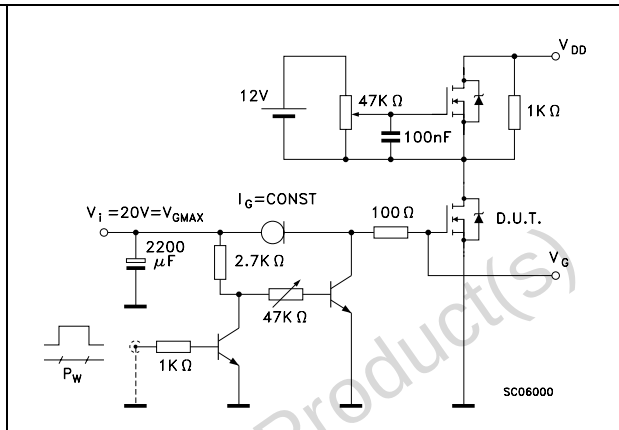


Figure 20. Test circuit for inductive load switching and diode recovery times

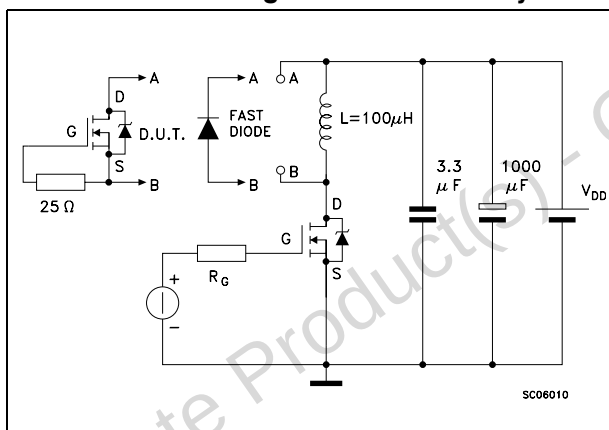


Figure 21. Unclamped inductive load test circuit

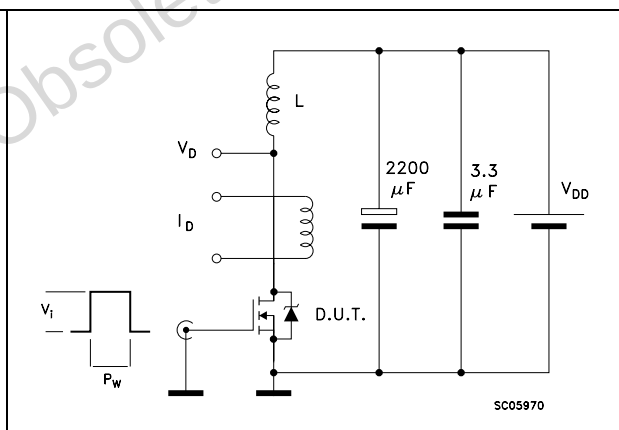


Figure 22. Unclamped inductive waveform

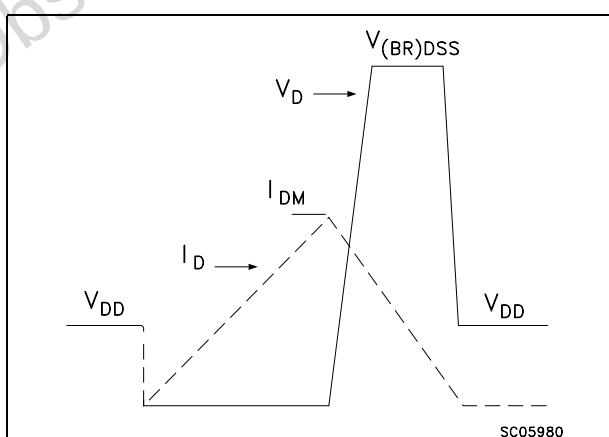
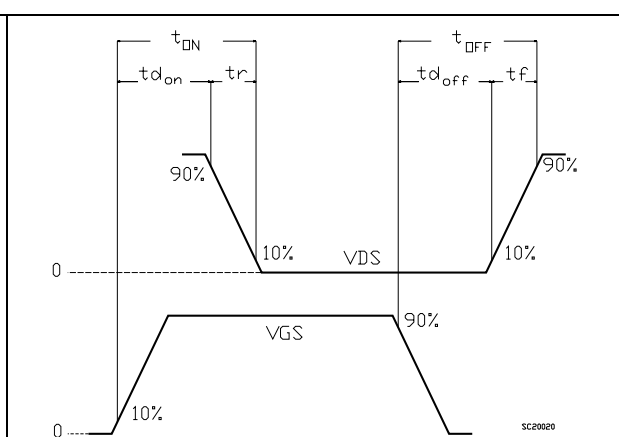


Figure 23. Switching time waveform



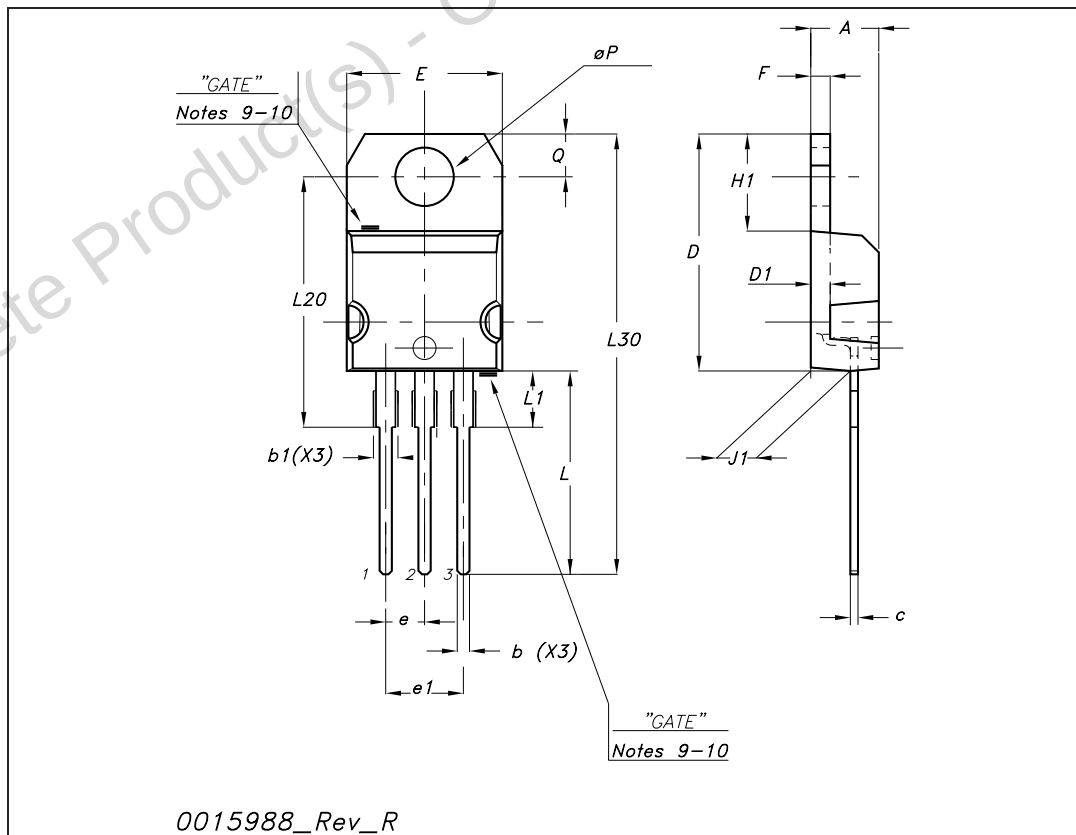
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

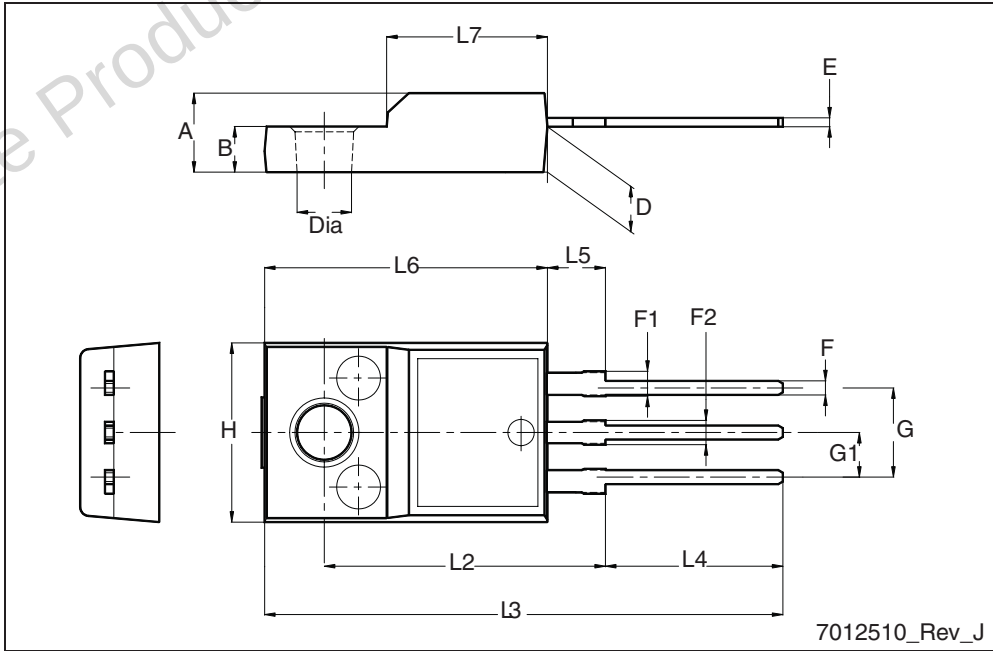
TO-220 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.48		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



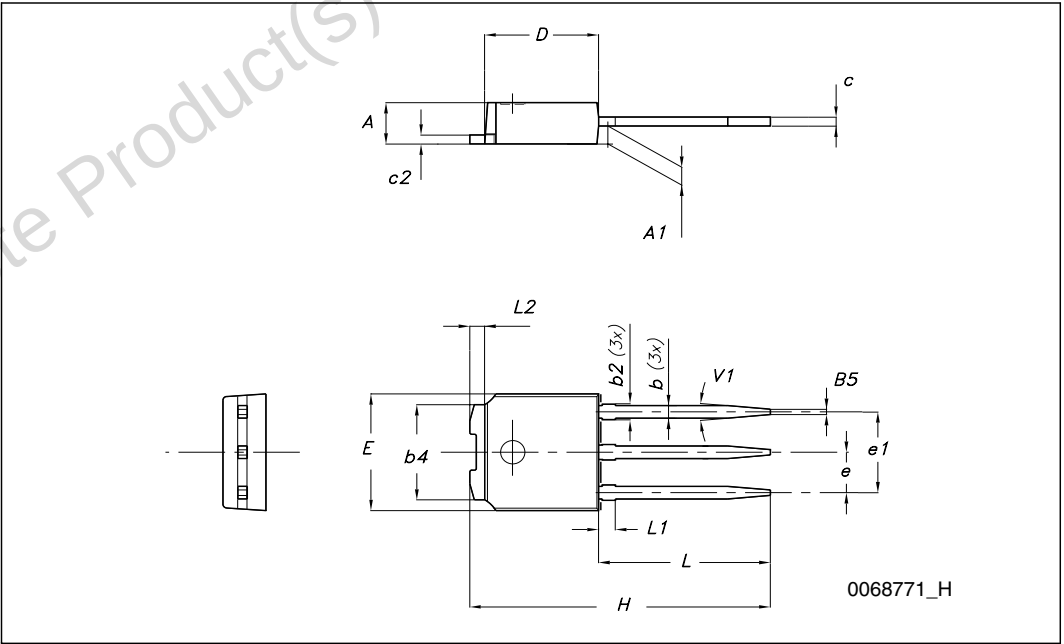
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



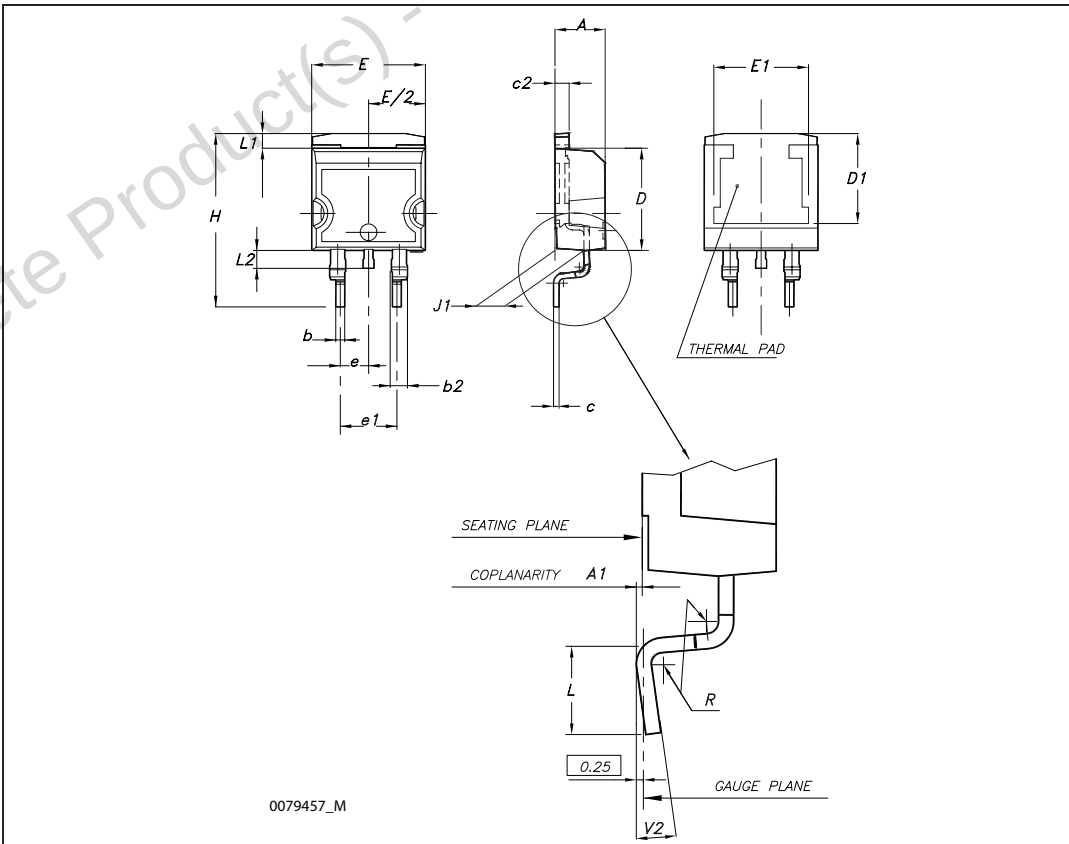
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	



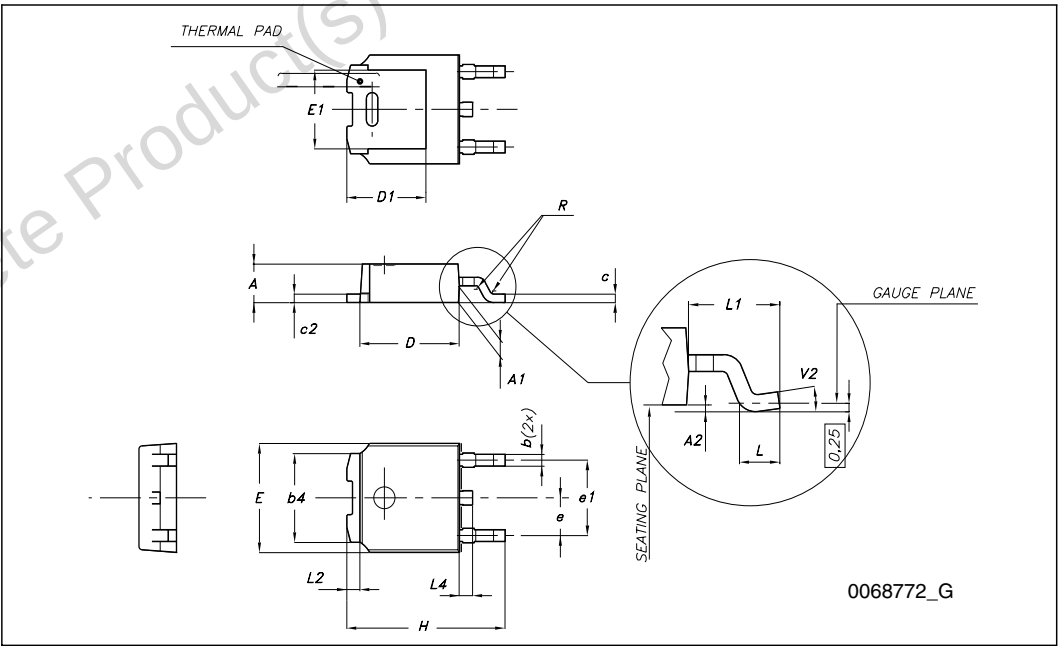
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°



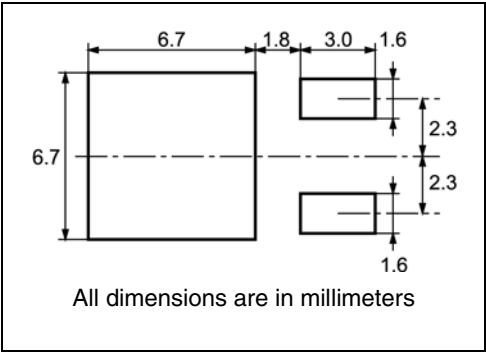
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

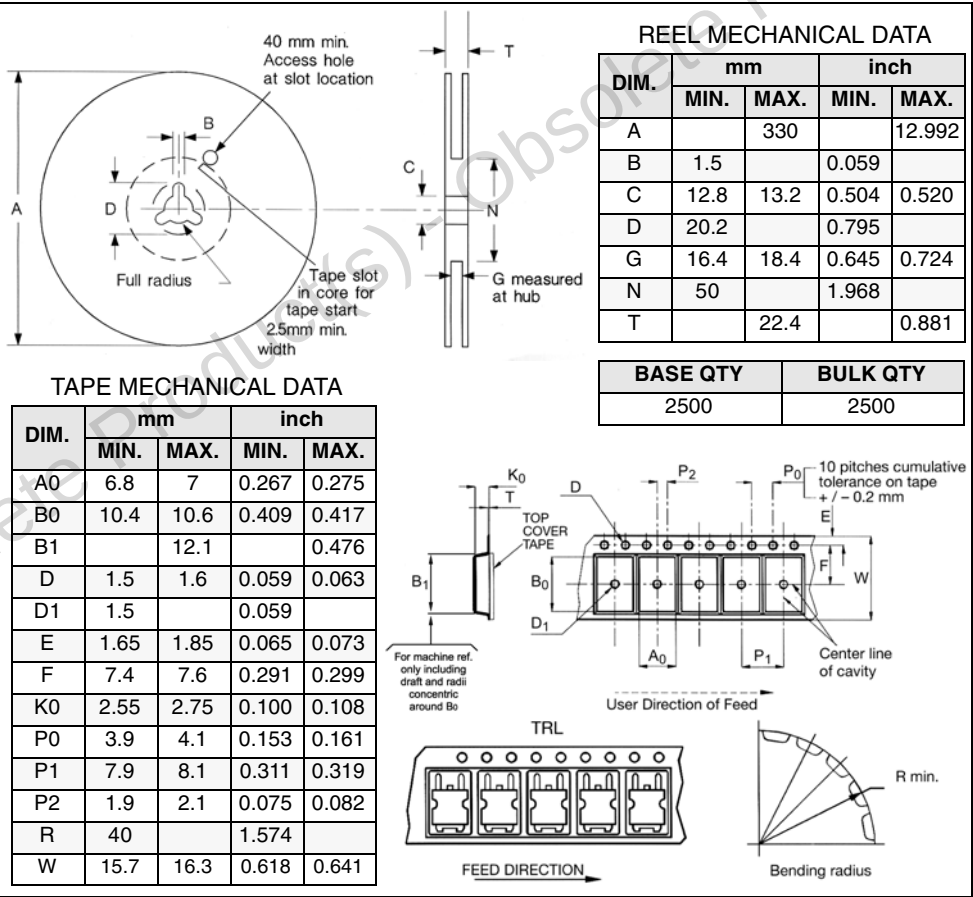


5 Packaging mechanical data

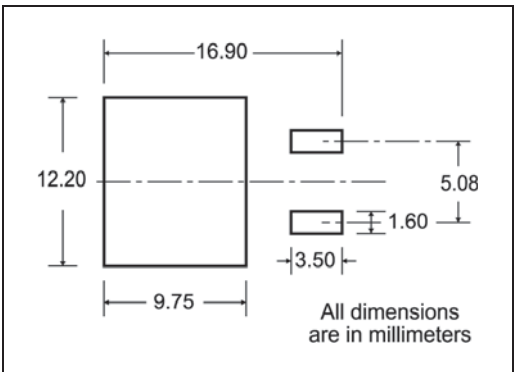
DPAK FOOTPRINT



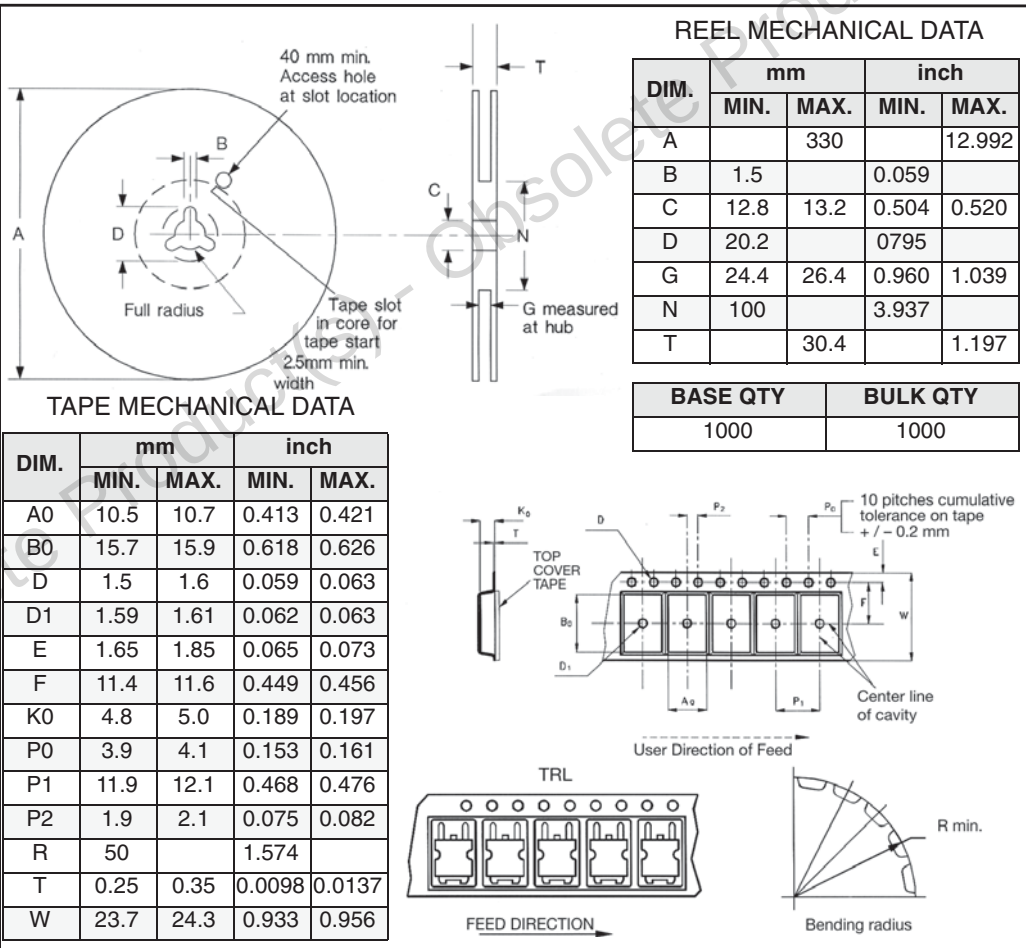
TAPE AND REEL SHIPMENT



D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Aug-2007	1	First release
07-Jan-2008	2	I _{DSS} value has been corrected on Table 5: On/off states
21-Nov-2008	3	Added new package, mechanical data.

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