

6-line IPAD™, low capacitance EMI filter and ESD protection

Features

- High efficiency EMI filtering (-40 dB @ 900 MHz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Lead-free package
- Optimized PCB space occupation: 2.92 mm x 1.29 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on inputs pins (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and wafer level packaging

Complies with the following standards:

- IEC 61000-4-2 Level 4 on input pins
 - 15 kV (air discharge)
 - 8 kV (contact discharge)
- MIL STD 883E - Method 3015-6 Class 3

Application

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU board

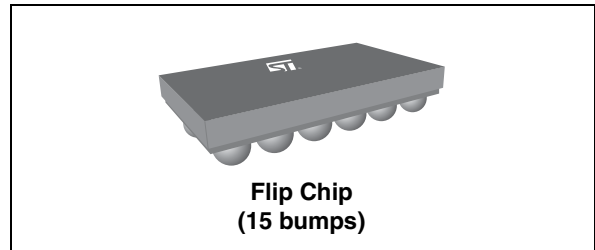


Figure 1. Pin layout (bump side)

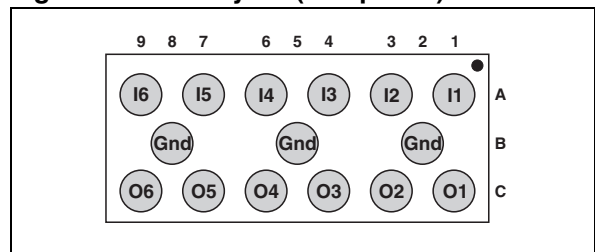
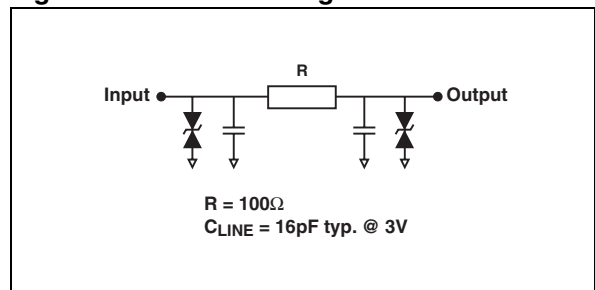


Figure 2. Device configuration



Description

The EMIF06-VID01F2 is a 6-line highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interference.

The EMIF06-VID01F2 Flip Chip packaging means the package size is equal to the die size.

Additionally, this filter includes ESD protection circuitry which prevents damage to the protected device when subjected to ESD surges up to 15 kV.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 2. Electrical characteristics ($T_{amb} = 25\text{ °C}$)

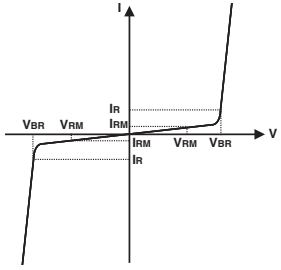
Symbol	Parameter				
V_{BR}	Breakdown voltage				
I_{RM}	Leakage current @ V_{RM}				
V_{RM}	Stand-off voltage				
R	Series resistance between input and output				
C_{line}	Input capacitance per line				
Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{ mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{ V per line}$			500	nA
R	$I = 10\text{ mA}$	80	100	120	Ω
C_{line}	$V_R = 3\text{ V dc, } 1\text{ MHz } V_{OSC} = 30\text{ mV}$		16	19	pF

Figure 3. S21 (dB) attenuation measurement **Figure 4. Analog crosstalk measurement**

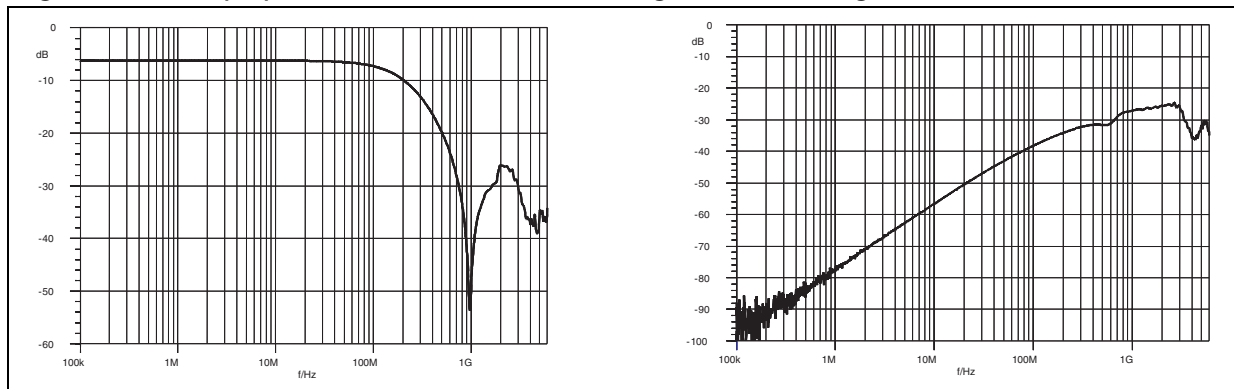


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

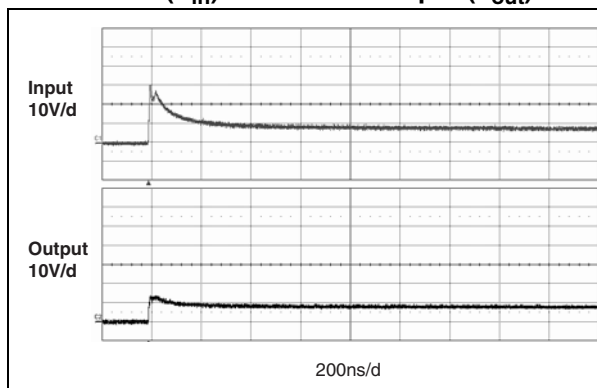


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{in}) and on one output (V_{out})

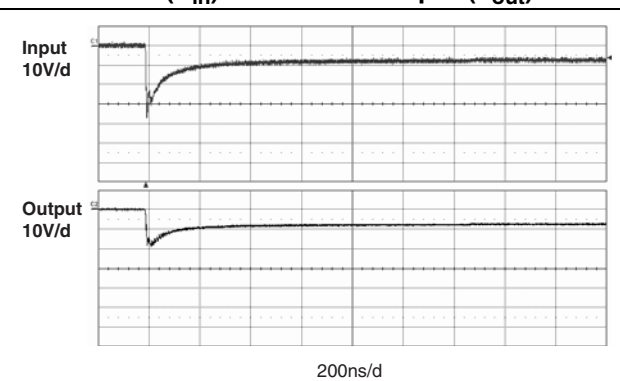
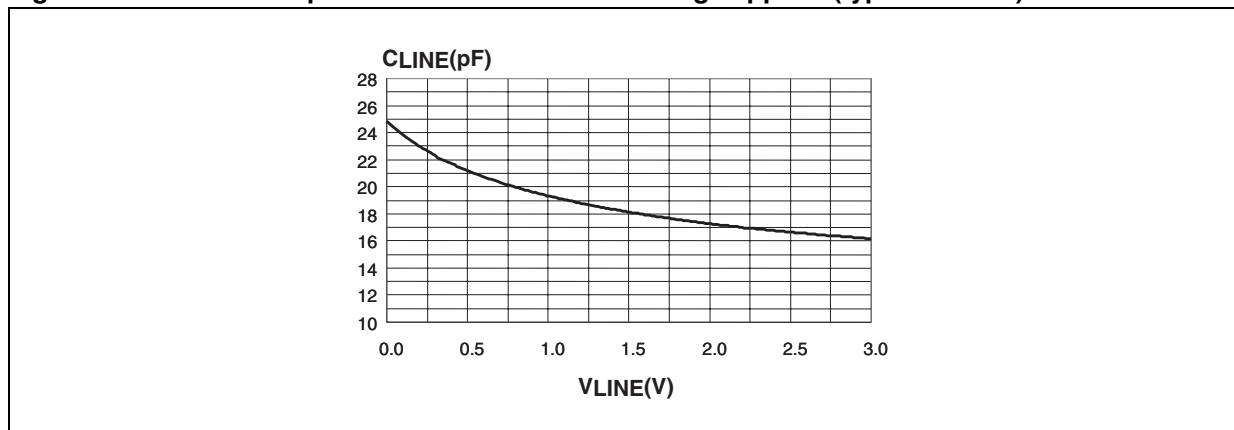
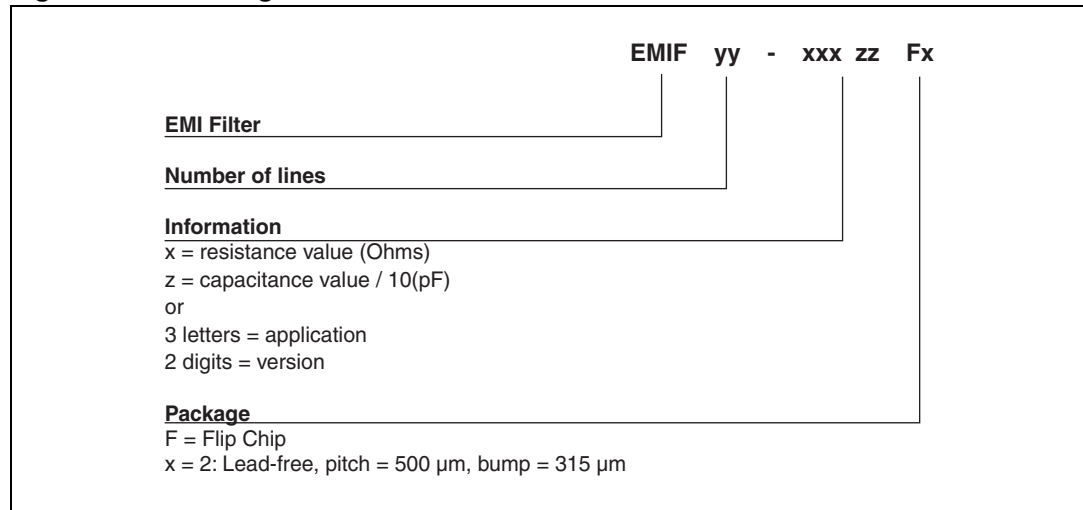


Figure 7. Junction capacitance versus reverse voltage applied (typical values)



2 Ordering information scheme

Figure 8. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 9. Flip Chip package dimensions

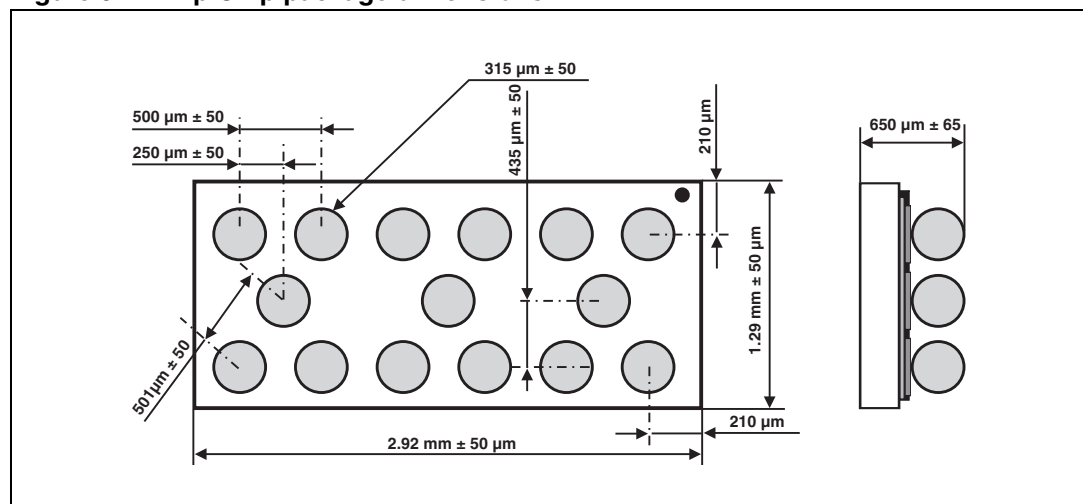


Figure 10. Footprint recommendations Figure 11. Marking

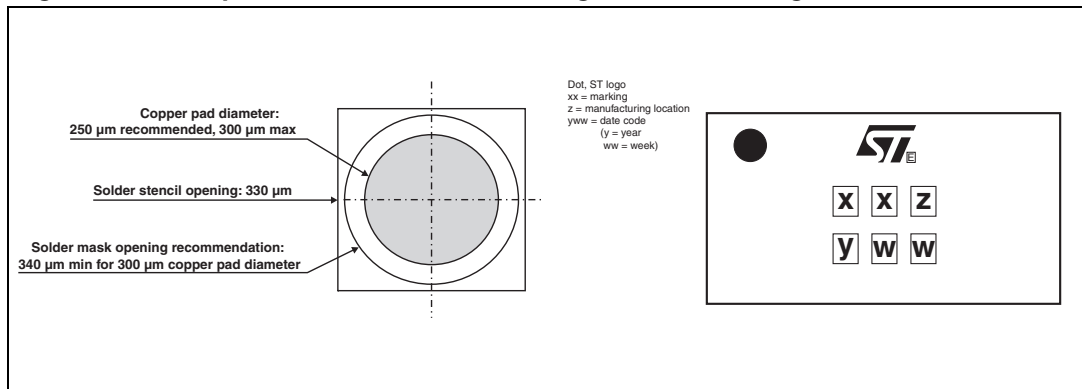
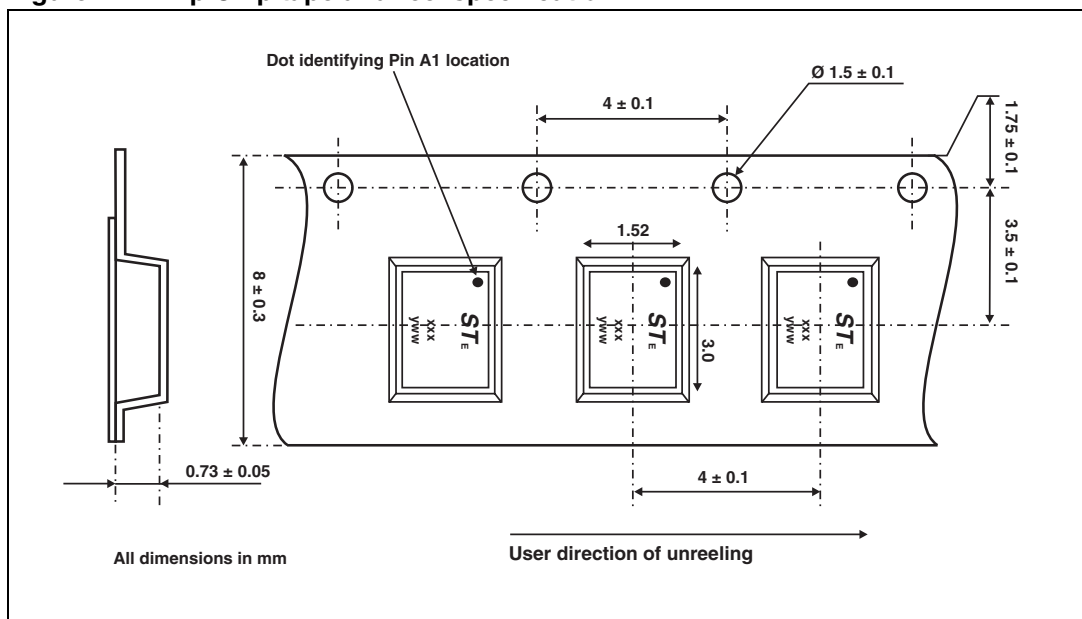


Figure 12. Flip Chip tape and reel specification



Note: More packing information is available in the application note
 AN1235: "Flip Chip: Package description and recommendations for use"
 AN1751: "EMI Filters: Recommendations and measurements"

4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF06-VID01F2	GR	Flip Chip	5.4 mg	5000	Tape and reel 7"

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
15-Feb-2005	1	First issue.
28-Apr-2008	2	Added ECOPACK statement. Updated Figure 9 , Figure 11 , and Figure 12 . Reformatted to current standards.

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