# EMIF06-HSD03F3



### Datasheet

# 6-line low capacitance EMI filter array with integrated ESD protections for microSD Card<sup>TM</sup>



(17 bumps)



Product status link EMIF06-HSD03F3

Product summary		
Order code	EMIF06-HSD03F3	
Package	CSP P 0.4 mm	
Packing	Tape and reel	

### Features

- EMI filter with integrated ESD protection on each SD card pins in one easy routing package
- Very low line capacitance to compensate long PCB tracks
- Ultra-low leakage current at V<sub>RM</sub>: 20 nA max
- Very low PCB space consumption: 1.1 mm x 2.4 mm
- ECOPACK2 RoHS compliant component
- Benefits
  - Very good matching between lines thanks to proprietary solid-state silicon technology
  - Very low capacitance between lines to GND for optimized data integrity and speed
  - Enhanced ESD protection with fast response time and low clamping voltage: IEC 61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
  - Integrated ESD protection of VCC and DET minimizes PCB space
  - Easy PCB routing thanks to flow-through package pinout

### Complies with following standards:

- UL94, V0
- IEC 61000-4-2 exceeding level 4: ±18 kV (air discharge Ix pins)
- IEC 61000-4-2 exceeding level 4: ±18 kV (contact discharge Ix pins)

# **Applications**

- SD3.0, UHS-1 SDR104 (208 MHz)
- Secure Digital (SD) Memory Card Interfaces
  - Mobile phones
  - Digital still cameras
  - Portable electronic equipment
  - Navigation systems
  - Security cameras

# Description

The EMIF06-HSD03F3 is a 6-line highly integrated low pass filter designed to suppress EMI / RFI noise for micro secure digital interface.

This filter integrates ESD protection diodes, designed to protect sensitive devices from damage when subjected to ESD surges up 18 kV contact.

The very low line capacitance ensures a high level of signal integrity without compromising protection of sensitive ICs against transient surge events.



# **1** Pin configuration and functions

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#### Table 1. Pin description

Pin #	Name	Description		
A1	01	Filtered line – IC side		
A3	11	Filtered line – SD card side		
B2	VCC	Power supply input		
C1	02	Filtered line – IC side		
C3	12	Filtered line – SD card side		
D2	GND	Ground		
E1	O3	Filtered line – IC side		
E3	13	tered line – SD card side		
F2	GND	ound		
G1	04	tered line – IC side		
G3	14	ered line – SD card side		
H2	GND	Ground		
11	O5	Filtered line – IC side		
13	15	Filtered line – SD card side		
J2	DET	Card detection pin		
K1	O6	Filtered line – IC side		
K3	16	Filtered line – SD card side		

### Figure 1. Pinout (bump side)



Note:

For lower ground parasitics leading to better filtering performances and ESD robustness, GND bumps must be connected together on PCB. Ground loop inductance can be reduced by using multiple vias to make the connection to the ground plane.



#### **Characteristics** 2

Symbol	Parameter Value Unit				
		IEC 61000-4-2 level 4 - C = 150 pF, R = 330 $\Omega$ for IX pins:			
V <sub>PP</sub> Peak put		Air discharge	±18		
	Peak pulse voltage	Contact discharge	±18		
		IEC 61000-4-2 level 4 - C = 150 pF, R = 330 $\Omega$ for OX pins:		ĸv	
		Air discharge	±10		
		Contact discharge	±10		
Tj	Maximum junction temperature range		125	°C	
T <sub>op</sub>	Maximum operating temperature range		-40 to +125	°C	
T <sub>stg</sub>	Storage temperature range		-55 to +150	°C	

### Table 2. Absolute maximum ratings (T<sub>amb</sub> = 25 °C)

### Figure 2. Electrical characteristics (definitions)

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VRM	Stand-off voltage	Ipp .
I <sub>RM</sub>	Leakage current at VRM	
VBR	Breakdown voltage	I <sub>BR</sub>
I <sub>BR</sub>	Breakdown current	
Vcl	Clamping voltage	VRM VBR VCL
Ірр	Peak pulse current	

### Table 3. Electrical characteristics (T<sub>amb</sub> = 25 °C)

Symbol	Parameter	Test conditions		Min.	Тур.	Max.	Unit
V <sub>RM</sub>	Reverse stand-off voltage					3	V
I <sub>RM</sub>	Reverse leakage current at $V_{RM}$	V <sub>RM</sub> = 3.0 V p	er line			20	nA
V <sub>BR</sub>	Reverse breakdown voltage	I <sub>BR</sub> = 1 mA		5		9	V
R <sub>I/O</sub>	Serial resistance	Between any I	x and Ox		1.0		Ω
L <sup>(1)</sup>	Serial inductance	Between any Ix and Ox			1.0		nH
V <sub>CL</sub> <sup>(1)</sup>	ESD clamping voltage	IEC 61000-4-2–C = 150 pF, R = 330 $\Omega$ , +8 kV contact discharge, measured at 30 ns			18.5		V
<b>P</b> <sub>p</sub> (1)	Dynamic registance	IO-GND (positive polarity			650		mΩ
		rp = 1001is	GND-IO (negative polarity)		320		mΩ
C <sub>I/O-GND</sub> <sup>(1)</sup>	Line capacitance between Ix/Ox / GND	$V_R$ = 0 V, 1 MHz, $V_{OSC}$ = 30 mV			2.5	3.0	pF
C <sub>VCC-GND</sub> <sup>(1)</sup>	Line capacitance between $V_{CC}$ / GND	V <sub>R</sub> = 0 V, 1 MHz, V <sub>OSC</sub> = 30 mV			40		pF
C <sub>DET-GND</sub> <sup>(1)</sup>	Line capacitance between DET / GND	V <sub>R</sub> = 0 V, 1 MHz, V <sub>OSC</sub> = 30 mV			40		pF

1. Specified by design, not tested in production.



# 2.1 Characteristics (curves)









Figure 7. TLP characteristic











# **3** Technical information

# 3.1 Application diagram



#### Note:

More information is available in the application notes:

- AN1751, "EMI filters: recommendations and measurements"
- AN4541: "EMI Filters for SD3.0 card: High speed SD card protection and filtering devices"

# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

### 4.1 Chip scale package (CSP) pitch 0.4 mm package information

Epoxy meets UL94, V0

### Figure 13. Chip scale package (CSP) pitch 0.4 mm package outline



### Table 4. Chip scale package (CSP) pitch 0.4 mm package mechanical data

	Dimensions				
Ref.		Millimeters			
	Min.	Тур.	Max.		
А	0.560	0.605	0.650		
A1	0.180	0.205	0.230		
A2	0.380	0.400	0.420		
b	0.230	0.250	0.290		
D	1.060	1.100	1.140		
D1		0.692			
SD		0.346			
E	2.360	2.40	2.440		
E1		2.00			
SE		0.200			
е		0.400			
fD	0.194	0.204	0.214		
fE	0.190	0.200	0.210		
ccc			0.075		









### Figure 20. Tape and reel outline



Note:

Pocket dimensions are not on scale Pocket shape may vary depending on package

#### Table 5. Tape dimension values

	Dimensions				
Ref.		Millimeters			
	Min.	Тур.	Max.		
D0	1.45	1.50	1.60		
D1	0.35	0.40	0.45		
F	3.45	3.50	3.55		
KO	0.64	0.69	0.74		
P0	3.90	4.00	4.10		
P1	3.90	4.00	4.10		
P2	1.95	2.00	2.05		
W	7.90	8.00	8.30		

#### Figure 21. Tape leader and trailer dimensions







# 5 Recommendation on PCB assembly

## 5.1 Reflow profile





*Note:* Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.



# 6 Ordering information



### Table 6. Ordering information

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF06-HSD03F3	KK <sup>(1)</sup>	CSP P 0.4 mm	3.4 mg	5000	Tape and reel (7")

1. The marking can be rotated by multiples of 90° to differentiate assembly locations.

# **Revision history**

### Table 7. Document revision history

Date	Version	Changes	
19-Nov-2013	1	Initial release.	
09-Jan-2014	2	Corrected typographical error.	
06-Jan-2015	3	Added mention for new AN4541.	
06-Oct-2016	4	Updated Figure 1. Pin configuration (bump side).	
10-Jun-2022	5	Updated Section 4.1 Chip scale package (CSP) pitch 0.4 mm package information. Minor text changes.	

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