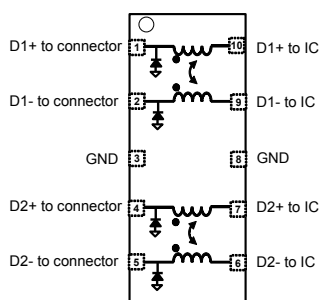


## Common mode filter with ESD protection for high speed serial interface



μQFN-10L  
1.35 mm x 2.2 mm x 0.5 mm



### Product status

ECMF4-20A42N10

### Features

- 5GHz differential bandwidth to comply with HDMI 2.0, HDMI 1.4, USB 3.1, MIPI, Display port, etc.
- High common mode attenuation on LTE, GSM, GPS and WLAN frequencies:
  - -13 dB at 0.7 GHz
  - -23 dB at 1.5 GHz
  - -25 dB at 2.4 GHz
  - -23 dB at 2.7 GHz
  - -13 dB at 5.0 GHz
- Very low PCB space consumption
- Thin package: 0.5 mm max.
- Lead free and RoHS package
- High reduction of parasitic elements through integration
- Complies with IEC 61000-4-2 level 4 standards:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

### Applications

- Notebook, laptop
- Streaming box
- Set top box
- Portable devices

### Description

The is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like HDMI 2.0, HDMI1.4, USB 3.1 Gen 1, Ethernet, MIPI, Display port and other high speed serial interfaces.

It has a very large differential bandwidth to comply with these standards and can also protect and filter 2 differential lanes.

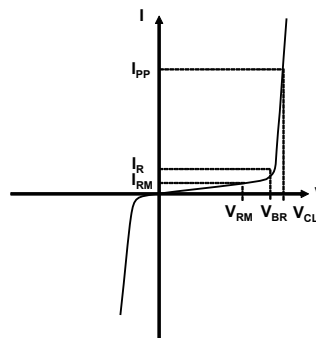
# 1 ECMF4-20A42N10 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

| Symbol    | Parameter                                     | Value                               | Unit               |
|-----------|---|-------------------------------------|--------------------|
| $V_{PP}$  | Peak pulse voltage                            | IEC 61000-4-2:<br>Contact discharge | kV                 |
|           |   | Air discharge                       |                    |
| $I_{RMS}$ | Maximum RMS current                           | 100                                 | mA                 |
| $T_{op}$  | Maximum operating temperature range           | -55 to +125                         | $^{\circ}\text{C}$ |
| $T_{stg}$ | Storage temperature range                     | -55 to +150                         |                    |
| $T_L$     | Maximum temperature for soldering during 10 s | 260                                 |                    |

**Figure 2. Electrical characteristics (definitions)**

$V_{RM}$  Maximum stand-off voltage  
 $V_{CL}$  Clamping voltage at peak pulse current  $I_{PP}$   
 $I_{RM}$  Leakage current at  $V_{RM}$   
 $I_{PP}$  Peak pulse current  
 $V_{BR}$  Breakdown voltage  
 $C_{DIODE}$  ESD diode capacitance  
 $R_{DC}$  DC serial resistance  
 $f_c$  Differential cut off frequency

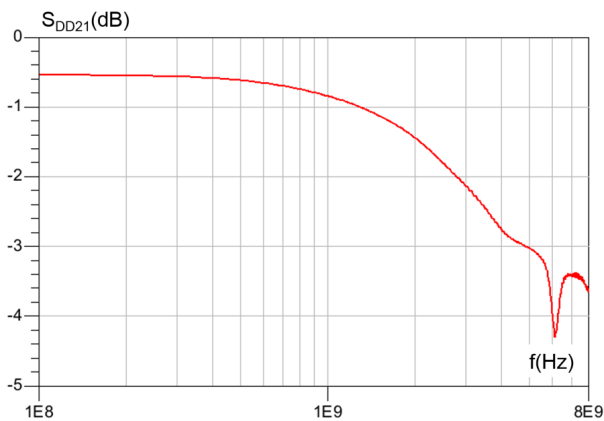
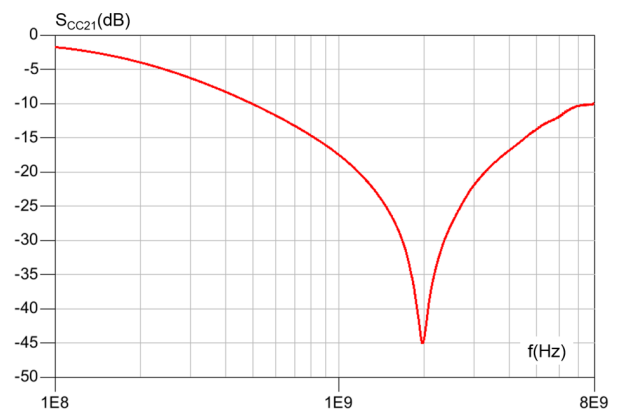
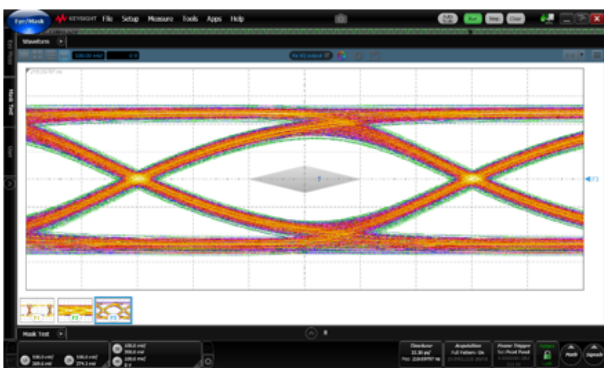
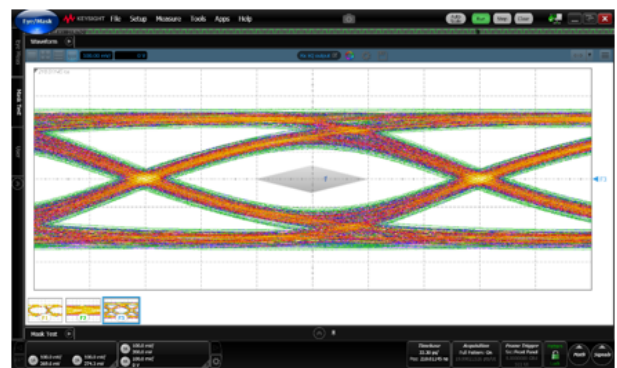

**Table 2. Electrical characteristics ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

| Symbol      | Test conditions  | Min. | Typ. | Max. | Unit     |
|-------------|--|------|------|------|----------|
| $V_{BR}$    | $I_R = 1\text{ mA}$  | 4.5  | 5.5  |      | V        |
| $I_{RM}$    | $V_{RM} = 3\text{ V per line}$   |      |      | 100  | nA       |
| $R_{DC}$    | DC serial resistance, $I_{DC} = 20\text{ mA}$  |      | 5.5  |      | $\Omega$ |
| $f_c$       | Differential mode cut-off frequency at -3 dB   |      | 5.0  |      | GHz      |
| $V_{CL}$    | $I_{PP} = 1\text{ A} - 8/20\text{ }\mu\text{s}$  |      |      | 10   | V        |
|             | 8 kV contact discharge after 30 ns, IEC 61000-4-2  |      | 11   |      |          |
| $C_{diode}$ | $V_{BIAS} = 0\text{ V}$ , $2.5\text{ GHz} \leq f \leq 6\text{ GHz}$ , $V_{OSC} = 30\text{ mV}$ |      | 0.35 | 0.45 | pF       |

**Table 3. Pin description**

| Pin number | Description      | Pin number | Description |
|------------|------------------|------------|-------------|
| 1          | D1+ to connector | 6          | D2- to IC   |
| 2          | D1- to connector | 7          | D2+ to IC   |
| 3          | GND              | 8          | GND         |
| 4          | D2+ to connector | 9          | D1- to IC   |
| 5          | D2- to connector | 10         | D1+ to IC   |

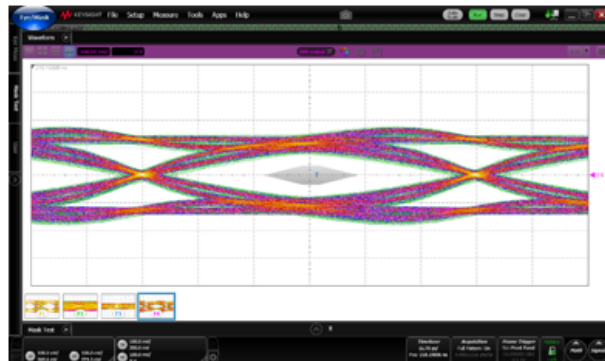
## 1.1 Characteristics (curves)

**Figure 3. Differential attenuation versus frequency ( $Z_0 \text{ DIFF} = 100 \Omega$ )**

**Figure 4. Common mode attenuation versus frequency ( $Z_0 \text{ COM} = 50 \Omega$ )**

**Figure 5. USB3.1 Gen 1 5.0 Gbps eye diagram without ECMF4-20A42N10 (test conditions: type C connector, reference cable and equalizer)**

**Figure 6. USB3.1 Gen 1 5.0 Gbps eye diagram with ECMF4-20A42N10 (test conditions: type C connector, reference cable and equalizer)**


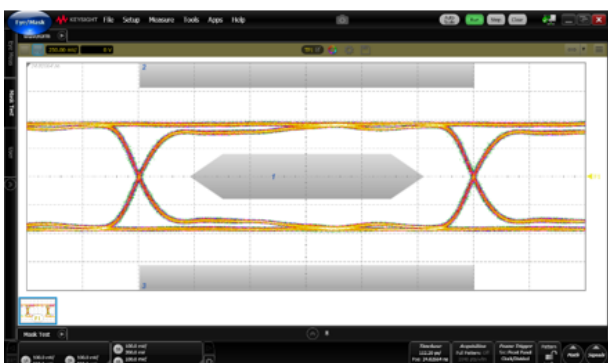
**Figure 7.** USB3.1 Gen 2 10.0 Gbps eye diagram without ECMF4-20A42N10 (test conditions: type C connector, reference cable equalizer with  $A_{DC} = 6$  dB and DFE)



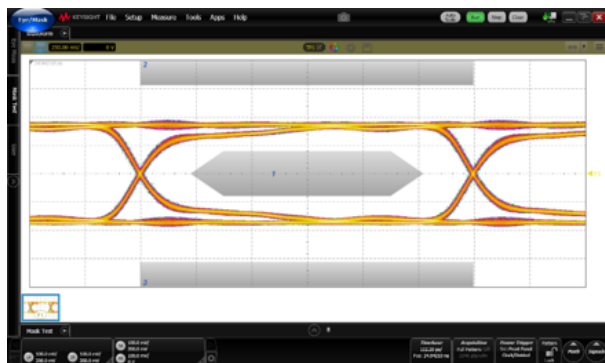
**Figure 8.** USB3.1 Gen 1 10.0 Gbps eye diagram with ECMF4-20A42N10 (test conditions: type C connector, reference cable equalizer with  $A_{DC} = 6$  dB and DFE)



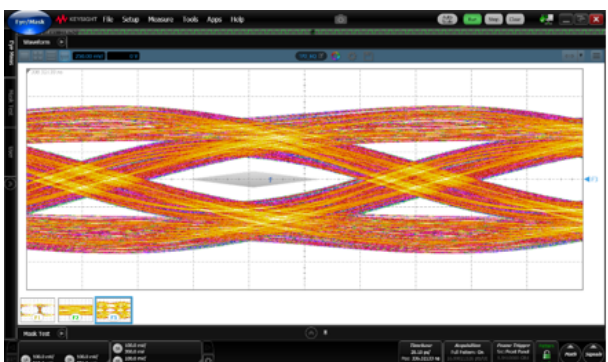
**Figure 9.** HDMI1.4 1.485 Gbps eye diagram without ECMF4-20A42N10



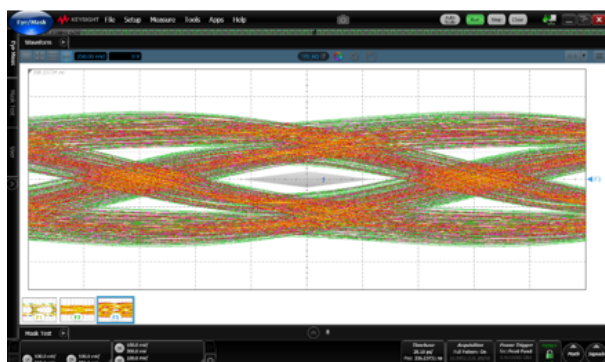
**Figure 10.** HDMI1.4 1.485 Gbps eye diagram with ECMF4-20A42N10



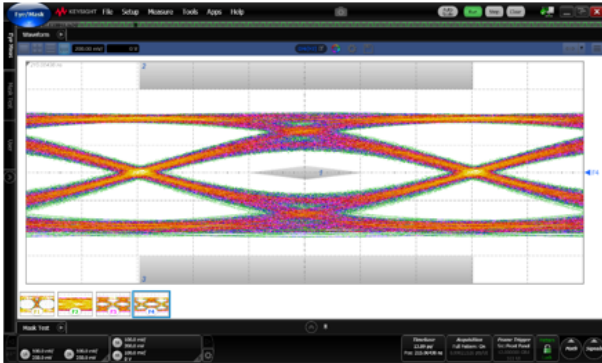
**Figure 11.** HDMI2.0 5.94 Gbps eye diagram without ECMF4-20A42N10. (test conditions : worst case cable and equalizer)



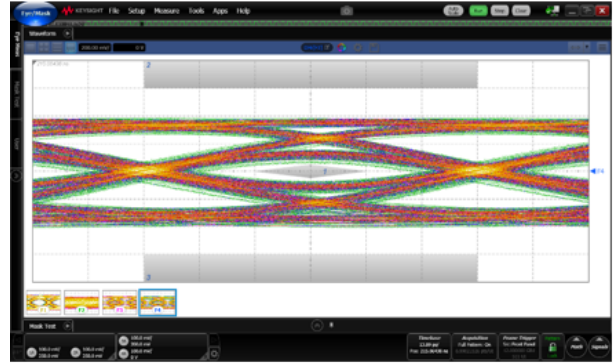
**Figure 12.** HDMI2.0 5.94 Gbps eye diagram with ECMF4-20A42N10. (test conditions : worst case cable and equalizer)



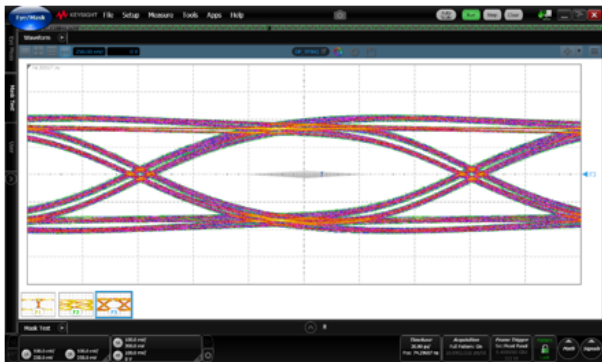
**Figure 13.** HDMI2.1 12 Gbps eye diagram without ECMF4-20A42N10. (test conditions: worst case cable, equalizer and CTLE)



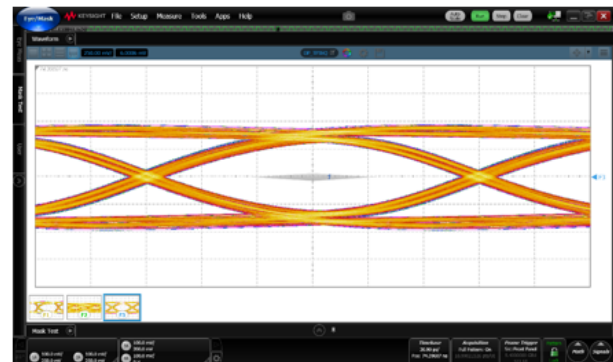
**Figure 14.** HDMI2.1 12 Gbps eye diagram with ECMF4-20A42N10. (test conditions: worst case cable, equalizer and CTLE)



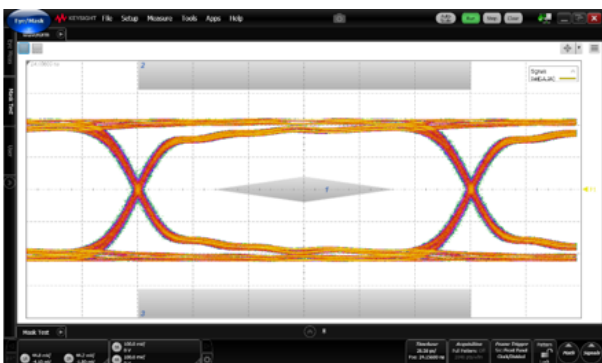
**Figure 15.** DP HBR2 5.4 Gbps eye diagram without ECMF4-20A42N10. (test conditions : with cable and equalizer)



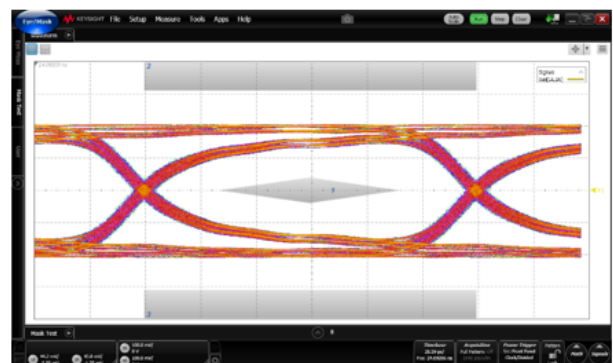
**Figure 16.** DP HBR2 5.4 Gbps eye diagram with ECMF4-20A42N10. (test conditions : with cable and equalizer)

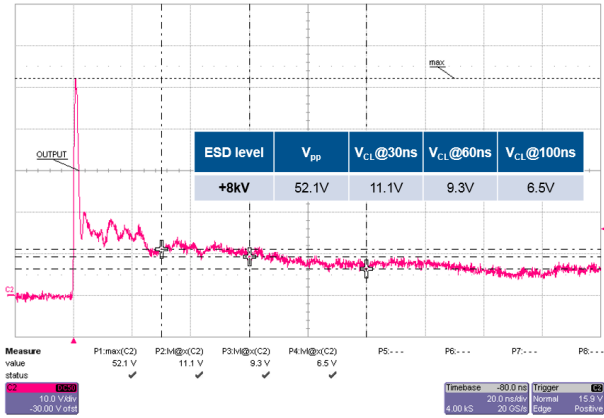
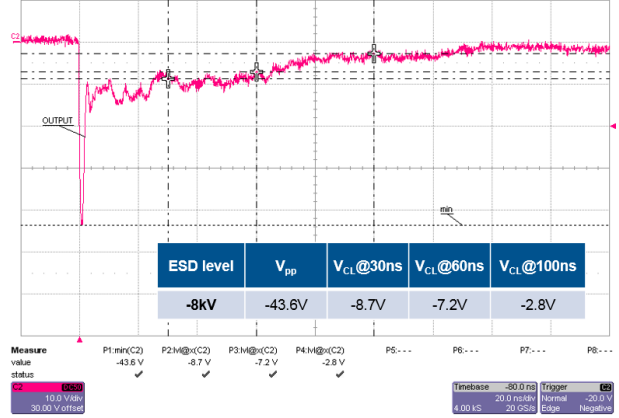
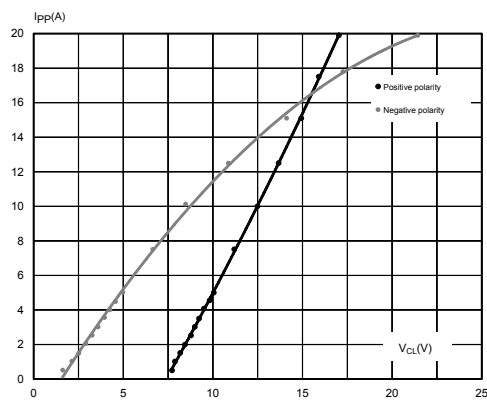


**Figure 17.** Mipi Gear3 5.83 Gbps eye diagram without ECMF4-20A42N10



**Figure 18.** Mipi Gear3 5.83 Gbps eye diagram with ECMF4-20A42N10



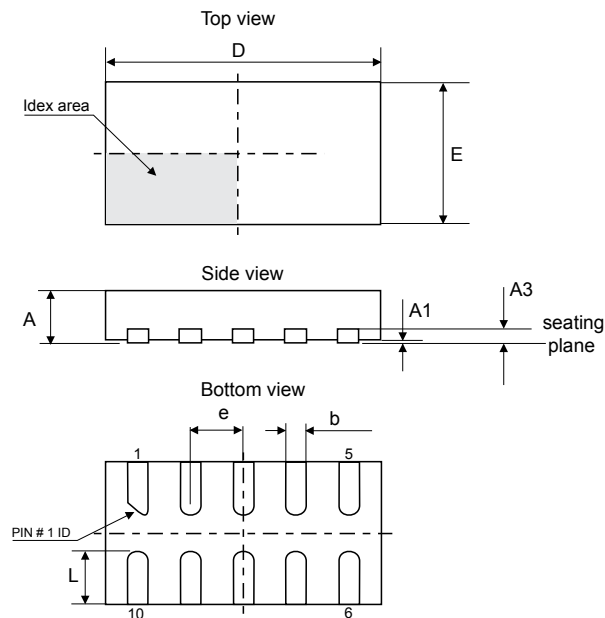
**Figure 19. ESD response to IEC61000-4-2 (+8 kV contact discharge)**

**Figure 20. ESD response to IEC61000-4-2 (-8 kV contact discharge)**

**Figure 21. TLP characteristic**


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 2.1 μQFN10L package information

**Figure 22. μQFN10L package outline**



**Table 4. μQFN10L package mechanical data**

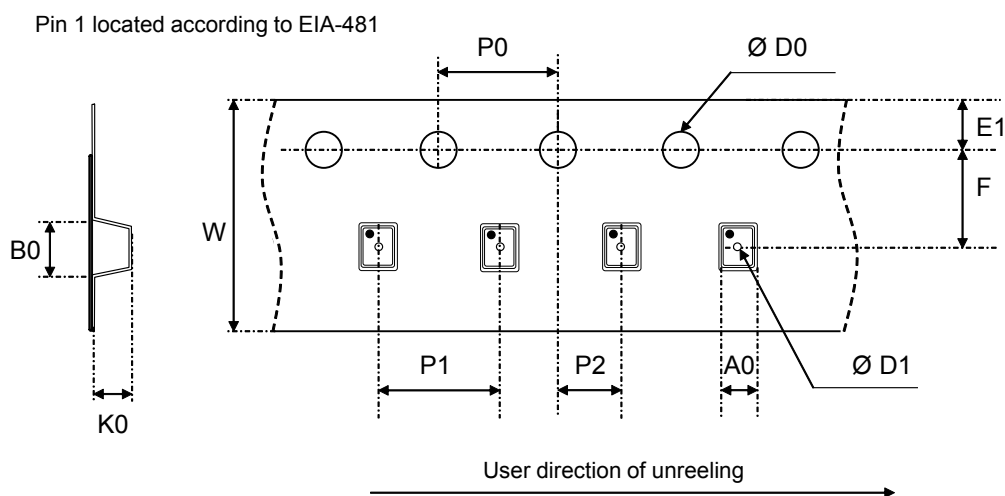
| Ref. | Dimensions  |       |      |
|------|-------------|-------|------|
|      | Millimeters |       |      |
|      | Min.        | Typ.  | Max. |
| A    | 0.41        | 0.45  | 0.50 |
| A1   | 0.00        | 0.02  | 0.05 |
| A3   |             | 0.127 |      |
| b    | 0.15        | 0.20  | 0.25 |
| D    | 2.15        | 2.20  | 2.25 |
| E    | 1.30        | 1.35  | 1.40 |
| e    |             | 0.40  |      |
| L    | 0.40        | 0.50  | 0.60 |

Figure 23. Marking layout



**Note:** The marking codes can be rotated by 90 ° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 24. Tape and reel outline



**Note:** Pocket dimensions are not on scale  
Pocket shape may vary depending on package

Table 5. Tape and reel mechanical data

| Ref. | Dimensions (millimeters) |      |      |
|------|--------------------------|------|------|
|      | Min.                     | Typ. | Max. |
| P1   | 3.9                      | 4.0  | 4.1  |
| P0   | 3.9                      | 4.0  | 4.1  |
| Ø D0 | 1.4                      | 1.5  | 1.6  |
| Ø D1 | 0.35                     | 0.40 | 0.45 |
| F    | 3.45                     | 3.5  | 3.55 |
| E1   | 1.65                     | 1.75 | 1.85 |

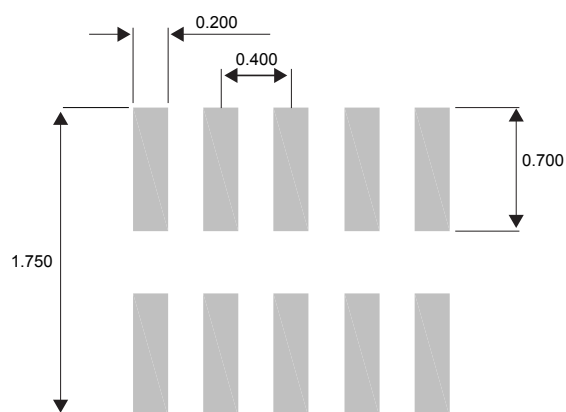


| Ref. | Dimensions (millimeters) |      |      |
|------|--------------------------|------|------|
|      | Min.                     | Typ. | Max. |
| K0   | 0.6                      | 0.65 | 0.7  |
| P2   | 1.95                     | 2    | 2.05 |
| W    | 7.9                      | 8    | 8.1  |
| A0   | 1.50                     | 1.55 | 1.60 |
| B0   | 2.35                     | 2.40 | 2.45 |

### 3 Recommendation on PCB assembly

#### 3.1 Footprint

**Figure 25. Footprint in mm**

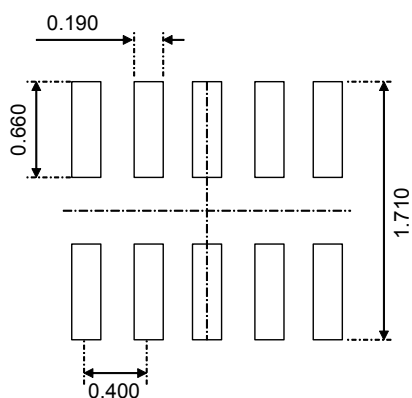


SMD footprint design is recommended.

#### 3.2 Stencil opening design

Recommended design reference: stencil opening thickness: 100  $\mu\text{m}$

**Figure 26. Stencil opening recommendations**



### 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during PCB movement.
4. Solder paste with fine particles: powder particle size is 20-38  $\mu\text{m}$ .

### 3.4 Placement

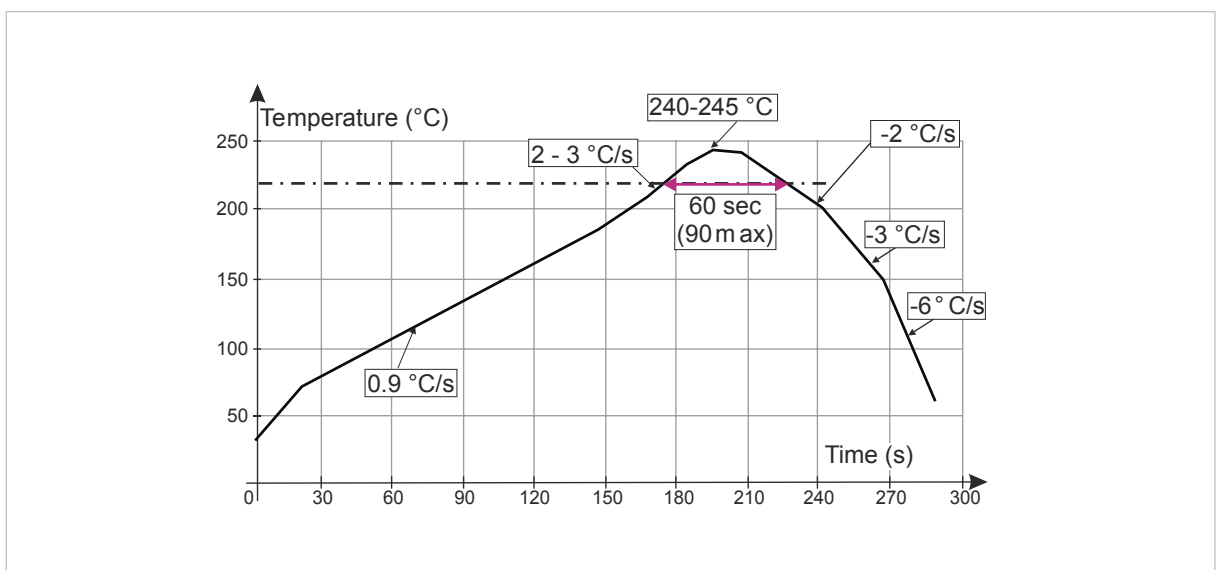
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.6 Reflow profile

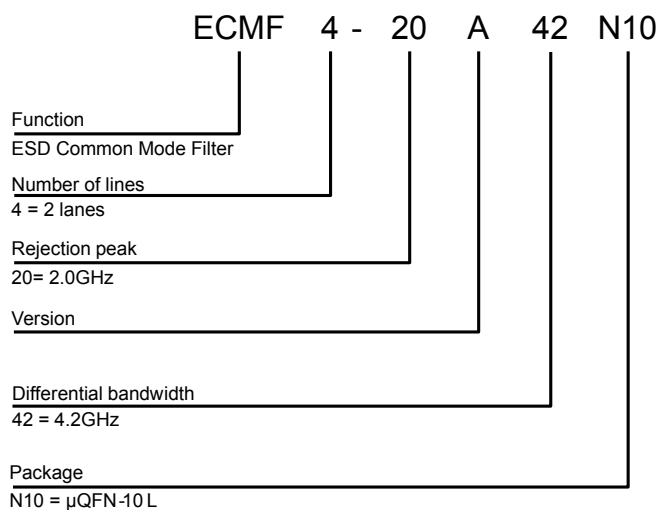
**Figure 27. ST ECOPACK® recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

## 4 ECMF4-20A42N10 Ordering information

**Figure 28. Ordering information scheme**



**Table 6. Ordering information**

| Order code     | Marking           | Package  | Weight | Base qty. | Delivery mode |
|----------------|-------------------|----------|--------|-----------|---------------|
| ECMF4-20A42N10 | MF <sup>(1)</sup> | μQFN-10L | 3.9 mg | 3000      | Tape and reel |

1. The marking can be rotated by 90° to differentiate assembly location

## Revision history

**Table 7. Document revision history**

| Date        | Revision | Changes  |
|-------------|----------|--|
| 16-May-2016 | 1        | Initial release.   |
| 12-Apr-2018 | 2        | Updated Section 1.1 Characteristics (curves), Table 4. $\mu$ QFN10L package mechanical data and Table 6. Ordering information.<br>Added Table 5. Tape and reel mechanical data, Section 3.1 Footprint, Figure 7. USB3.1 Gen 2 10.0 Gbps eye diagram without ECMF4-20A42N10 (test conditions: type C connector, reference cable equalizer with $A_{DC} = 6$ dB and DFE), Figure 8. USB3.1 Gen 1 10.0 Gbps eye diagram with ECMF4-20A42N10 (test conditions: type C connector, reference cable equalizer with $A_{DC} = 6$ dB and DFE) and Section 3.2 Stencil opening design. |
| 28-May-2018 | 3        | Updated Section • Product status / summary.  |

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