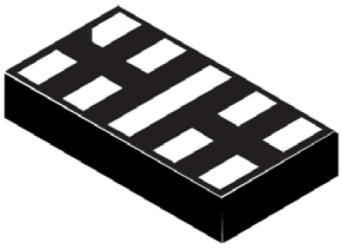
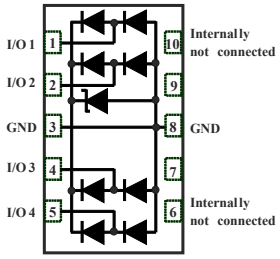
HSP054-4N10

Datasheet

4-line high speed ESD protection with ultra-low clamping voltage



µQFN 1.9x1 10L



Product status link
HSP054-4N10

Features

- Flow-through routing to keep signal integrity
- Unidirectional protection
- Ultra large bandwidth: 12 GHz (I/O2 to GND)
- Ultra-low capacitance: 0.30 pF
- Ultra-low clamping voltage: 9 V at 16 A TLP
- Extended operating junction temperature range: -40 °C to 150 °C
- RoHS compliant
- Exceeds IEC 61000-4-2 level 4:
  - ±15 kV (contact discharge)
  - ±30 kV (air discharge)

Applications

- USB 3.1 up to 10 Gbps
- USB 3.2 up to 10 Gbps
- Ethernet 1000 BASE-T
- Ethernet 10 G BASE-T
- DisplayPort
- LVDS

Description

The HSP054-4N10 is a 4 channel ESD array with a rail to rail architecture.

The HSP054-4N10 is designed to protect most sensitive, submicron technology circuits, thanks to its very low clamping voltage < 9 V under a 8 KV ESD surge.

HSP054-4N10 high protection level is achieved with no compromise on high speed lines signal integrity, thanks to ST new extra low capacitance technology.

The device is packaged in µQFN 1.9 mm x 1 mm with a 400 µm pitch.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge	 15 30	kV
I_{PP}	Peak pulse current (8/20 µs), IEC 61000-4-5		3	A
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Operating junction temperature range		-40 to +150	
T_L	Maximum lead temperature for soldering during 10 s		260	

Figure 1. Electrical characteristics - parameters definition

Symbol		Parameter
V_{RM}	=	Stand-off voltage
I_{RM}		Leakage current @ V_{RM}
V_{TRIG}	=	Trigger voltage
V_H	=	Minimum voltage when the protection is triggered
V_{CL}	=	Clamping voltage
I_{PP}	=	Peak pulse current
R_D	=	Dynamic resistance
C_{LINE}	=	Input capacitance per line

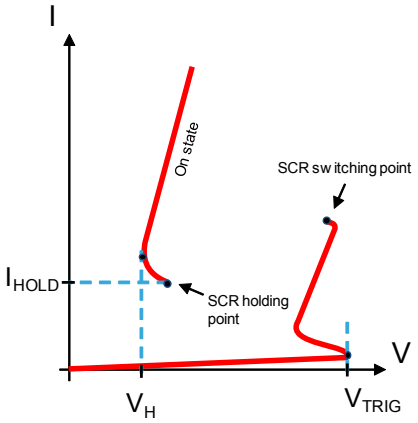


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
V_{TRIG}	Higher voltage than V_{TRIG} guarantees the protection turn-on			-	8.5	10	V
V_H	Lower voltage than VH guarantees the protection turn-off			-	1.8		V
I_{HOLD}	Lower current than IHOLD guarantees the protection turn-off			-	40		mA
V_{RM}	Reverse working voltage			-		5	V
I_{RM}	Leakage current	V_{RM} = 5 V		-	5	100	nA
V_{CL}	Clamping voltage	8 µs/20 µs wave form I_{PP} = 3 A	I/O to GND	-	3.8		V
			GND to I/O	-	4.8		
		8 kV contact discharge after 30 ns, IEC 61000-4-2	I/O to GND	-	9		
			GND to I/O	-	9		
		TLP measurement I_{PP} = 16 A	I/O to GND	-	8		
			GND to I/O	-	9		
R_d	Dynamic resistance, TLP measurement (pulse duration 100 ns)	I/O to GND		-	0.40		Ω
		GND to I/O		-	0.55		
$C_{I/O - I/O}$	Line capacitance $V_{I/O}$ = 0 V V_{OSC} = 30 mV	F = 200 MHz		-	0.25		pF
$C_{I/O - GND}$	Line capacitance $V_{I/O}$ = 0 V V_{OSC} = 30 mV	F = 200 MHz		-	0.45	0.70	
		F = 3 GHZ		-	0.30	0.45	
f_C	Differential mode cut-off frequency at - 3dB			-	10		GHz

1.1 Characteristics (curves)

Figure 2. S21 attenuation measurement

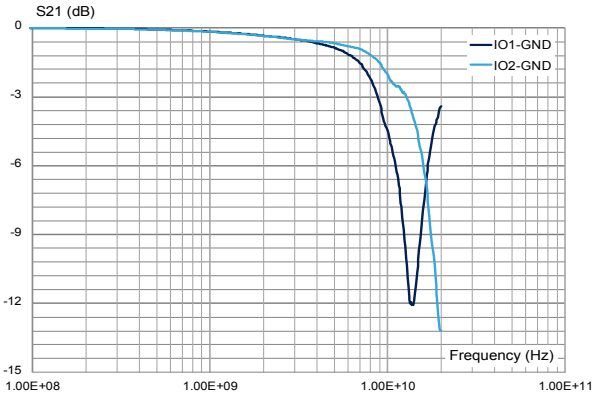


Figure 3. USB3.1 Gen 2 10.0 Gbps eye diagram without HSP054-4N10 (with type C connector, reference cable, equalizer with A_{DC} = 6 dB and DFE)

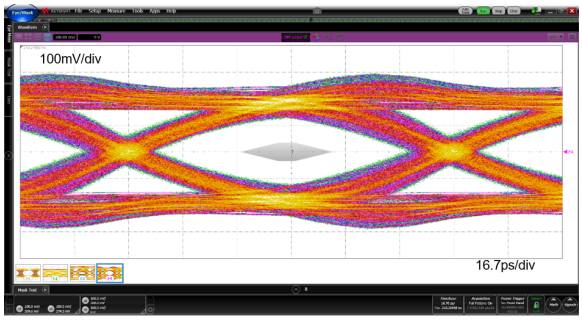


Figure 4. USB3.1 Gen 2 10.0 Gbps eye diagram with HSP054-4N10 (with type C connector, reference cable, equalizer with A_{DC} = 6 dB and DFE)

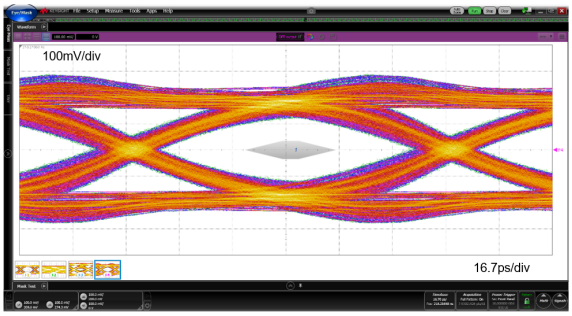


Figure 5. USB3.1 Gen 1 5.0 Gbps eye diagram without HSP054-4N10 (with type C connector, reference cable, equalizer)

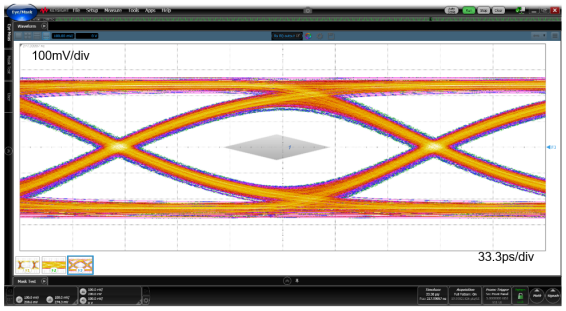


Figure 6. USB3.1 Gen 1 5.0 Gbps eye diagram with HSP054-4N10 (with type C connector, reference cable, equalizer)

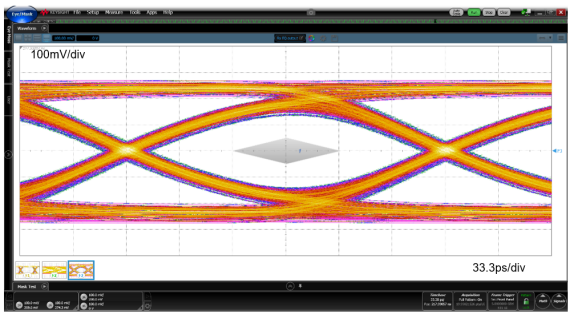


Figure 7. TLP Characteristic

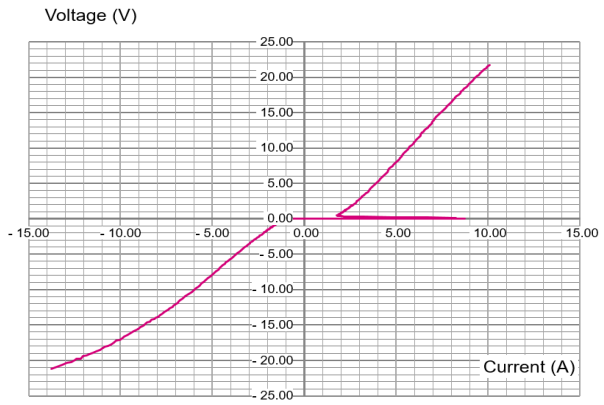


Figure 8. TDR measurement

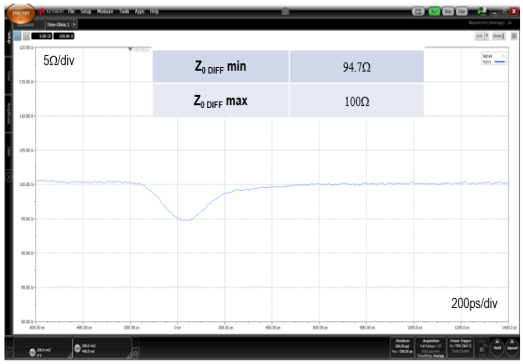


Figure 9. ESD response to IEC61000-4-2 (+8 kV contact discharge)

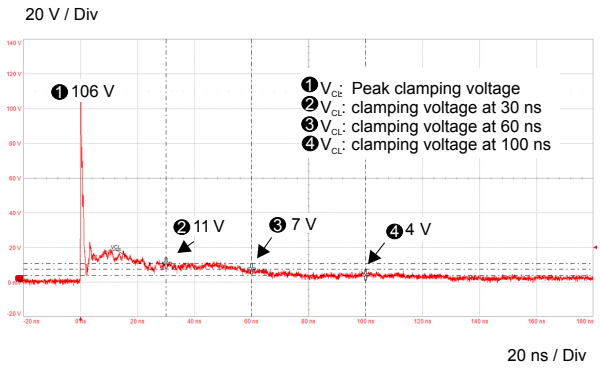
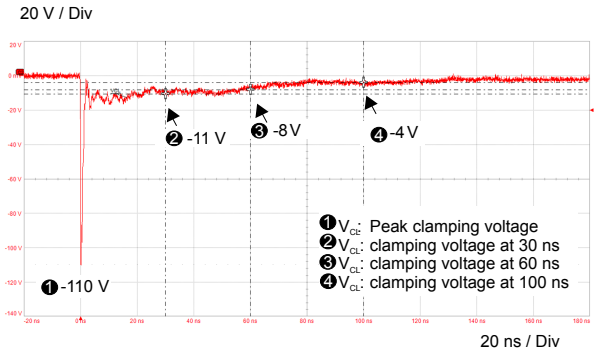


Figure 10. ESD response to IEC61000-4-2 (-8 kV contact discharge)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 µQFN1.9x1 10L package information

Figure 11. µQFN1.9x1 10L package outline

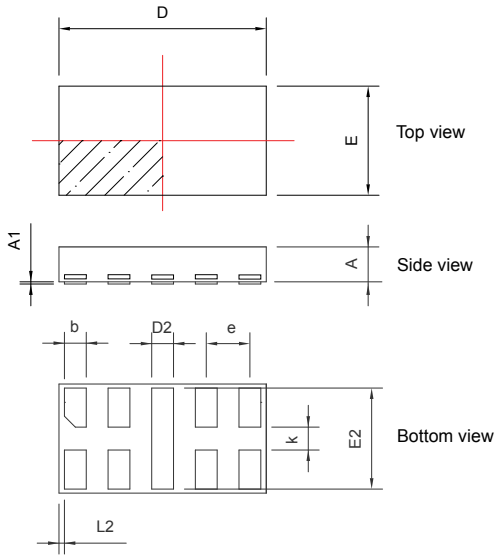


Table 3. µQFN1.9x1 10L package mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.28	0.32	0.35
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
D	1.85	1.90	1.95
D2	0.15	0.20	0.25
E	0.95	1.00	1.05
E2	0.88	0.93	0.98
e		0.40	
k		0.21	
L2	0.02	0.05	0.07

Figure 12. **Footprint (dimensions in mm)**

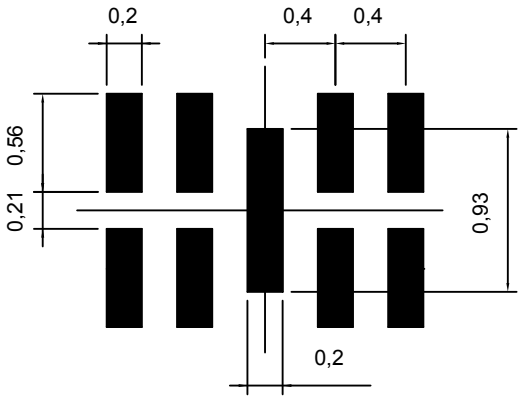
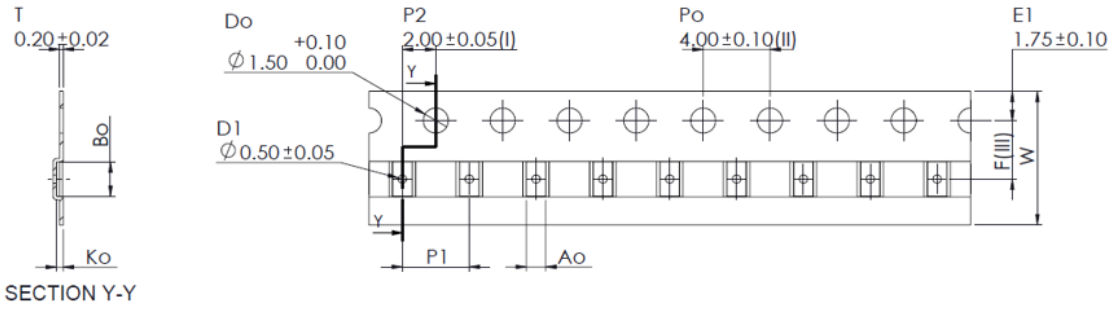


Figure 13. **µQFN1.9x1 10L tape and reel specification**



Ao	1.15 +/- 0.05
Bo	2.05 +/- 0.05
Ko	0.40 +/- 0.05
F	3.50 +/- 0.05
P1	4.00 +/- 0.10
W	8.00 +/- 0.10

3 Recommendation on PCB assembly

3.1 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-38 µm.

3.2 Placement

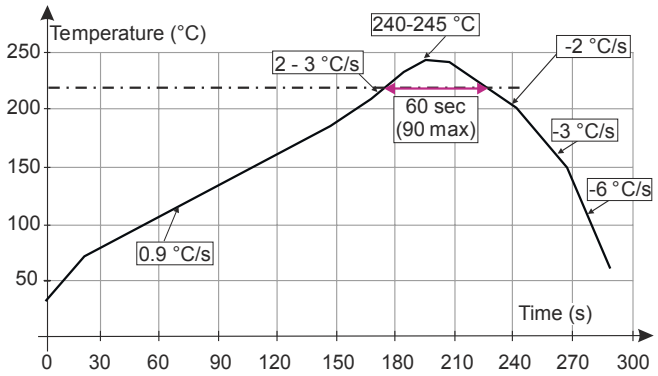
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.3 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.4 Reflow profile

Figure 14. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Note: Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HSP054-4N10	H4	µQFN-10L	1.8 mg	7000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
11-Dec-2019	1	Initial release.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

STMicroelectronics:

HSP054-4N10