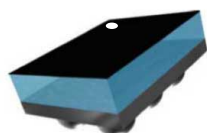
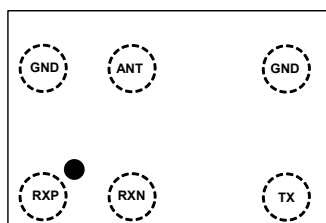


## 50 $\Omega$ nominal input / conjugate matched balun to ST S2-LP, 433 MHz with integrated harmonic filter



Flip-Chip (6 bumps) package

Pinout diagram - Top view



### Features

- 50  $\Omega$  nominal input / conjugate matched to ST S2-LP for 433 MHz frequency operation
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint
- Very low profile < 620  $\mu\text{m}$  after reflow
- High RF performance
- RF BOM and area reduction
- ECOPACK<sup>®</sup>2 compliant component

### Applications

- 433 MHz impedance matched balun filter
- Optimized for ST S2-LP sub GHz RFIC

### Description

This device is an ultra-miniature balun. The BALF-SPI2-02D3 integrates matching network and harmonics filter. Matching impedance has been customized for the ST S2-LP transceiver. The BALF-SPI2-02D3 uses STMicroelectronics IPD technology on non-conductive glass substrate which optimize RF performance.

#### Product status

BALF-SPI2-02D3

# 1 Characteristics

**Table 1. Absolute maximum ratings ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

| Symbol    | Parameter                                                                                       | Value       | Unit               |
|-----------|-------------------------------------------------------------------------------------------------|-------------|--------------------|
| $P_{IN}$  | Input power $RF_{IN}$                                                                           | 20          | dBm                |
| $V_{ESD}$ | ESD ratings human body model (JESD22-A114), all I/O one at a time while others connected to GND | 2000        | V                  |
|           | ESD ratings machine model (JESD22-A115), all I/O                                                | 200         |                    |
| $T_{OP}$  | Operating temperature                                                                           | -40 to +105 | $^{\circ}\text{C}$ |

**Table 2. Impedances ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

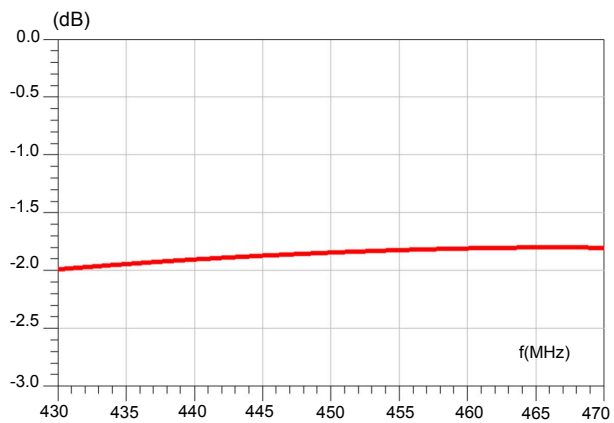
| Symbol    | Parameter                               | Value |                  |      | Unit     |
|-----------|-----------------------------------------|-------|------------------|------|----------|
|           |                                         | Min.  | Typ.             | Max. |          |
| $Z_{RX}$  | Nominal differential RX balun impedance | -     | matched ST S2-LP | -    | $\Omega$ |
| $Z_{TX}$  | Nominal TX filter impedance             |       |                  |      |          |
| $Z_{ANT}$ | Antenna impedance                       | -     | 50               | -    | $\Omega$ |

**Table 3. Electrical characteristics and RF performances ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )**

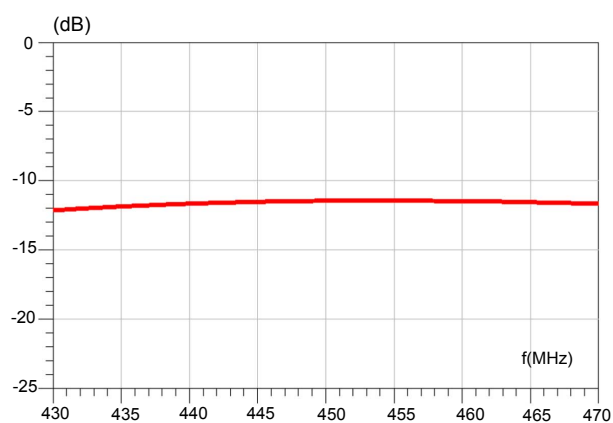
| Symbol        | Parameter                                                     | Test condition     | Value |      |      | Unit       |
|---------------|---------------------------------------------------------------|--------------------|-------|------|------|------------|
|               |                                                               |                    | Min.  | Typ. | Max. |            |
| f             | Frequency range                                               |                    |       | 433  |      | MHz        |
| $IL_{RX-ANT}$ | Insertion loss in bandwidth without mismatch loss (RX balun)  |                    |       | 1.95 | 2.20 | dB         |
| $IL_{TX-ANT}$ | Insertion loss in bandwidth without mismatch loss (TX filter) |                    |       | 3.15 | 3.60 | dB         |
| $RL_{RX-ANT}$ | Input return loss in bandwidth (RX balun)                     |                    | 11    | 12   |      | dB         |
| $RL_{TX-ANT}$ | Input return loss in bandwidth (TX filter)                    |                    | 6.5   | 8.0  |      | dB         |
| $\phi_{imb}$  | Output phase imbalance (RX balun)                             |                    | -2.1  |      | 2.1  | $^{\circ}$ |
| $A_{imb}$     | Output amplitude imbalance (RX balun)                         |                    | -1.1  |      | 1.1  | dB         |
| Att           | Harmonic levels (TX filter)                                   | Attenuation at 2fo | 52    | 58   |      | dB         |
|               |                                                               | Attenuation at 3fo | 53    | 63   |      |            |
|               |                                                               | Attenuation at 4fo | 54    | 55   |      |            |
|               |                                                               | Attenuation at 5fo | 54    | 55   |      |            |
|               |                                                               | Attenuation at 6fo | 55    | 56   |      |            |
|               |                                                               | Attenuation at 7fo | 56    | 57   |      |            |

## 1.1 RF measurements (Rx balun)

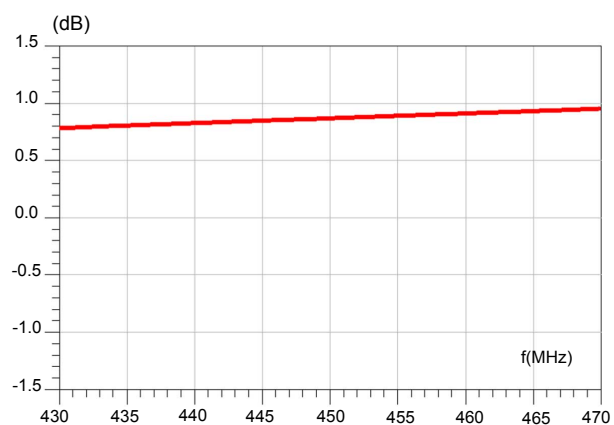
**Figure 1. Insertion loss**



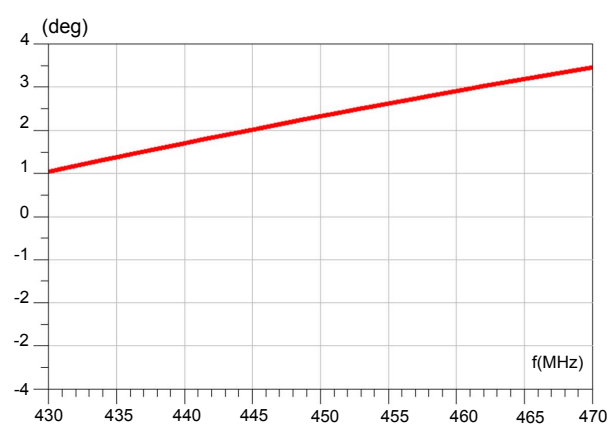
**Figure 2. Return loss on antenna**



**Figure 3. Amplitude imbalance**

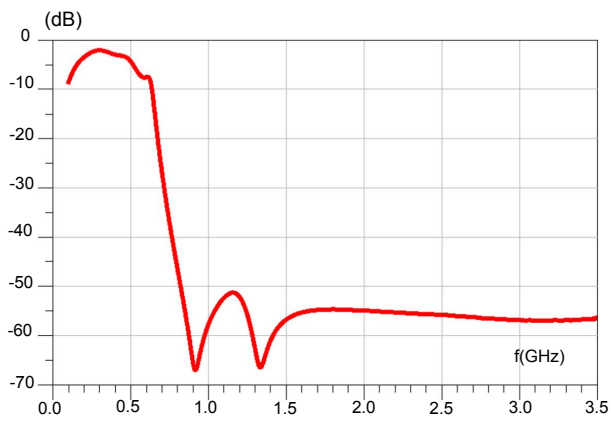


**Figure 4. Phase imbalance**

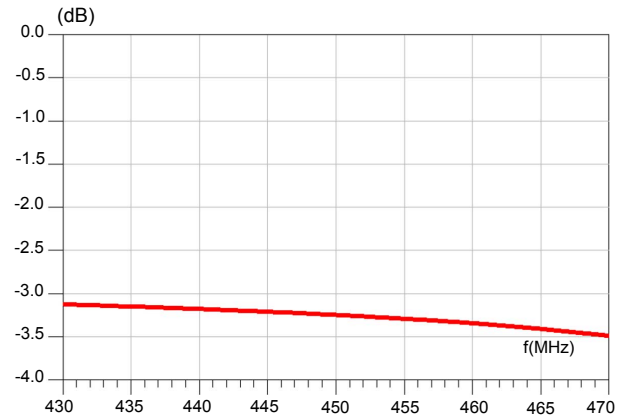


## 1.2 RF measurements (Tx filter)

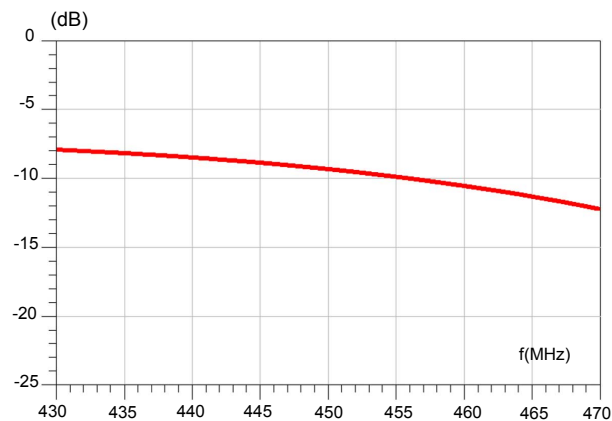
**Figure 5. Transmission**



**Figure 6. Insertion loss**

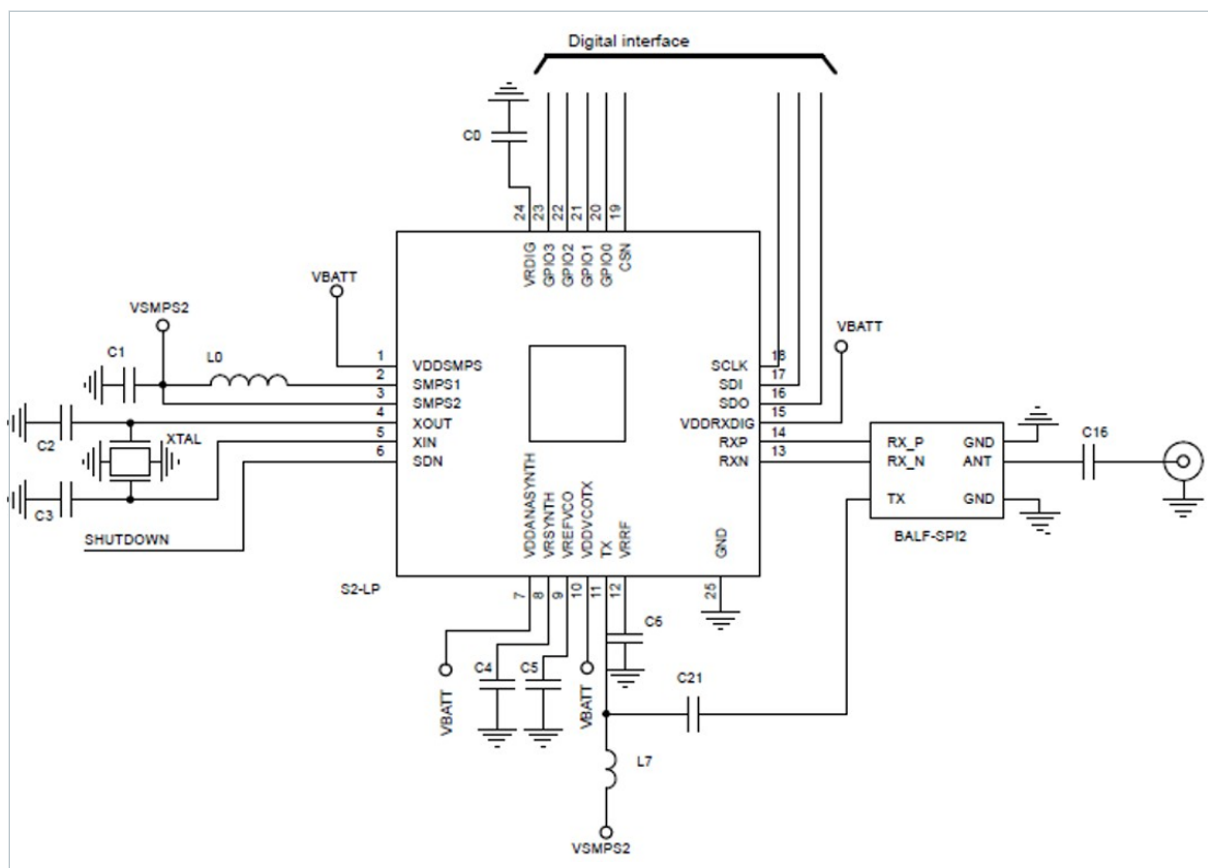


**Figure 7. Return loss on antenna**



### 1.3 ST S2-LP application diagram example

Figure 8. ST S2-LP application diagram example

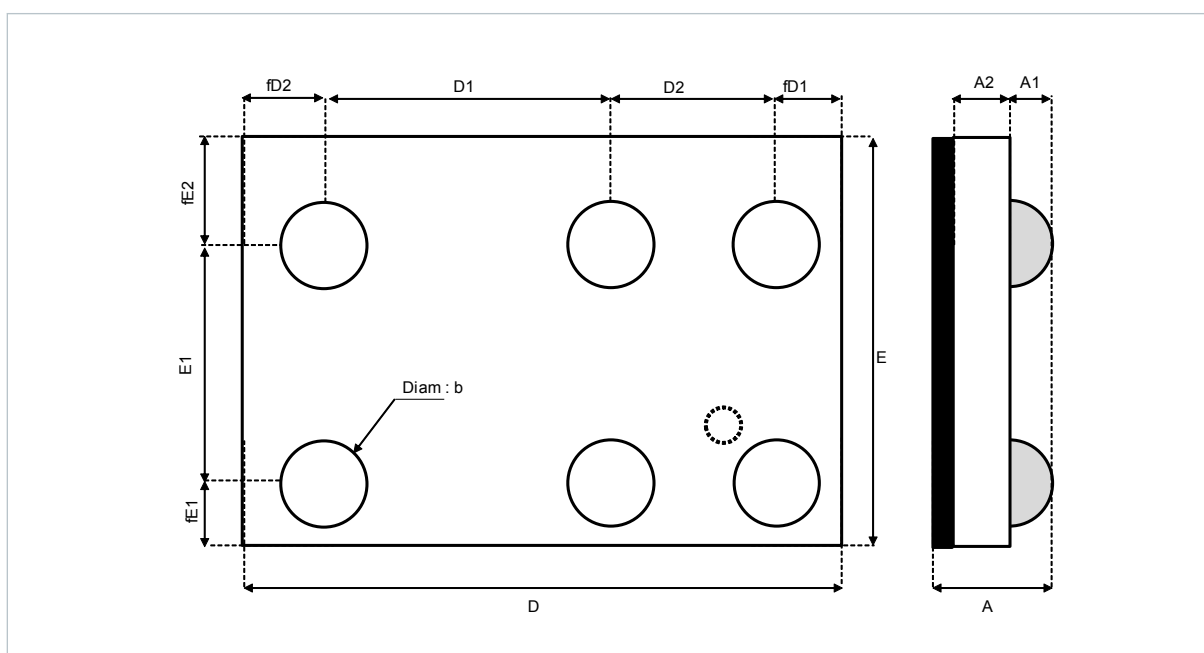


## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 2.1 Flip-Chip 6 bumps package information

**Figure 9. Flip-Chip 6 bumps package outline (bottom and side view)**

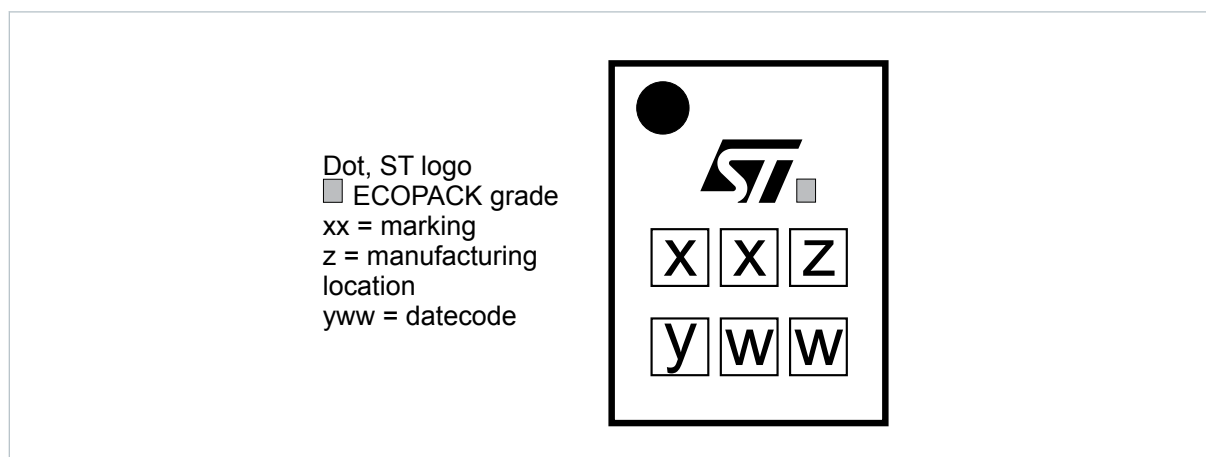


**Table 4. Flip-Chip 6 bumps dimensions (in mm)**

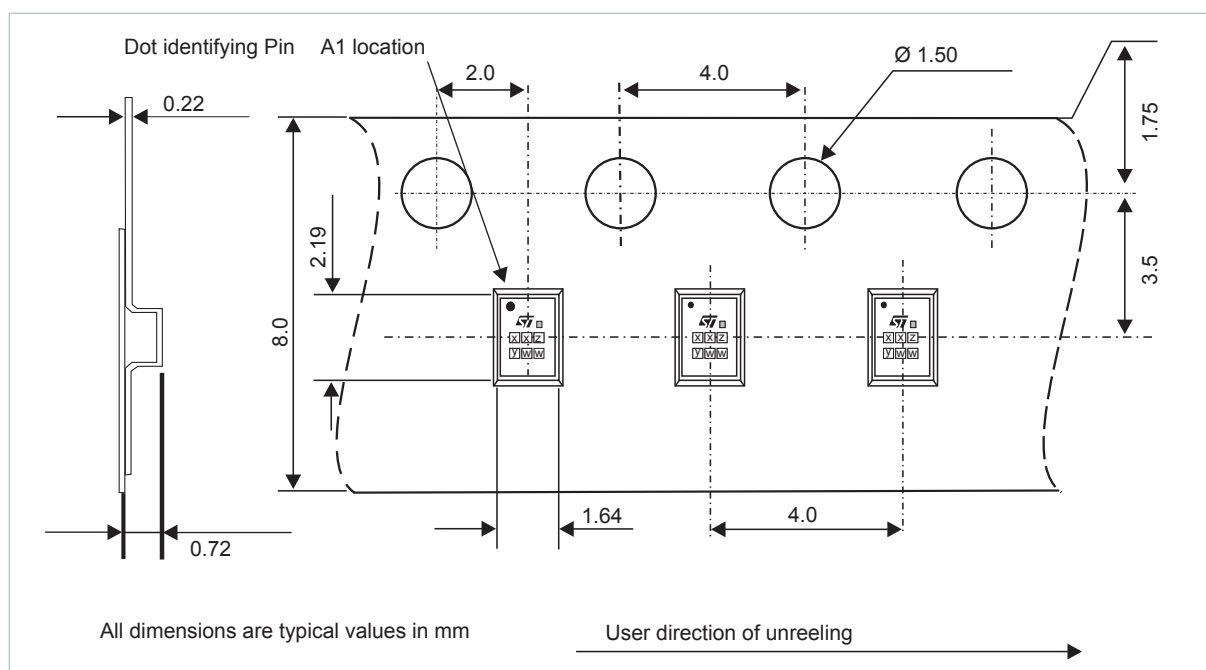
| Parameter | Min.  | Typ.  | Max.  |
|-----------|-------|-------|-------|
| A         | 0.580 | 0.630 | 0.680 |
| A1        | 0.180 | 0.205 | 0.230 |
| A2        | 0.380 | 0.400 | 0.420 |
| b         | 0.230 | 0.255 | 0.280 |
| D         | 2.050 | 2.100 | 2.150 |
| D1        |       | 1.210 |       |
| D2        |       | 0.500 |       |
| E         | 1.500 | 1.550 | 1.600 |
| E1        |       | 1.060 |       |
| fD1       |       | 0.195 |       |
| fD2       |       | 0.195 |       |
| fE1       |       | 0.195 |       |
| fE2       |       | 0.295 |       |

## 2.2 Flip-chip 6 bumps packing information

### Figure 10. Marking



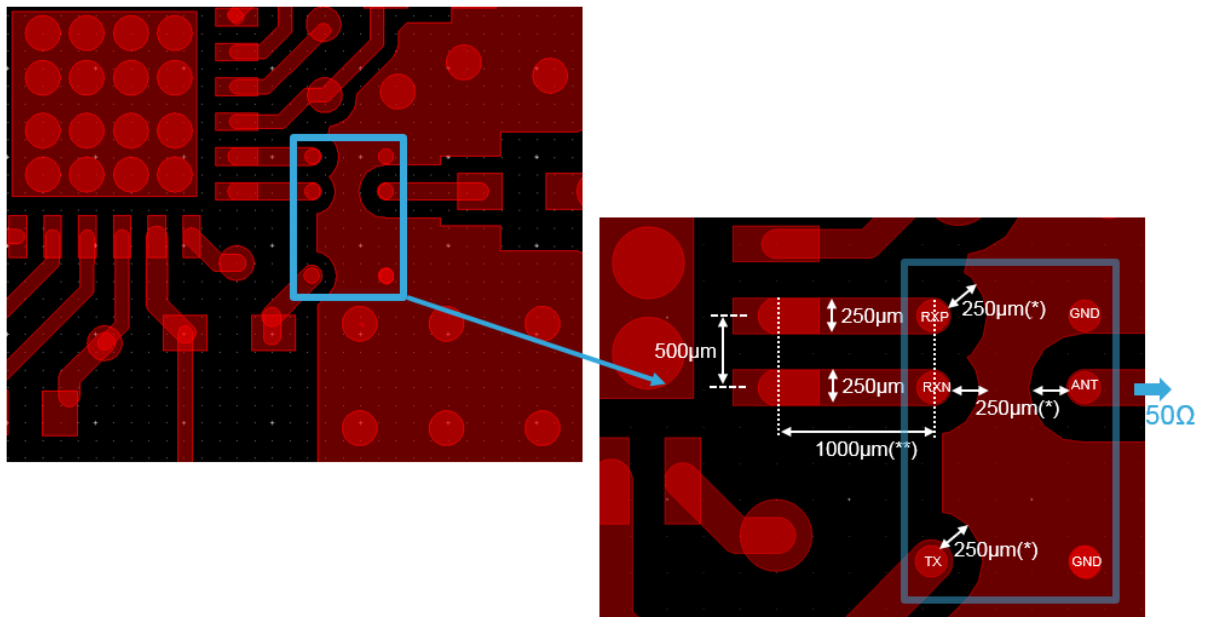
### Figure 11. Flip Chip tape and reel specifications



### 3 PCB assembly recommendations

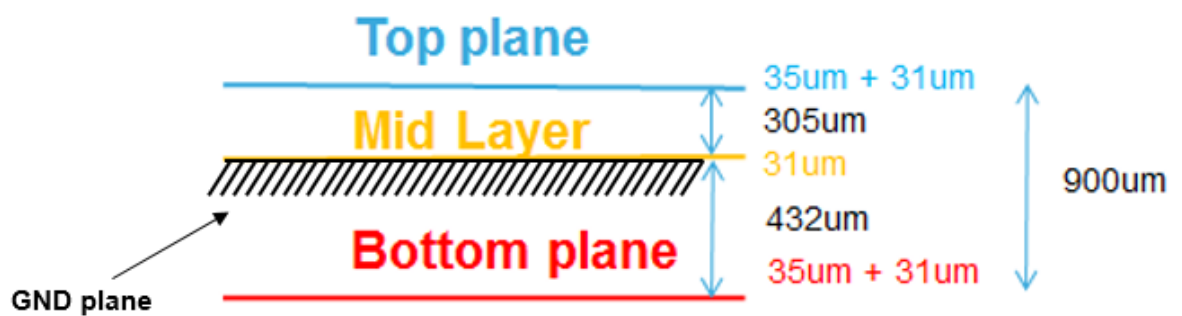
#### 3.1 Land pattern

Figure 12. Recommended balun land pattern



Note: (\*) Clearance 250 µm is needed to ensure good sensitivity.  
(\*\*) 1000 µm length between S2-LP & balun (between center QFN pads to center IPD pads).

Figure 13. PCB stack-up recommendations





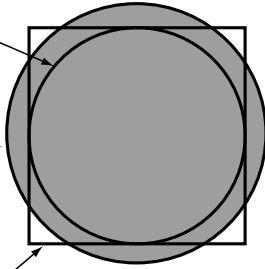
## 3.2 Stencil opening design

**Figure 14. Footprint - 3 mils stencil -non solder mask defined**

Copper pad diameter:  
 220  $\mu\text{m}$  recommended  
 180  $\mu\text{m}$  minimum  
 260  $\mu\text{m}$  maximum

Solder mask opening:  
 320  $\mu\text{m}$  recommended  
 300  $\mu\text{m}$  minimum  
 340  $\mu\text{m}$  maximum

Solder stencil opening:  
 220  $\mu\text{m}$  recommended

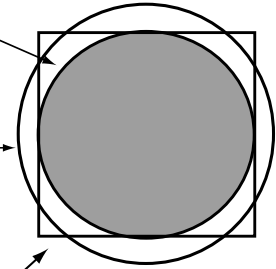


**Figure 15. Footprint - 3 mils stencil - solder mask defined**

Solder mask opening:  
 220  $\mu\text{m}$  recommended  
 180  $\mu\text{m}$  minimum  
 260  $\mu\text{m}$  maximum

Copper pad diameter:  
 320  $\mu\text{m}$  recommended  
 300  $\mu\text{m}$  minimum

Solder stencil opening:  
 220  $\mu\text{m}$  recommended



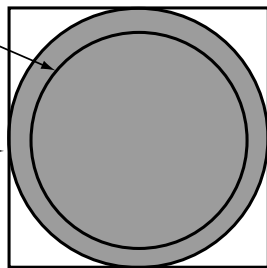
**Figure 16. Footprint - 5 mils stencil -non solder mask defined**

Copper pad diameter:  
 220  $\mu\text{m}$  recommended  
 180  $\mu\text{m}$  minimum  
 260  $\mu\text{m}$  maximum

Solder mask opening:  
 320  $\mu\text{m}$  recommended  
 300  $\mu\text{m}$  minimum  
 340  $\mu\text{m}$  maximum

Solder stencil opening:  
 330  $\mu\text{m}$  recommended\*

\*depending on paste, it can go down to 270  $\mu\text{m}$



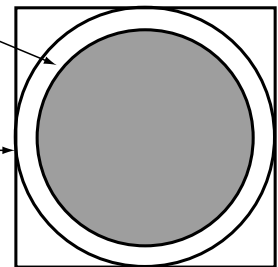
**Figure 17. Footprint - 5 mils stencil - solder mask defined**

Solder mask opening:  
 220  $\mu\text{m}$  recommended  
 180  $\mu\text{m}$  minimum  
 260  $\mu\text{m}$  maximum

Copper pad diameter:  
 320  $\mu\text{m}$  recommended  
 300  $\mu\text{m}$  minimum

Solder stencil opening:  
 330  $\mu\text{m}$  recommended\*

\*depending on paste, it can go down to 270  $\mu\text{m}$



## 3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-38  $\mu\text{m}$ .

### 3.4 Placement

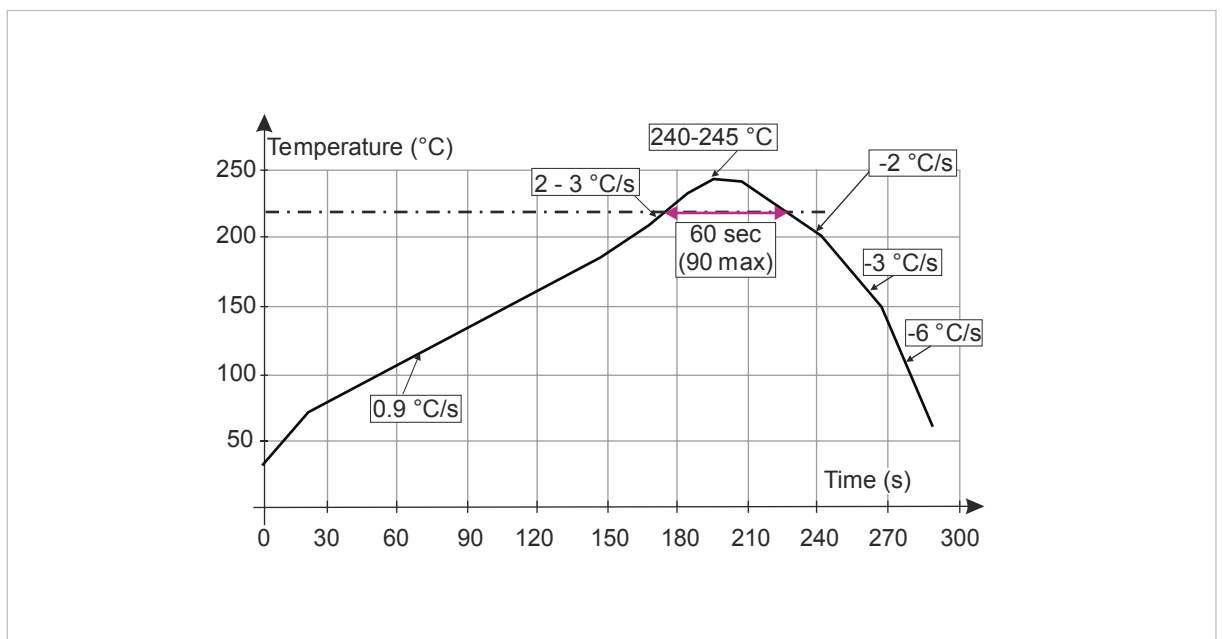
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.6 Reflow profile

**Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting**



**Note:** Minimize air convection currents in the reflow oven to avoid component movement.

**Note:** More information is available in the application note:

- AN2348 Flip-Chip: "Package description and recommendations for use"

## 4 Ordering information

**Table 5. Ordering information**

| Order code     | Marking | Package           | Weight | Base qty. | Delivery mode |
|----------------|---------|-------------------|--------|-----------|---------------|
| BALF-SPI2-02D3 | TN      | Flip-Chip 6 bumps | 3.4 mg | 5000      | Tape and reel |

## Revision history

**Table 6. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 02-May-2018 | 1        | Initial release. |

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