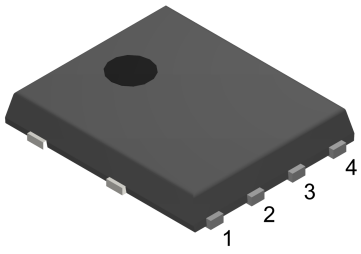
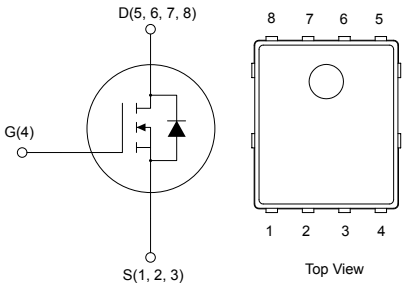
N-channel 300 V, 72 mΩ typ., 23 A MDmesh M8 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT™ 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL26N30M8	300 V	89 mΩ	23 A

- Very low $R_{DS(on)}$ x area
- Extremely low gate charge and input capacitance
- Low gate resistance (R_G)
- 100% avalanche tested
- High dv/dt ruggedness

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET belongs to the MDmesh™ M8 series, based on the new ST trench super-junction technology. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ x area, low gate charge (Q_g) and low gate resistance (R_G), making it suitable for the most demanding high efficiency converters.

Product status
STL26N30M8

Device summary	
Order code	STL26N30M8
Marking	26N30M8
Package	PawerFLAT™ 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	300	V
V_{GS}	Gate-source voltage	±25	V
I_D(1)	Drain current (continuous) at T_c = 25 °C	23	A
I_D(1)	Drain current (continuous) at T_c = 100 °C	14.7	A
I_{DM}(1)(2)	Drain current (pulsed)	69	A
I_D(3)	Drain current (continuous) at T_{pcb} = 25 °C	4.4	A
I_D(3)	Drain Current (continuous) at T_{pcb} = 100 °C	2.8	A
I_{DM} (2)(3)	Drain current (pulsed)	17.6	A
P_{TOT}(1)	Total dissipation at T_C = 25 °C	114	W
P_{TOT}(3)	Total dissipation at T_{pcb} = 25 °C	4	W
dv/dt (4)	Peak diode recovery voltage slope	15	V/ns
dv/dt(5)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *This value is rated according to $R_{thj\text{-}c}$.*
2. *Pulse width is limited by safe operating area.*
3. *This value is rated accordinf to Rthj-pcb.*
4. *I_{SD} ≤ 23 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 240 V.*
5. *V_{DS} ≤ 240 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{THJ\text{-}C}$	Thermal resistance junction-case	1.1	°C/W
$R_{THJ\text{-}pcb}$(1)	Thermal resistance junction-pcb	31.3	°C/W

1. *When mounted on FR-4 board of 1 inch², 2 oz Cu, t <10 s.*

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	580	mJ

2 Electrical characteristics

(T_C = 25 °C)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	300			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 300 V			1	µA
I_{GSS}	Gate-source leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(TH)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 11.5 A		72	89	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		1430		pF
C_{OSS}	Output capacitance			78		pF
C_{RSS}	Reverse transfer capacitance			10		pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 240 V		167		pF
$C_{o(er)}$(2)	Equivalent capacitance energy related			83		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain		1.1		Ω
Q_g	Total gate charge	V_{DS} = 240 V, I_D = 11.5 A, V_{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)		30.8		nC
Q_{gs}	Gate-source charge			7.8		nC
Q_{gd}	Gate-drain charge			14.8		nC

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Inductive load switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_d (v)	Voltage delay time	V_{DD} = 240 V, I_D = 23 A, R_G = 4.7 Ω, V_{GS} = 10 V(see Figure 17. Test circuit for inductive load switching and diode recovery times and Figure 20. Switching time waveform)		36		ns
t_r (v)	Voltage rise time			11		ns
t_f (i)	Current fall time			36		ns
t_c (off)	Crossing time			38		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				23	A
I_{SDM}(1)	Source-drain current (pulsed)				69	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 23 A			1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 23 A, di/dt = 100 A/µs		201		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see Figure 17. Test circuit for inductive load switching and diode recovery times)		2.06		µC
I_{RRM}	Reverse recovery current			20.5		A
t_{rr}	Reverse recovery time	I_{SD} = 23 A, di/dt = 100 A/µs		256		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_j = 150°C		3.1		µC
I_{RRM}	Reverse recovery current	(see Figure 17. Test circuit for inductive load switching and diode recovery times)		24		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 3. Safe operating area

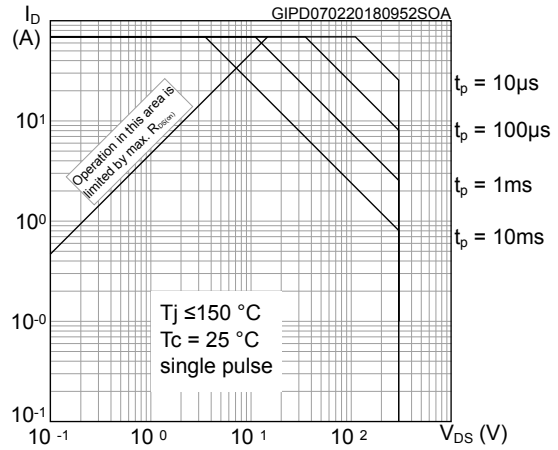


Figure 4. Thermal impedance

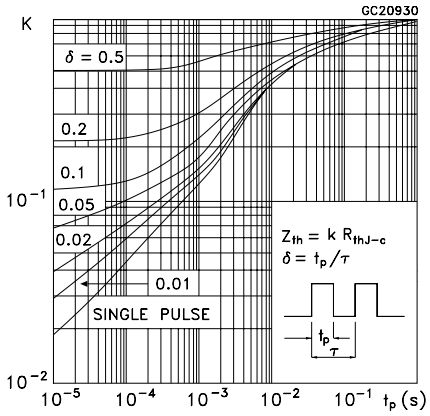


Figure 5. Output characteristics

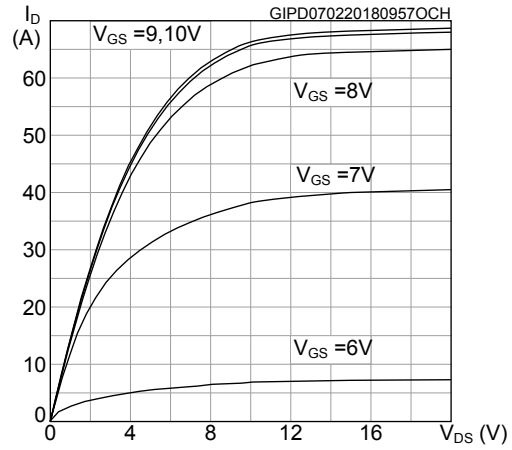


Figure 6. Transfer characteristics

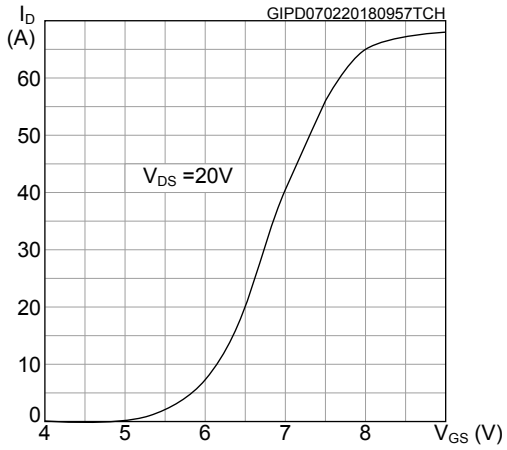


Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

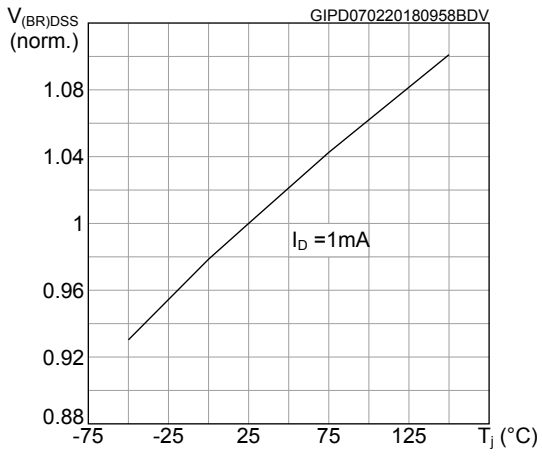


Figure 8. Static drain-source on-resistance

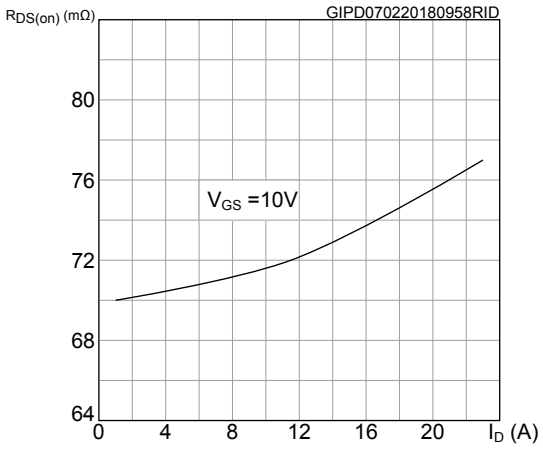


Figure 9. Gate charge vs gate-source voltage

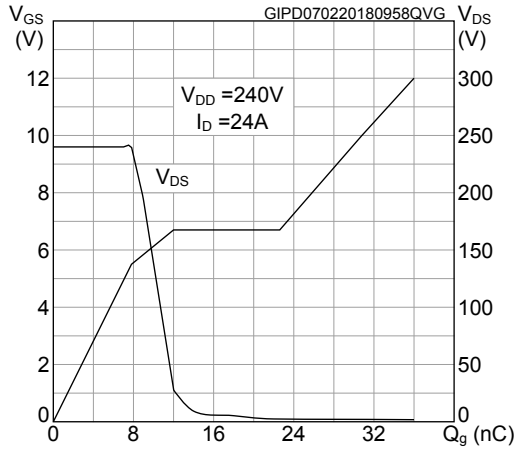


Figure 10. Capacitance variations

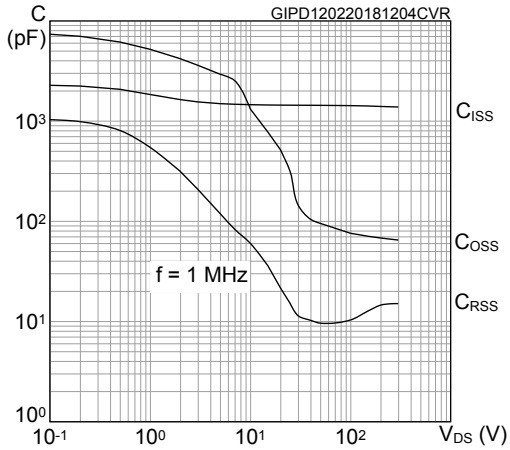


Figure 11. Normalized gate threshold voltage vs temperature

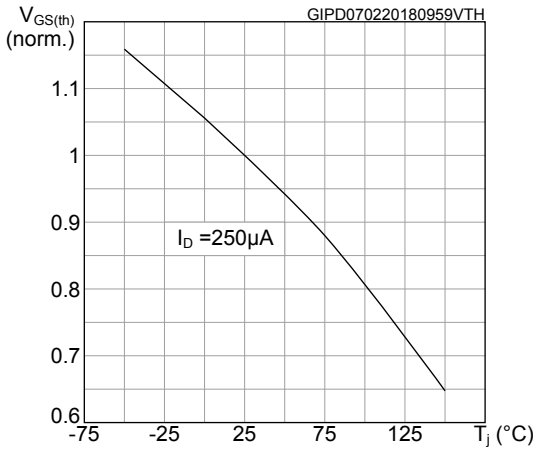


Figure 12. Normalized on-resistance vs temperature

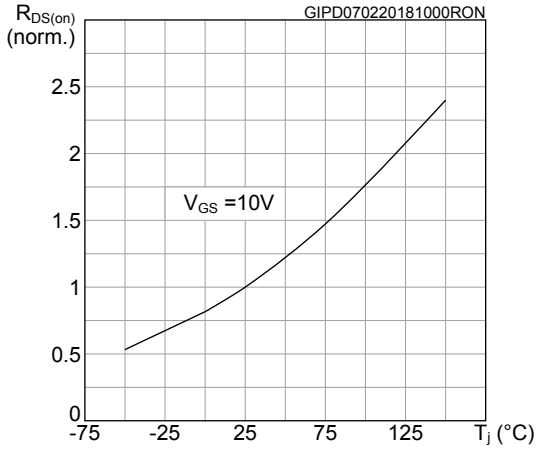


Figure 13. Output capacitance stored energy

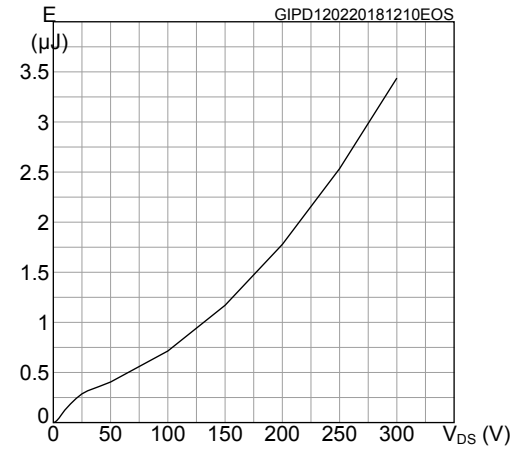
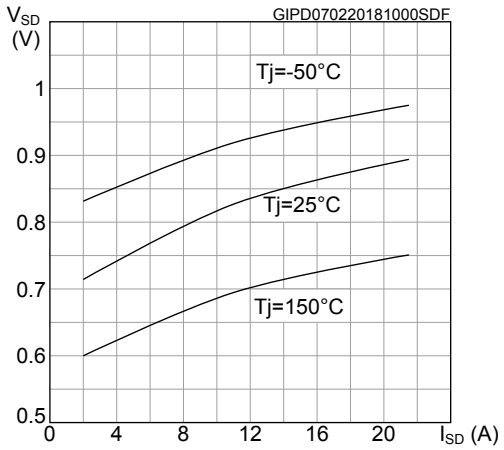


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Test circuit for resistive load switching times

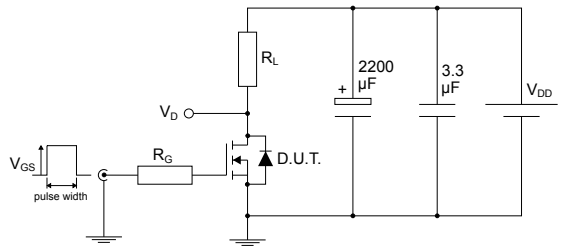


Figure 16. Test circuit for gate charge behavior

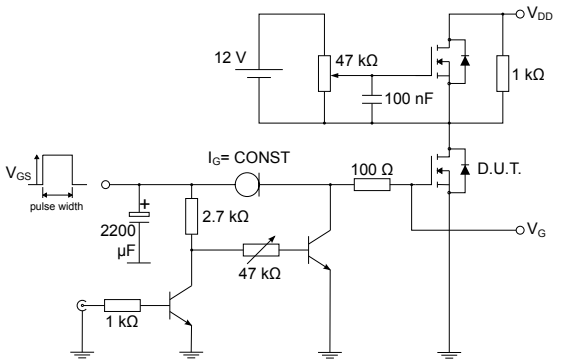


Figure 17. Test circuit for inductive load switching and diode recovery times

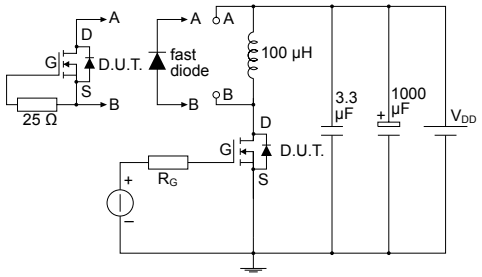


Figure 18. Unclamped inductive load test circuit

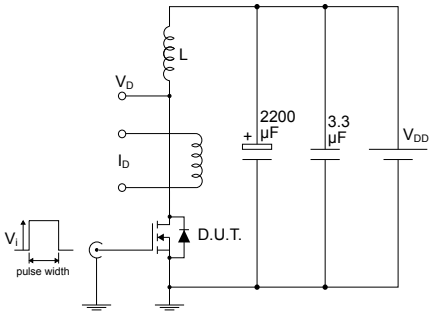


Figure 19. Unclamped inductive waveform

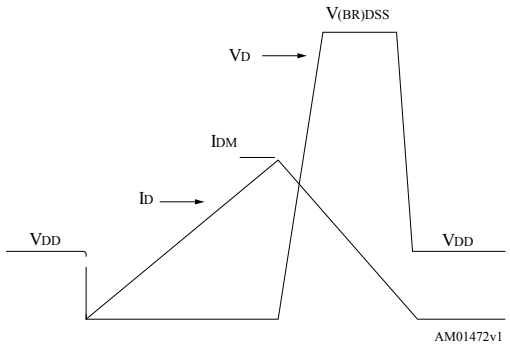
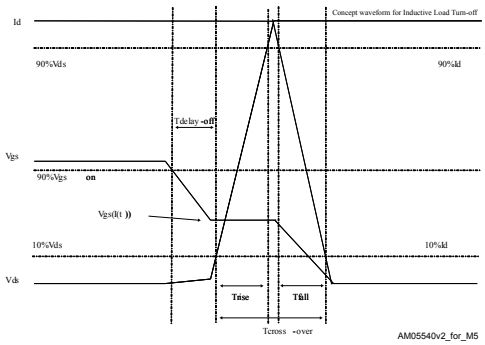


Figure 20. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 type C package information

Figure 21. PowerFLAT™ 5x6 type C package outline

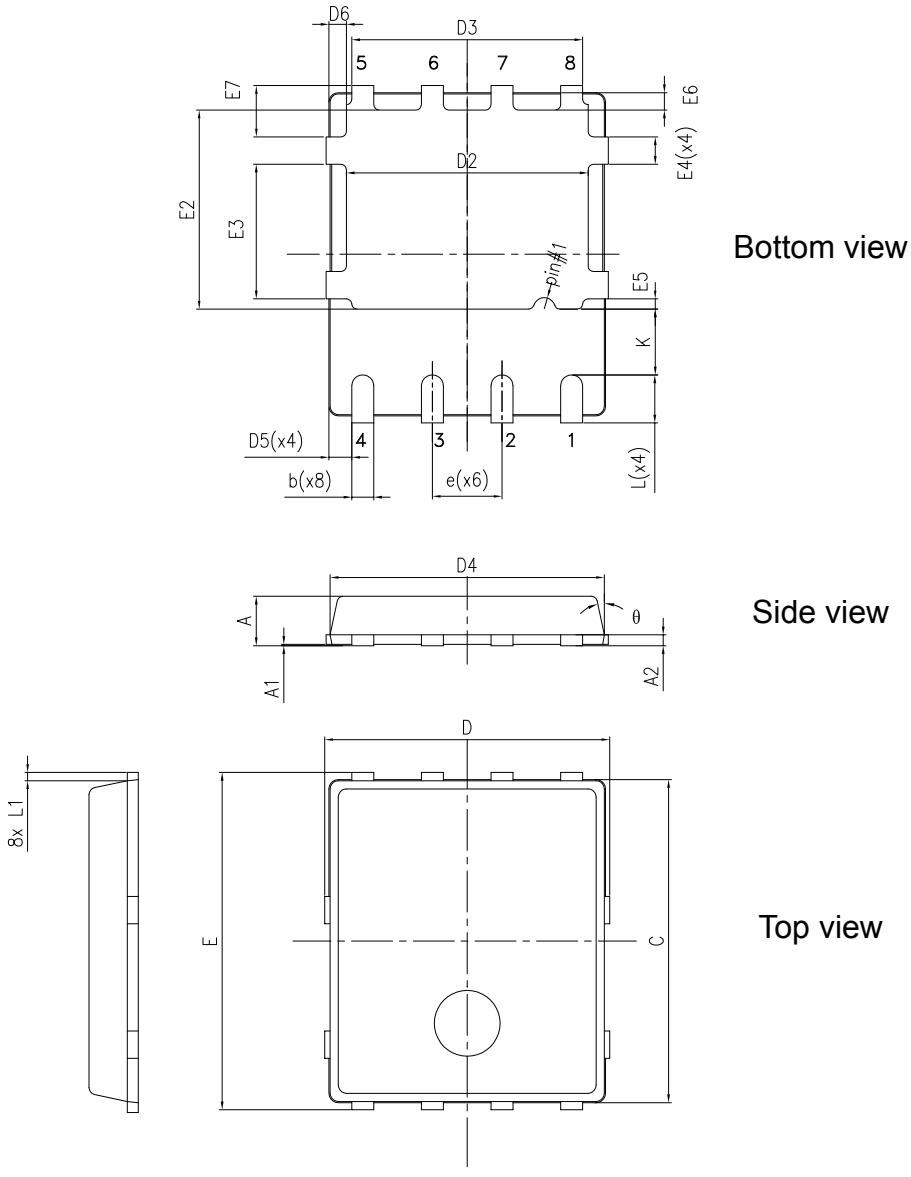
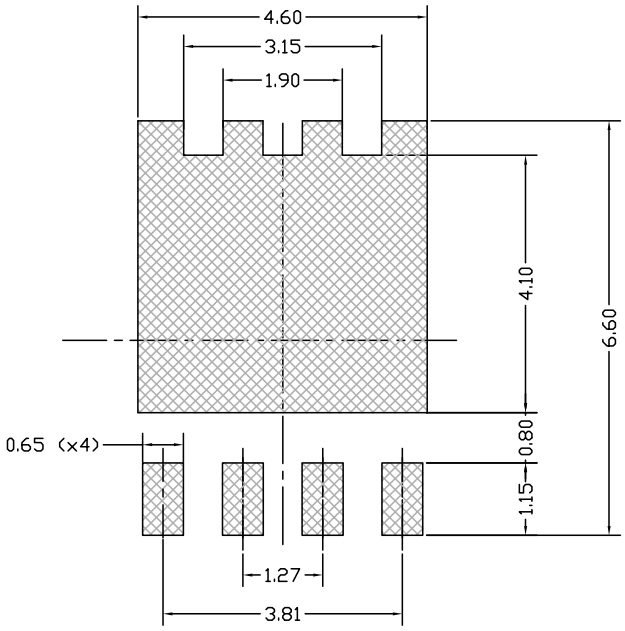


Table 8. **PowerFLAT™ 5x6 type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.05		1.35
L	0.725		1.025
L1	0.05	0.15	0.25
θ	0°		12°

Figure 22. **PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)**



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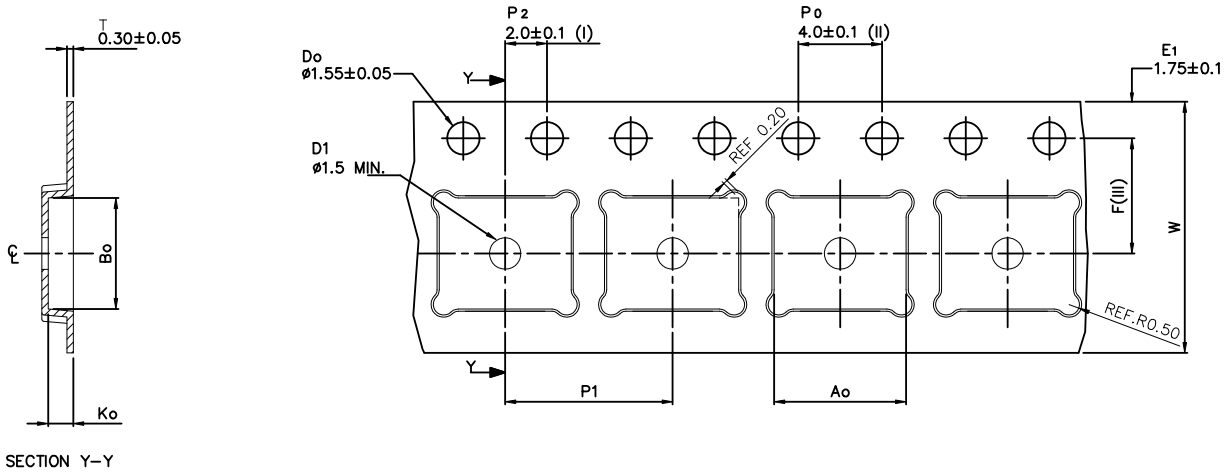
4.2 PowerFLAT™ 5x6 packing information

Figure 23. **PowerFLAT™ 5x6 tape (dimensions are in mm)**



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 24. **PowerFLAT™ 5x6 package orientation in carrier tape**

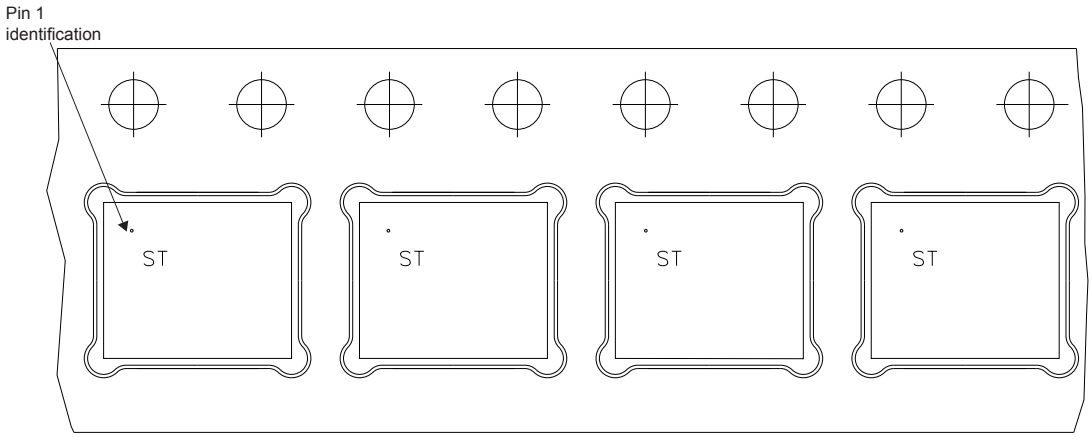
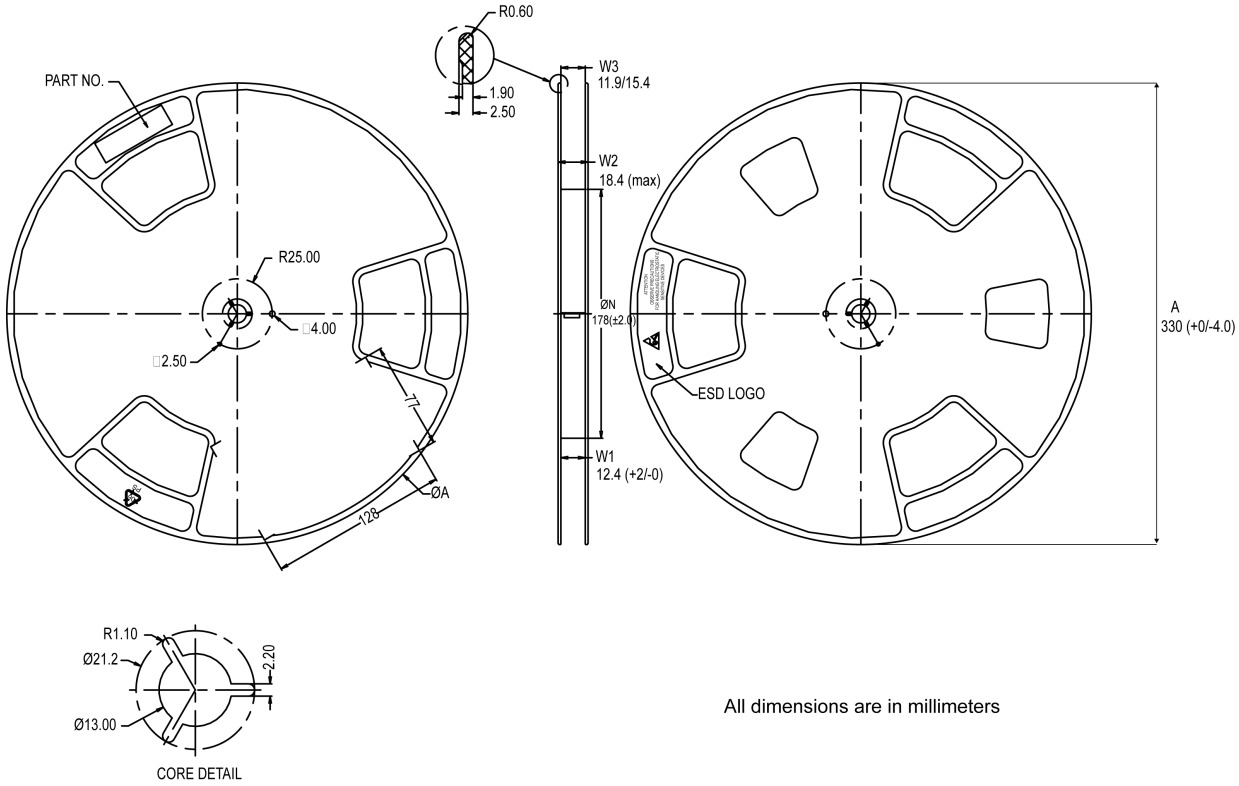


Figure 25. **PowerFLAT™ 5x6 reel**



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 9. **Document revision history**

Date	Version	Changes
07-Feb-2018	1	Initial release.

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