

Automotive-grade N-channel 55 V, 12 mΩ typ., 60 A STripFET™ II Power MOSFET in a DPAK package

Datasheet - production data

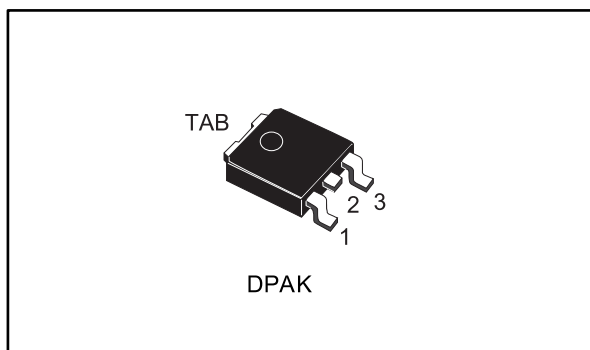
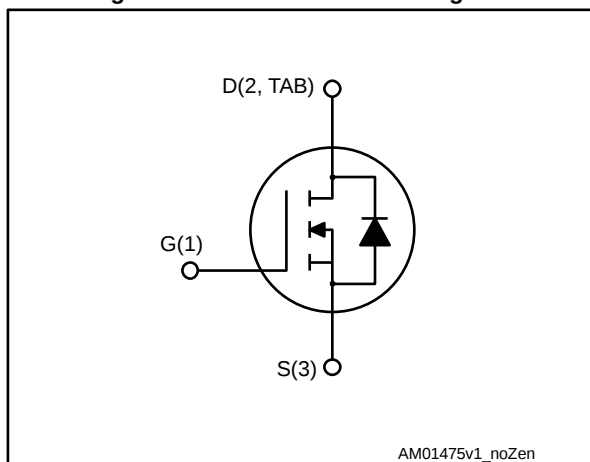


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STD60NF55LAT4	55 V	15 mΩ	60 A

- AEC-Q101 qualified
- Low threshold drive



Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STD60NF55LAT4	D60NF55LA	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate-source voltage	±15	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	60	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	42	
$I_{DM}^{(1)}$	Drain current (pulsed)	240	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	16	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	400	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾ $I_{SD} \leq 40\text{ A}$, $di/dt \leq 350\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

⁽³⁾Starting $T_J = 25\text{ °C}$, $I_D = 17.5\text{ A}$, $V_{DD} = 24\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.36	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	°C/W

Notes:

⁽¹⁾When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 250 μA	55			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 55 V			1	μA
		V _{GS} = 0 V, V _{DS} = 55 V, T _C = 125 °C ⁽¹⁾			10	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±15 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 30 A		12	15	mΩ
		V _{GS} = 5 V, I _D = 30 A		14	17	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	1950	-	pF
C _{oss}	Output capacitance			390		
C _{rss}	Reverse transfer capacitance			130		
Q _g	Total gate charge	V _{DD} = 40 V, I _D = 60 A, V _{GS} = 0 to 5 V, R _G = 4.7 Ω (see Figure 13: "Test circuit for gate charge behavior")	-	40	-	nC
Q _{gs}	Gate-source charge			10		
Q _{gd}	Gate-drain charge			20		

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 25\text{ V}$, $I_D = 30\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 12: "Test circuit for resistive load switching times" and Figure 17: "Switching time waveform")	-	30	-	ns
t_r	Rise time			180		
$t_{d(off)}$	Turn-off delay time			80		
t_f	Fall time			35		

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		60	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		240	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 60\text{ A}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14: "Test circuit for inductive load switching and diode recovery times")	-	65		ns
Q_{rr}	Reverse recovery charge		-	130		nC
I_{RRM}	Reverse recovery current		-	4		A

Notes:

⁽¹⁾Pulse width is limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

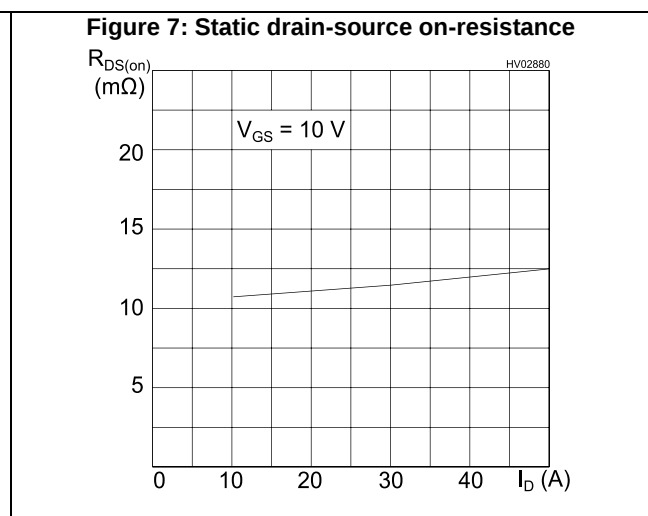
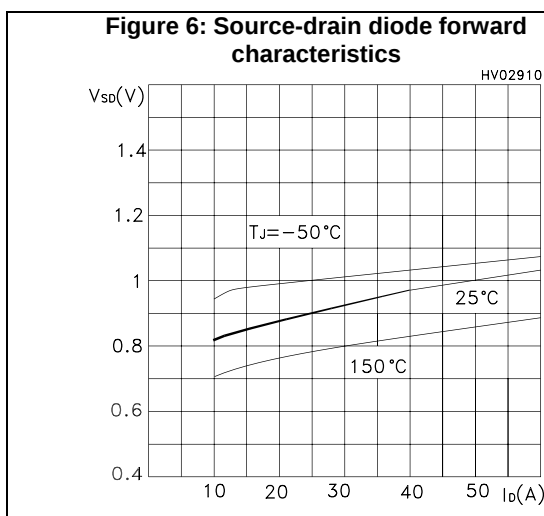
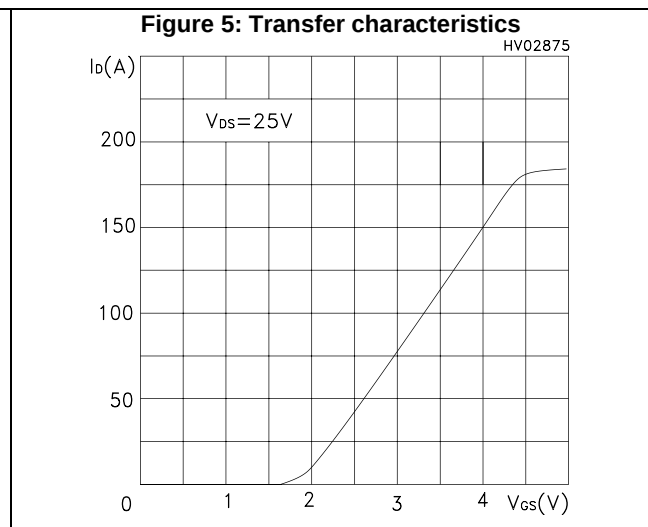
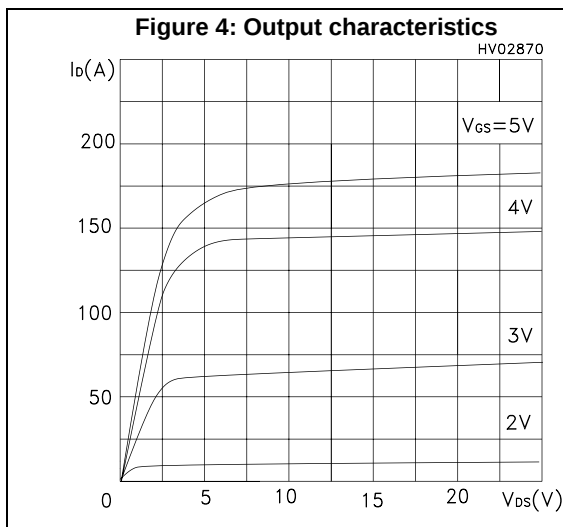
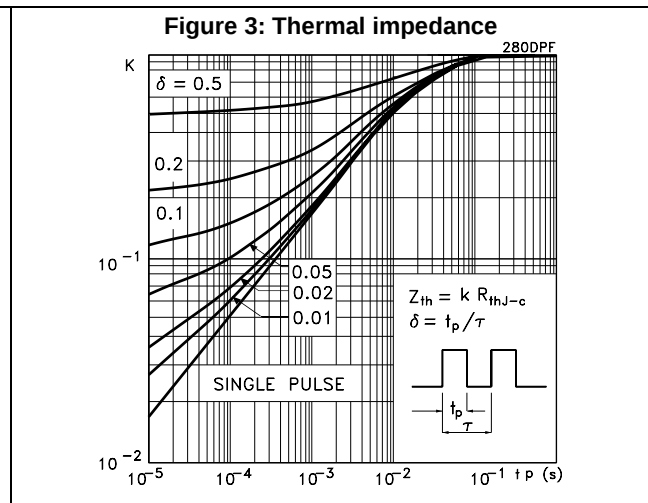
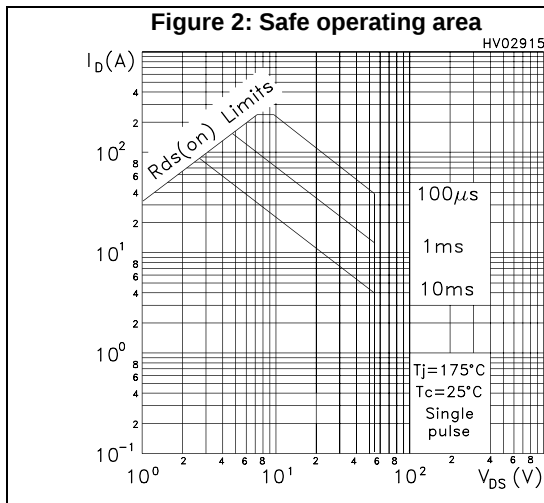


Figure 8: Gate charge vs gate-source voltage

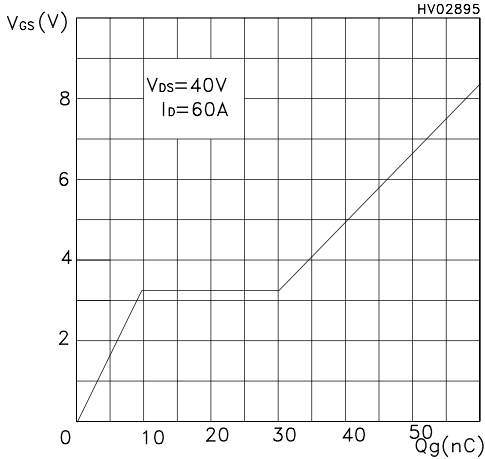


Figure 9: Capacitance variations

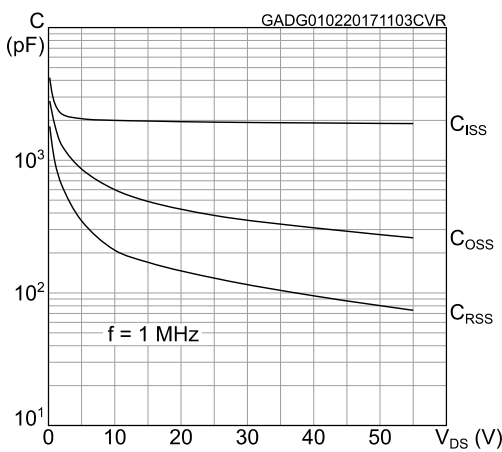


Figure 10: Normalized gate threshold voltage vs temperature

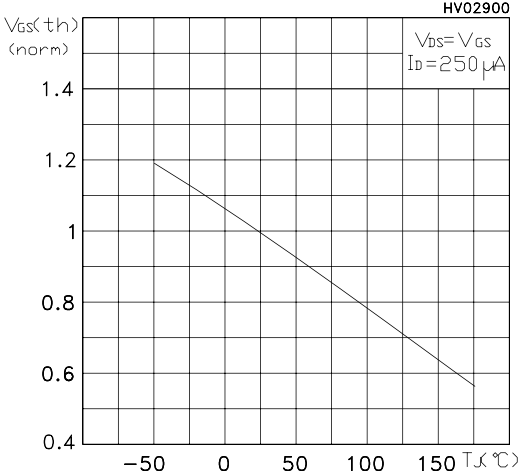
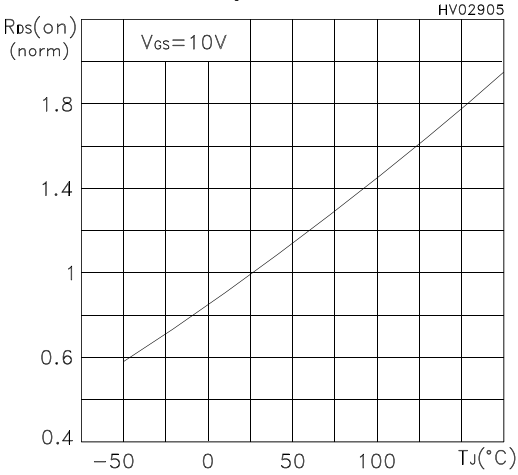


Figure 11: Normalized on-resistance vs temperature



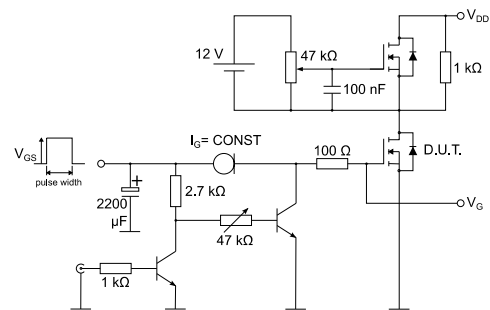
3 Test circuits

Figure 12: Test circuit for resistive load switching times



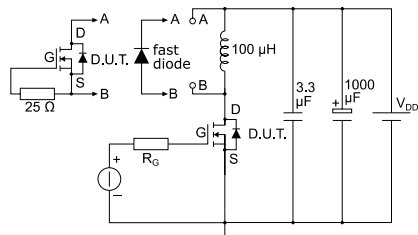
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Figure 13: Test circuit for gate charge behavior



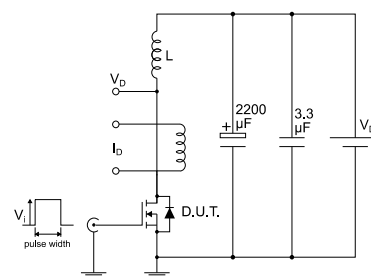
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Figure 14: Test circuit for inductive load switching and diode recovery times



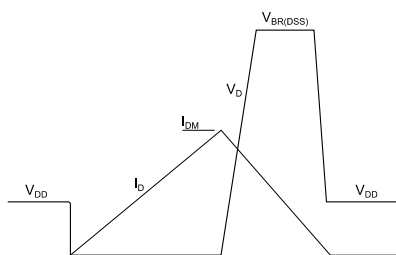
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Figure 15: Unclamped inductive load test circuit



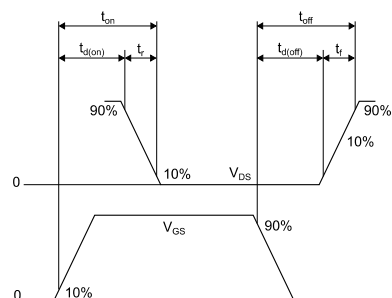
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Figure 16: Unclamped inductive waveform



AM01472v1

Figure 17: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 18: DPAK (TO-252) type A2 package outline

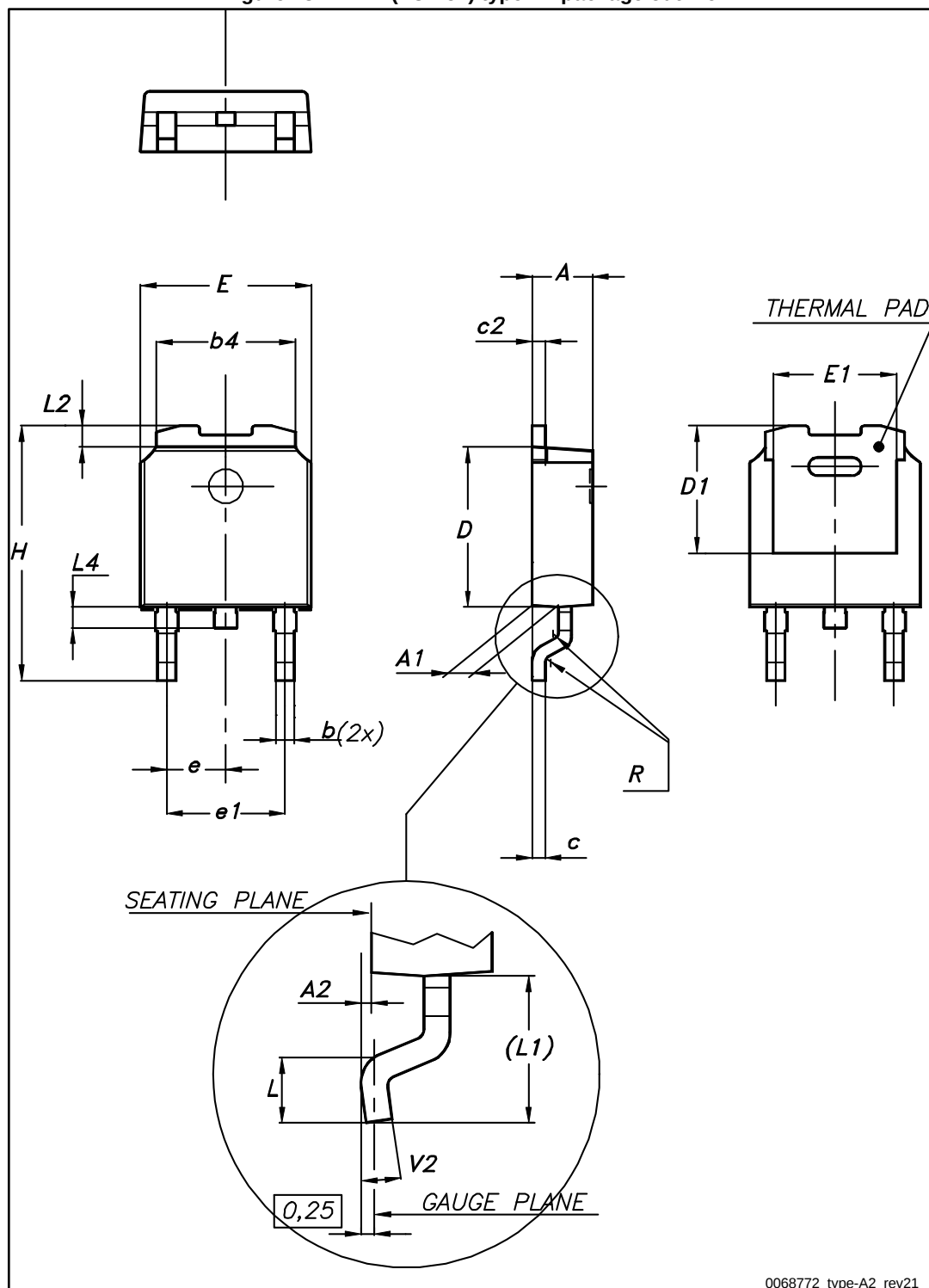
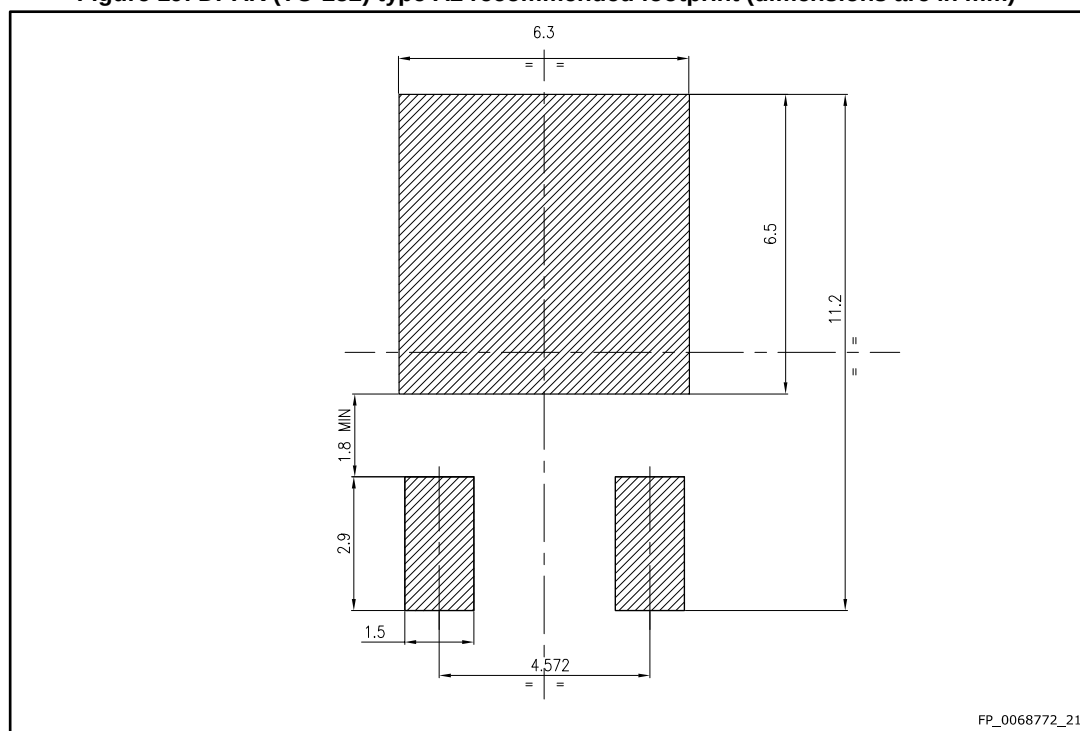


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 20: DPAK (TO-252) tape outline

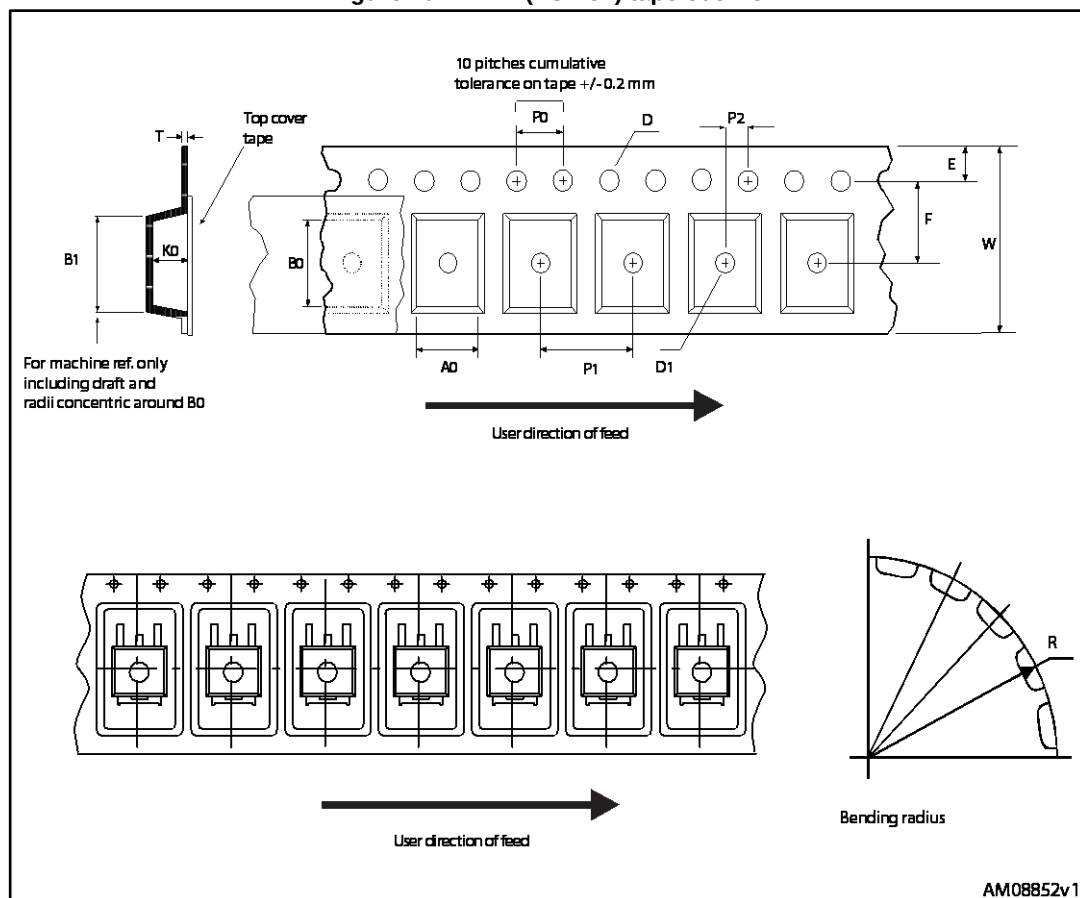


Figure 21: DPAK (TO-252) reel outline

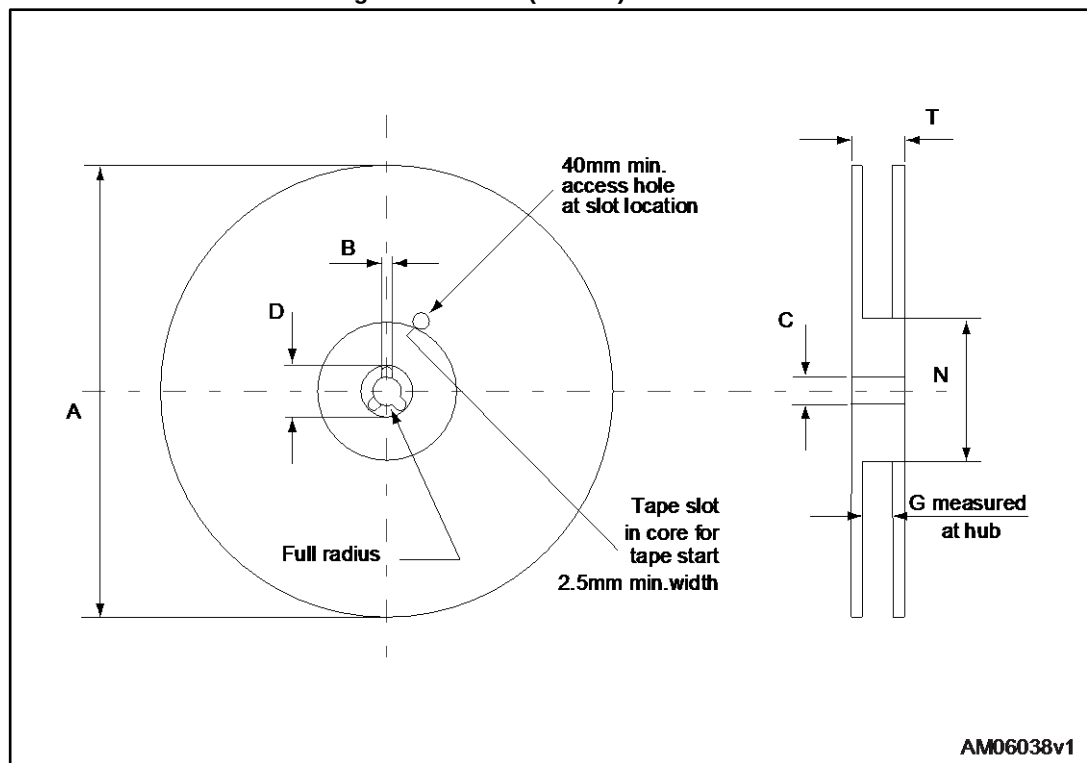


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
09-Feb-2017	1	First release

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