

N-channel 950 V, 0.110 Ω typ., 38 A MDmesh™ K5 Power MOSFET in a TO-247 long leads package

Datasheet - production data

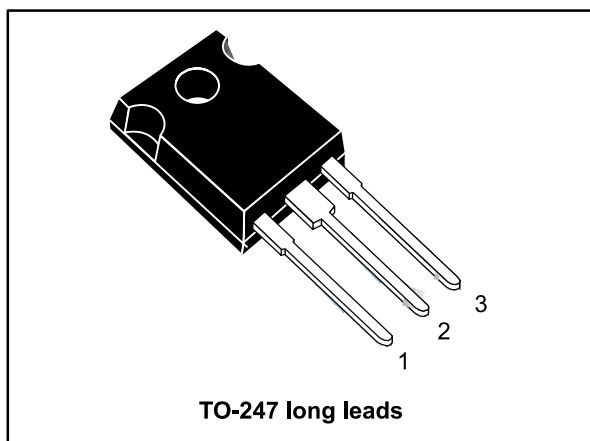
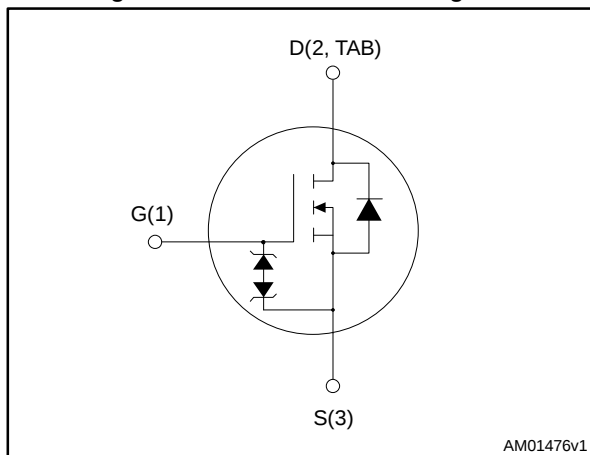


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STWA40N95K5	950 V	0.130 Ω	38 A	450 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STWA40N95K5	40N95K5	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves).....	6
3	Test circuits	9
4	Package mechanical data	10
	4.1 TO-247 long leads package information	10
5	Revision history	12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	38	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	24	A
$I_{DM}^{(1)}$	Drain current (pulsed)	152	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
I_{AR}	Max current during repetitive or single pulse avalanche	13	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 13\text{ A}$, $V_{DD} = 50\text{ V}$)	700	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 19\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(\text{peak})} \leq V_{(BR)DSS}$.

⁽³⁾ $V_{DS} \leq 760\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	0.28	$^{\circ}\text{C}/\text{W}$
$R_{thj\text{-amb}}$	Thermal resistance junction-amb max	50	$^{\circ}\text{C}/\text{W}$

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0, I_{\text{D}} = 1\text{ mA}$	950			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0, V_{\text{DS}} = 950\text{ V}$			1	μA
		$V_{\text{GS}} = 0, V_{\text{DS}} = 950\text{ V}, T_{\text{C}} = 125\text{ }^{\circ}\text{C}$			50	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0, V_{\text{GS}} = \pm 20\text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}, I_{\text{D}} = 19\text{ A}$		0.110	0.130	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{GS}} = 0, V_{\text{DS}} = 100\text{ V}, f = 1\text{ MHz}$	-	3300	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{\text{o(tr)}}^{(1)}$	Equivalent capacitance time related	$V_{\text{GS}} = 0, V_{\text{DS}} = 0\text{ to }760\text{ V}$	-	398	-	pF
$C_{\text{o(er)}}^{(2)}$	Equivalent capacitance energy related		-	142	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}, I_{\text{D}} = 0$	-	5	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 760\text{ V}, I_{\text{D}} = 38\text{ A}$	-	93	-	nC
Q_{gs}	Gate-source charge	$V_{\text{GS}} = 10\text{ V}$	-	18.7	-	nC
Q_{gd}	Gate-drain charge	(see Figure 16: "Gate charge test circuit")	-	63.4	-	nC

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 475\text{ V}, I_{\text{D}} = 19\text{ A}, R_{\text{G}} = 4.7\text{ }\Omega, V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Switching times test circuit for resistive load")	-	33.5	-	ns
t_{r}	Rise time		-	51	-	ns
$t_{\text{d(off)}}$	Turn-off-delay time		-	91.5	-	ns
t_{f}	Fall time		-	10	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18: "Unclamped inductive load test circuit")	-	706		ns
Q_{rr}	Reverse recovery charge		-	22		μC
I_{RRM}	Reverse recovery current		-	62		A
t_{rr}	Reverse recovery time	$I_{SD} = 38\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 18: "Unclamped inductive load test circuit")	-	886		ns
Q_{rr}	Reverse recovery charge		-	28.2		μC
I_{RRM}	Reverse recovery current		-	64		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

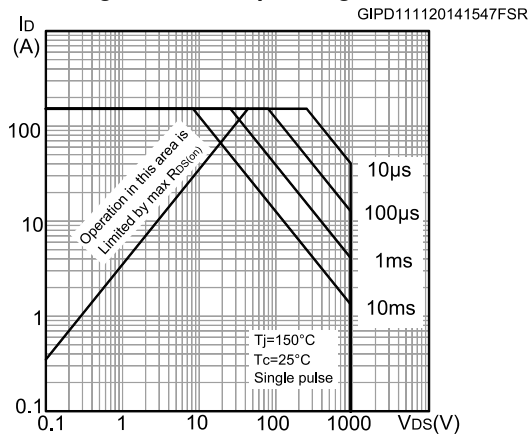


Figure 3: Thermal impedance

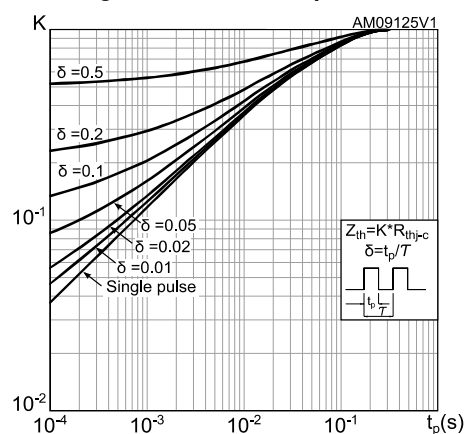


Figure 4: Output characteristics

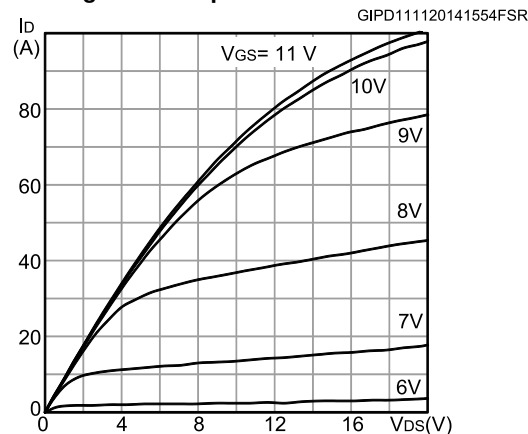


Figure 5: Transfer characteristics

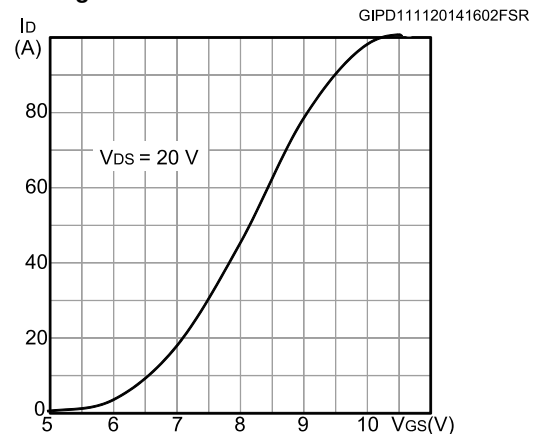


Figure 6: Gate charge vs gate-source voltage

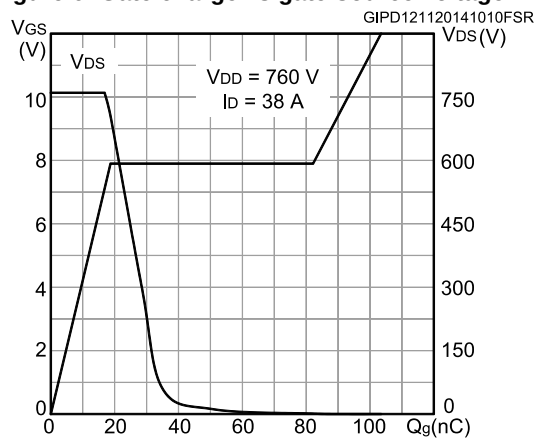


Figure 7: Static drain-source on-resistance

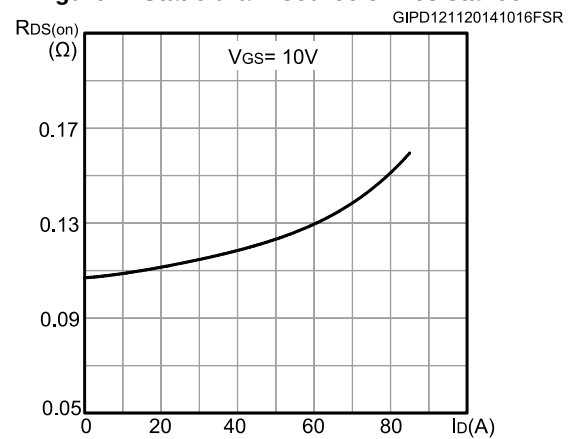


Figure 8: Capacitance variations

GIPD121120141027FSR

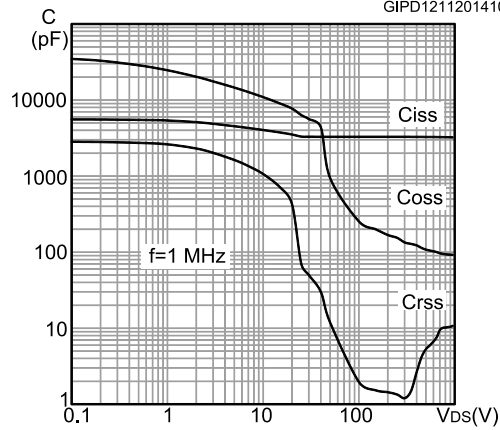


Figure 9: Normalized gate threshold voltage vs temperature

GIPD121120141035FSR

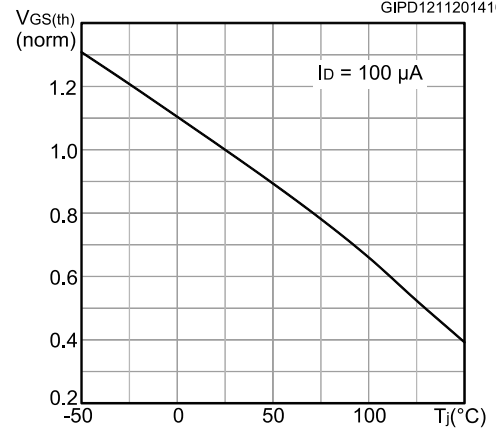


Figure 10: Normalized on-resistance

GIPD121120141039FSR

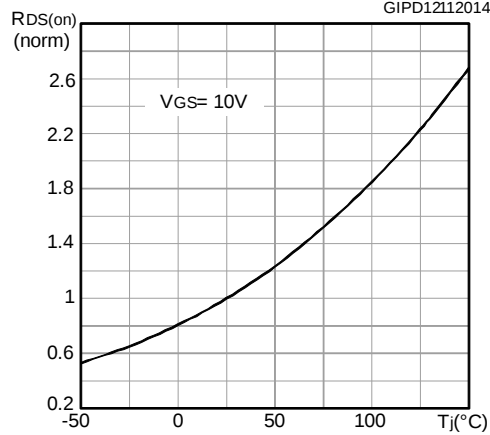


Figure 11: Normalized V(BR)DSS vs temperature

GIPD121120141041FSR

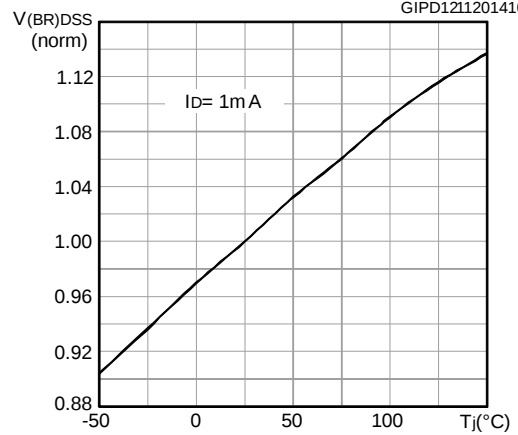


Figure 12: Output capacitance stored energy

GIPD121120141433FSR

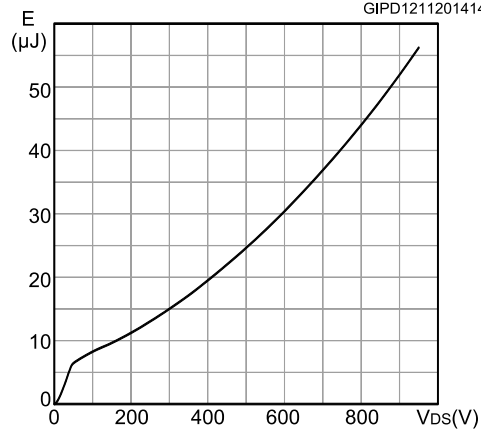


Figure 13: Source-drain diode forward characteristics

GIPD121120141439FSR

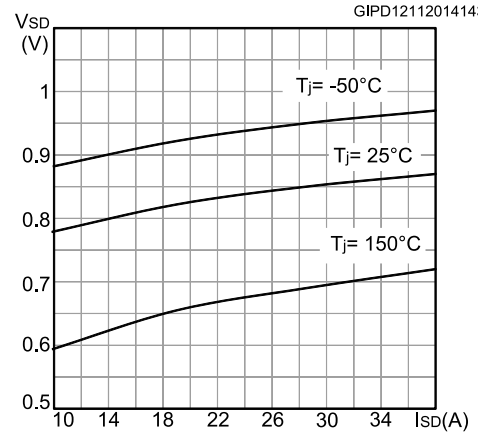
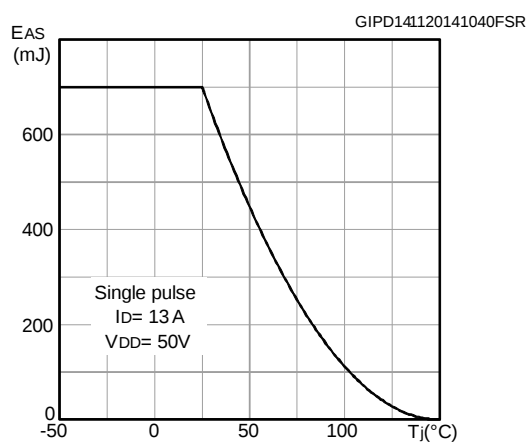


Figure 14: Maximum avalanche energy vs T J



3 Test circuits

Figure 15: Switching times test circuit for resistive load

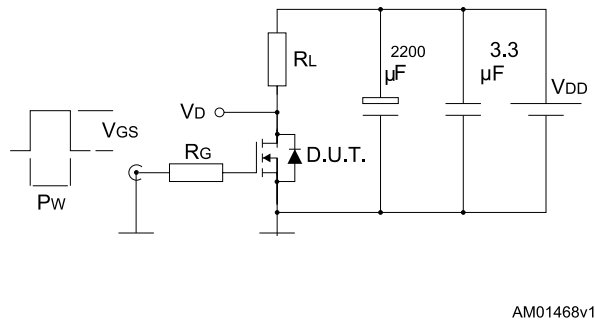


Figure 16: Gate charge test circuit

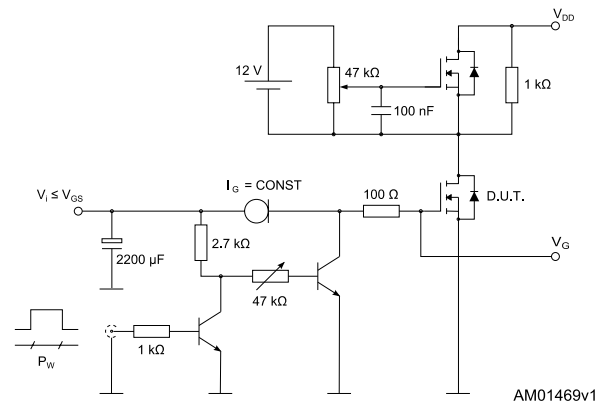


Figure 17: Test circuit for inductive load switching and diode recovery times

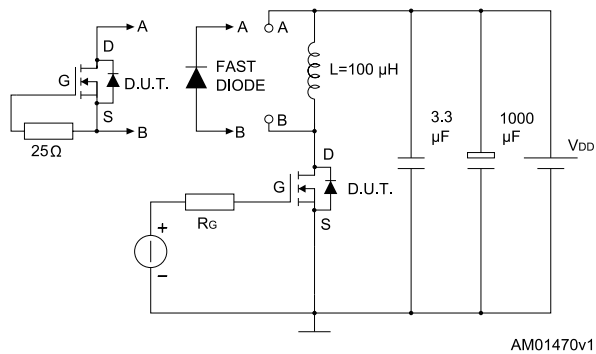


Figure 18: Unclamped inductive load test circuit

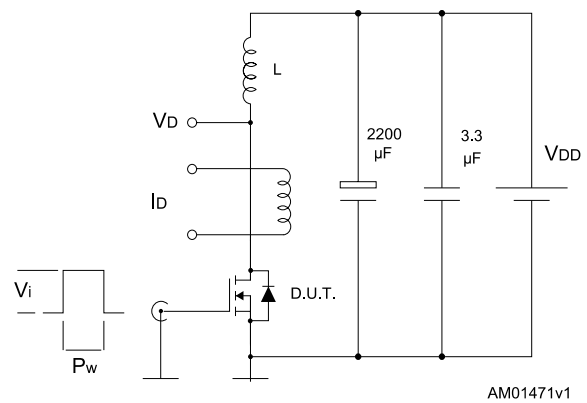


Figure 19: Unclamped inductive waveform

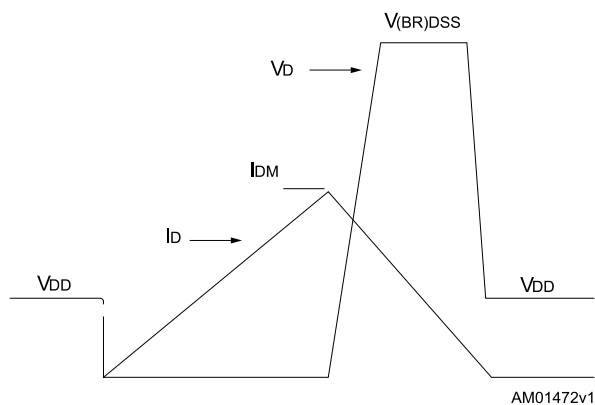
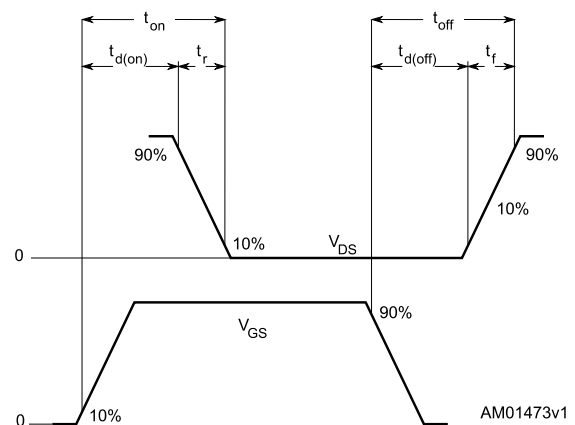


Figure 20: Switching time waveform

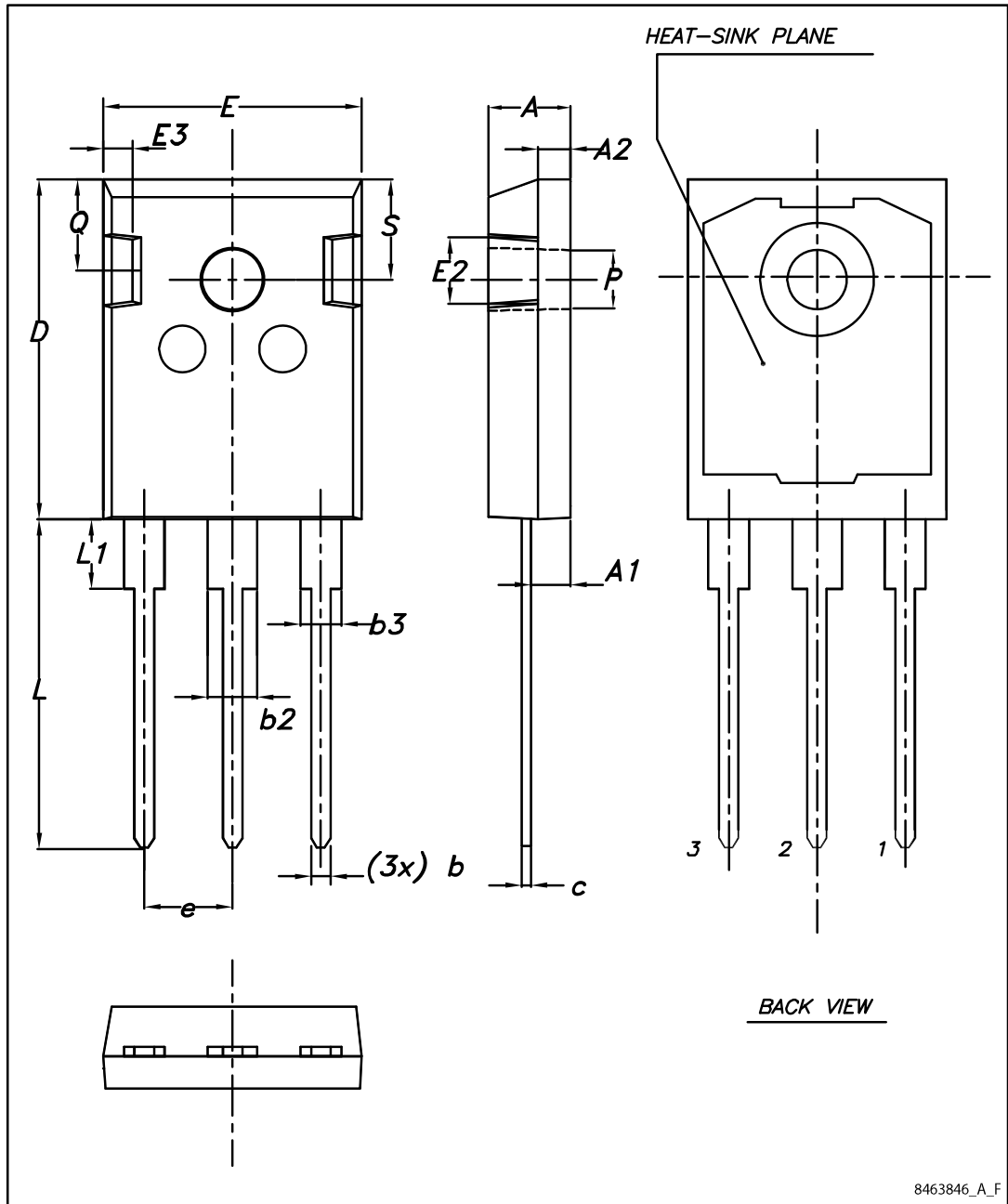


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 long leads package information

Figure 21: TO-247 long leads package outline



8463846_A_F

Table 9: TO-247 long leads package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
05-Aug-2015	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STWA40N95K5](#)