

N-channel 80 V, 6.4 mΩ typ., 80 A, STripFET™ F7 Power MOSFET in a TO-220 package

Datasheet - production data

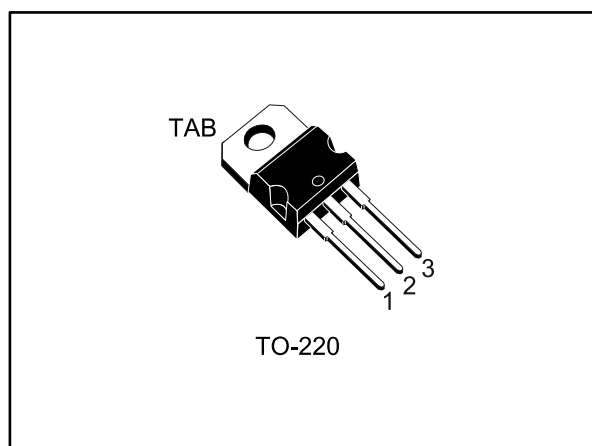
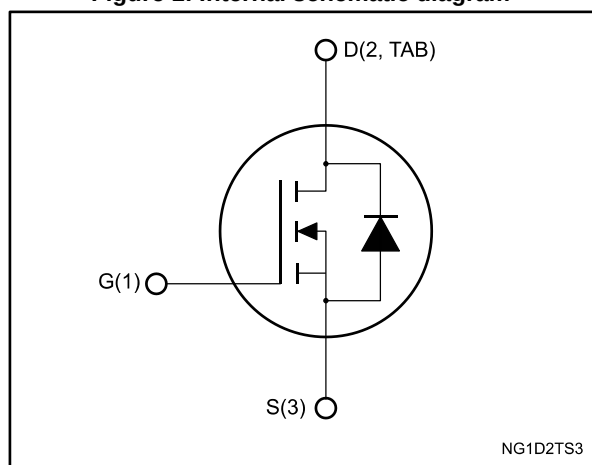


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)max}	I _D	P _{TOT}
STP110N8F7	80 V	7.5 mΩ	80 A	170 W

- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packaging
STP110N8F7	110N8F7	TO-220	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
	4.1 TO-220 package mechanical data	10
5	Revision history	12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	80 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	76	A
I_{DM} ⁽²⁾	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	170	W
E_{AS} ⁽³⁾	Single pulse avalanche energy	220	mJ
T_J	Operating junction temperature	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature		$^{\circ}\text{C}$

Notes:⁽¹⁾Limited by package⁽²⁾Pulse width is limited by safe operating area⁽³⁾Starting $T_J = 25^{\circ}\text{C}$, $I_d = 25\text{ A}$, $V_{dd} = 40\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.88	$^{\circ}\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^{\circ}\text{C/W}$

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	80			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 80\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 80\text{ V}, T_C = 125\text{ }^{\circ}\text{C}$			10	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		6.4	7.5	m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 40\text{ V}, f = 1\text{ MHz}$	-	3435	-	pF
C_{oss}	Output capacitance		-	653	-	pF
C_{rss}	Reverse transfer capacitance		-	57	-	pF
Q_g	Total gate charge	$V_{DD} = 40\text{ V}, I_D = 80\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	46.8	-	nC
Q_{gs}	Gate-source charge		-	23.4	-	nC
Q_{gd}	Gate-drain charge		-	11.2	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{ V}, I_D = 40\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	49	-	ns
t_r	Rise time		-	95	-	ns
$t_{d(off)}$	Turn-off delay time		-	60	-	ns
t_f	Fall time		-	32	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0$, $I_{SD} = 80$ A	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 80$ A, $di/dt = 100$ A/ μ s $V_{DD} = 60$ V (see Figure 15 : "Test circuit for inductive load switching and diode recovery times")	-	48.6		ns
Q_{rr}	Reverse recovery charge		-	58.6		nC
I_{RRM}	Reverse recovery current		-	2.4		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μ s, duty cycle 1.5%

2.2 Electrical characteristics (curves)

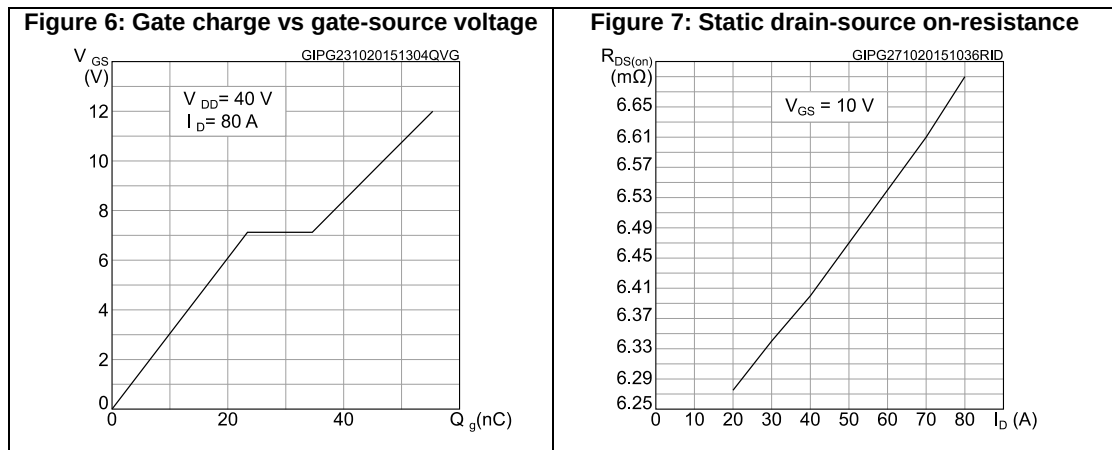
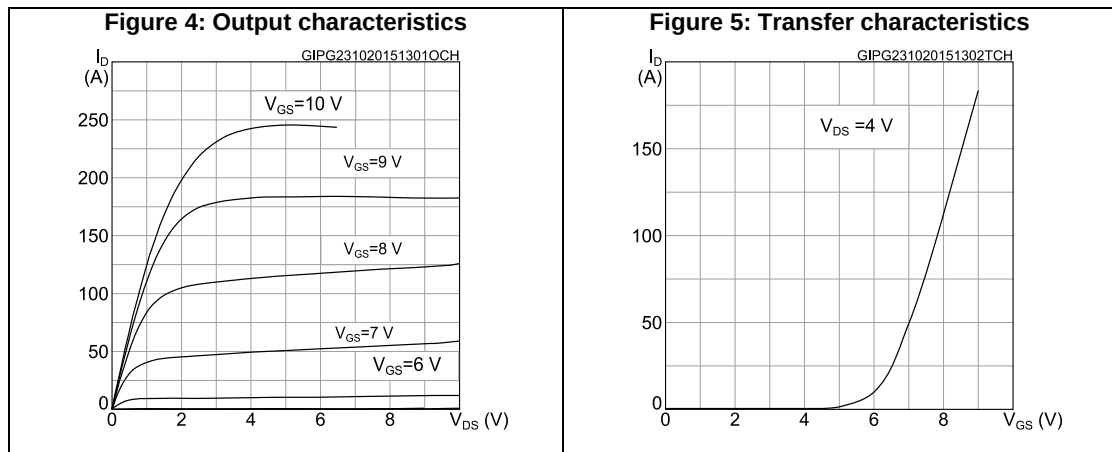
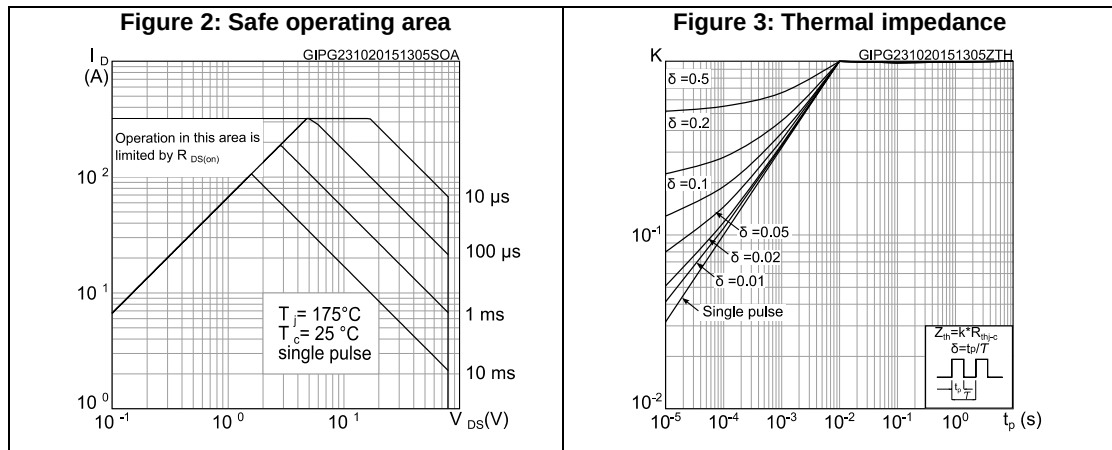


Figure 8: Capacitance variations

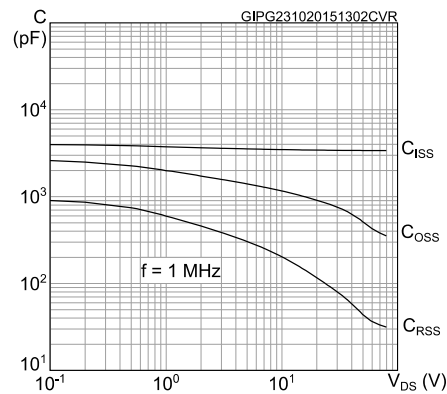


Figure 9: Normalized gate threshold voltage vs temperature

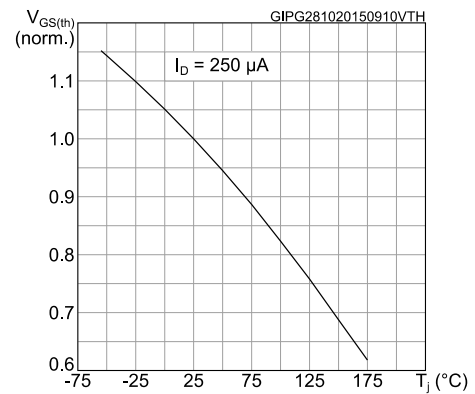


Figure 10: Normalized on-resistance vs temperature

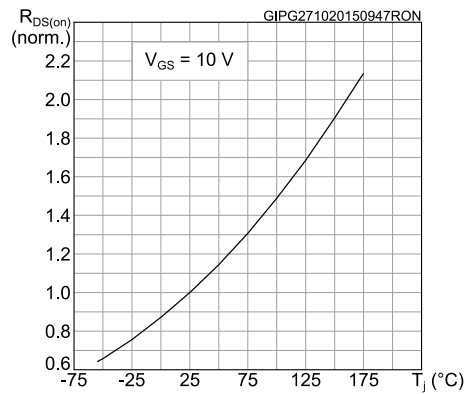
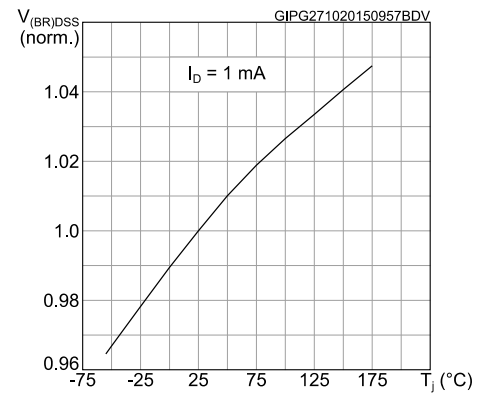
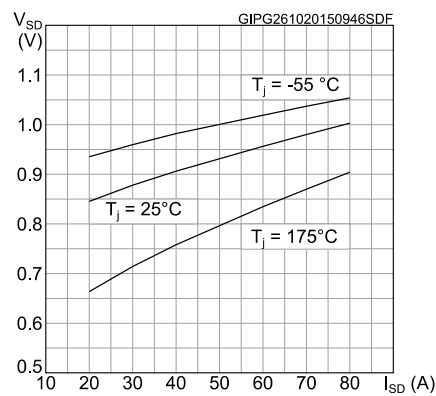
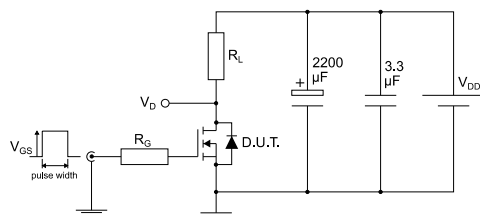
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



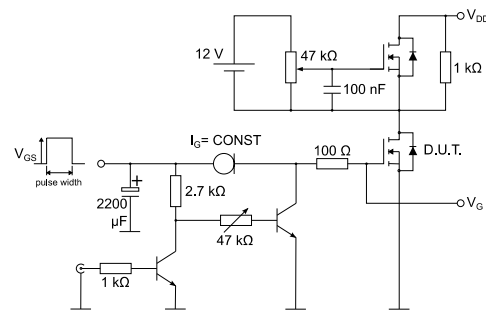
3 Test circuits

Figure 13: Test circuit for resistive load switching times



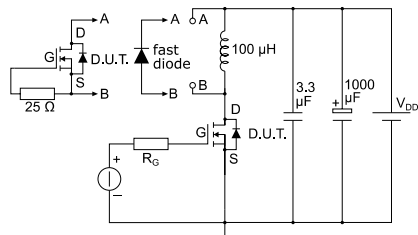
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Figure 14: Test circuit for gate charge behavior



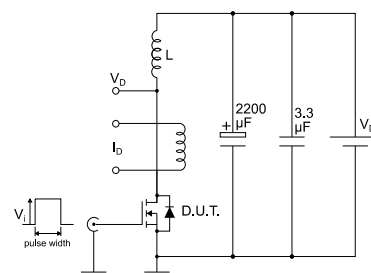
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Figure 15: Test circuit for inductive load switching and diode recovery times



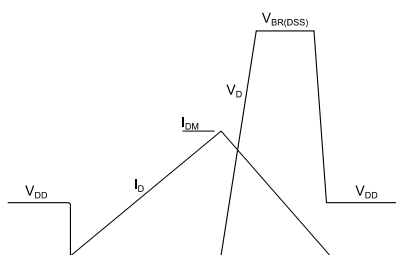
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Figure 16: Unclamped inductive load test circuit



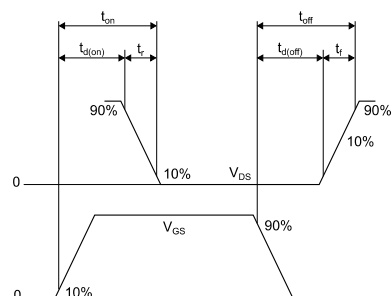
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



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4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-220 package mechanical data

Figure 19: TO-220 type A package outline

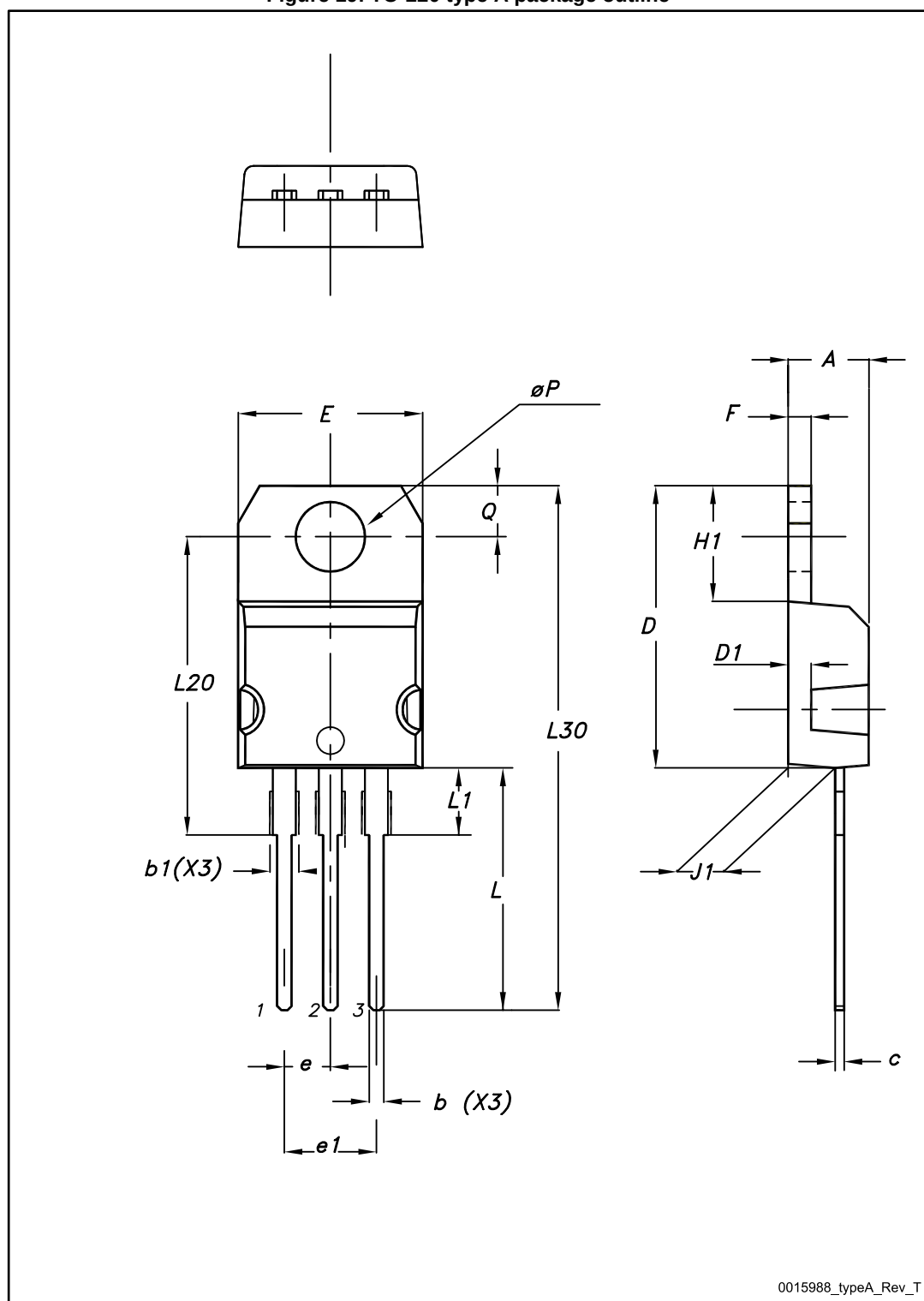


Table 8: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
10-Nov-2014	1	Initial release.
04-Nov-2015	2	Datasheet promoted from target to production data. Modified: Table 2: "Absolute maximum ratings" , Table 5: "Dynamic" , Table 6: "Switching times" and Table 7: "Source drain diode" Added: Section 4.1: "Electrical characteristics (curves)" Minor text changes.

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