# STBB3J

## 2 A, high efficiency single inductor buck-boost DC-DC converter

**Datasheet - production data**

**Flip Chip 20, pitch = 0.4 mm**

## Features

- Input voltage range from 1.8 V to 5.5 V
- 2 A output current at 3.3 V in buck mode ($V_{IN}$ = 3.6 V to 5.5 V)
- 800 mA output current at 3.3 V in boost mode ($V_{IN}$ 2.0 V)
- Typical efficiency higher than 94%
- ± 2% DC feedback voltage tolerance
- Automatic transition between step-down and boost mode
- Adjustable output voltage from 1.2 V to 5.5 V
- Power save mode (PS) at light load
- 2.0 MHz fixed switching frequency
- Adjustable switching frequency up to 2.4 MHz (by external synchronous square signal)
- Device quiescent current less than 50 µA
- Load disconnect during shutdown
- Shutdown function and soft-start
- Shutdown current < 1 µA
- Available in Flip Chip 20, pitch = 0.4 mm

## Applications

- Single cell Li-Ion, two-cell and three-cell alkaline, Ni-MH powered devices
- Memory card supply
- Tablet, smartphones
- Digital cameras

## Description

The STBB3J is a fixed frequency, high efficiency, buck-boost DC-DC converter which provides output voltages from 1.2 V to 5.5 V starting from input voltage from 1.8 V to 5.5 V. The device can operate with input voltages higher than, equal to, or lower than the output voltage making the product suitable for cell lithium-Ion applications where the output voltage is within the battery voltage range. The low-$R_{DS(on)}$ N-channel and P-channel MOSFET switches are integrated and contribute to achieve high efficiency. The MODE pin allows the selection between auto mode and forced PWM mode, taking advantage from either lower power consumption or best dynamic performance.The device also includes soft-start control, thermal shutdown, and current limit. The STBB3J is packaged in Flip Chip 20 bumps with 2.5 x 1.75 mm.

**Table 1. Device summary**

| Order code | Part number | Marking | Packing | Output voltage |
|---|---|---|---|---|
| STBB3JR | STBB3J | BB3 | Flip Chip 20 | Adjustable |

# Contents

# List of figures

# 1 Application schematic

**Figure 1. Application schematic for adjustable output version**

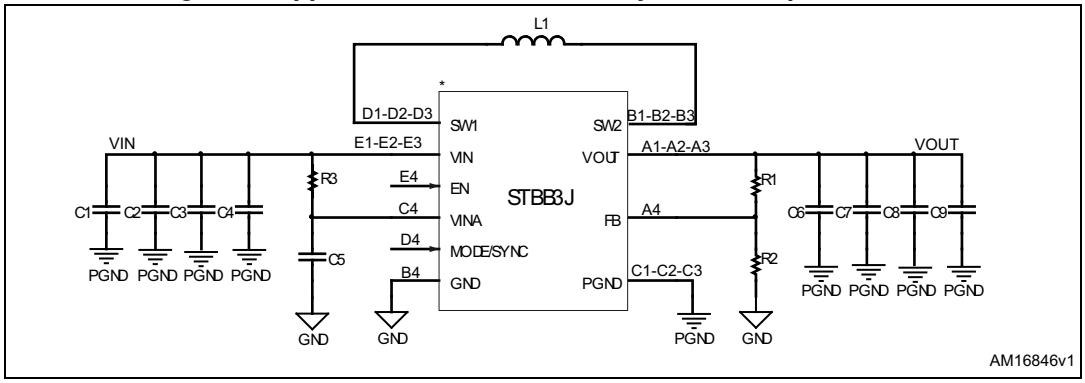



**Table 2. Typical external components**

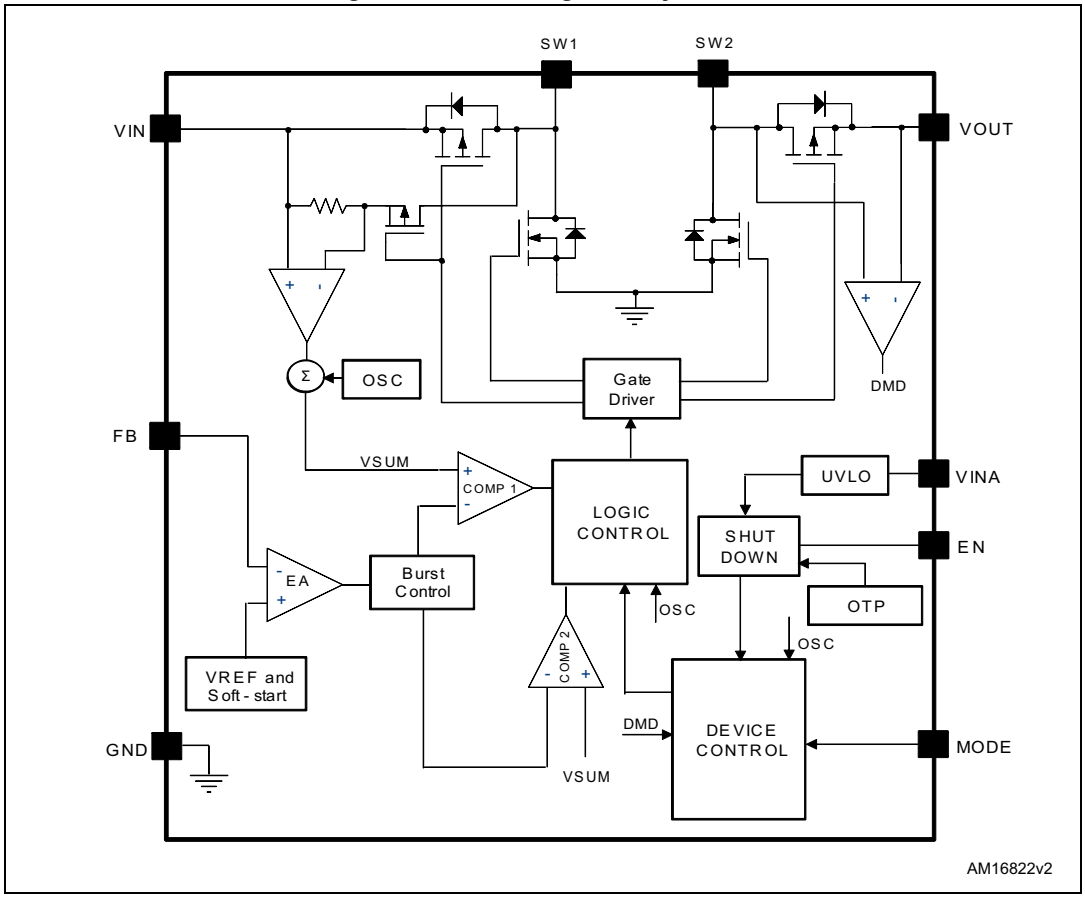
| Component | Manufacturer | Part number | Value | Size |
|---|---|---|---|---|
| C1,C2,C3, C4 | Murata | GRM188R60J106ME84 | 10 µF | 0603 |
| C6, C7, C8, C9 | TDK-EPC | C1608X5R1A106M | | |
| C5 | Murata | TBD | 100 nF | 0603 |
| | TDK-EPC | C1608X7R1H104K | | |
| L(1) | Coilcraft | XFL4020-152MEB | 1.5 µH | 4 x 3.2 x 1.5 mm |
| | TDK-EPC | VLF403215MT-1R5N | | 4 x 4 x 2 mm |
| R1 | Depending on the output voltage | | | 0603 |
| R2 | Depending on the output voltage | | | 0603 |
| R3 | - | - | 47 Ω | 0603 |

1. Inductor used for the maximum power capability. Optimized choice can be made according to the application conditions (see *Section 8*).

*Note: All the above components refer to a typical application. Operation of the device is not limited to the choice of these external components.*

# 2 Block diagram

**Figure 2. Block diagram adjustable**



# 3 Pin configuration

**Figure 3. Pin connection top view**

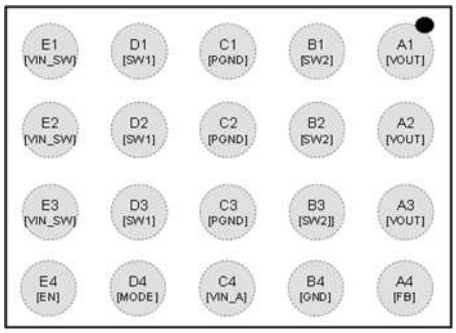



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**Figure 4. Pin connection bottom view**

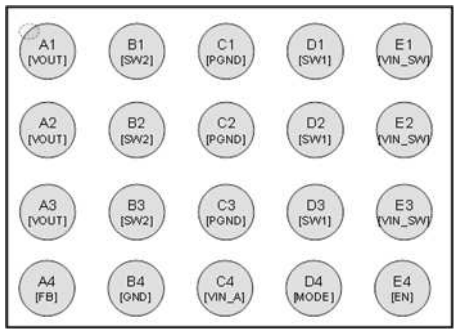


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**Table 3. Pin description**

| Pin name | Pin | Description |
|---|---|---|
| VOUT | A1, A2, A3 | Output voltage. |
| SW1 | D1, D2, D3 | Switch pin - internal switches are connected to this pin. Connect inductor between SW1 to SW2. |
| PGND | C1, C2, C3 | Power ground. |
| SW2 | B1, B2, B3 | Switch pin - internal switches are connected to this pin. Connect inductor between SW1 and SW2. |
| EN | E4 | Enable pin. Connect this pin to GND or a voltage lower than 0.4 V to shut down the IC. A voltage higher than 1.2 V is required to enable the IC. |
| MODE/SYNC | D4 | When in normal operation, the MODE pin selects between auto transition mode and fixed frequency PWM mode. If the MODE pin is low, the STBB3J automatically switches between pulse-skipping and standard fixed frequency PWM according to the load level. If the MODE pin is pulled high, the STBB3J works always at fixed frequency. When a square wave is applied, this pin provides the clock signal for oscillator synchronization. |
| VIN_A | C4 | Supply voltage for control stage. Connecting an R-C filter between VIN_A and GND. |
| VIN_SW | E1, E2, E3 | Power input voltage. |
| GND | B4 | Signal ground. |
| FB | A4 | Feedback voltage. |

# 4 Absolute maximum ratings

**Table 4. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| VIN_A, VIN_SW | Supply voltage | -0.3 to 7.0 | V |
| SW1,SW2 | Switching nodes | -0.3 to 7.0 | V |
| VOUT | Output voltage | -0.3 to 7.0 | V |
| MODE, EN | Logic pins | -0.3 to 7.0 | V |
| FB | Feedback pin for adjustable version | -0.3 to 1.5 | V |
| ESD | Human body model | ± 2000 | V |
| $T_{AMB}$ | Operating ambient temperature | -40 to 85 | °C |
| $T_J$ | Maximum operating junction temperature | 150 | °C |
| $T_{STG}$ | Storage temperature | -65 to 150 | °C |

*Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.*

**Table 5. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(JA)}$ | Thermal resistance junction-ambient | 84 | °C/W |

# 5 Electrical characteristics

$V_{IN}$ = $V_{INA}$ = $V_{EN}$ = 3.6 V, $V_{OUT}$ = 3.3 V, $C_{IN}$ = 4x10 µF, $C_{OUT}$ = 4 x 10 µF, $R_{INA}$ = 47 Ohm, $C_{INA}$ = 100 nF, L = 1.5 µH, $T_A$ = - 40 °C to 85 °C (unless otherwise specified; typical values are referred to $T_A$ = 25 °C).

**Table 6. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General section** | | | | | | |
| $V_{IN}$ | Input voltage range | | 1.8 | | 5.5 | V |
| | Minimum input voltage for the startup | $I_{OUT}$ = 600 mA, mode = $V_{IN}$ | | 1.8 | 1.9 | V |
| $V_{UVLO}$ | Undervoltage lockout threshold | $V_{INA}$ rising, $I_{OUT}$ = 100 mA MODE = $V_{IN;}$ | 1.5 | 1.6 | 1.7 | V |
| | | $V_{INA}$ falling; $I_{OUT}$ = 100 mA $V_{MODE}$ = $V_{IN;}$ | 1.4 | 1.5 | 1.6 | |
| $I_q$ | Quiescent current $V_{IN}$ and $V_{INA}$ | $I_{OUT}$ = 0 A $V_{MODE}$ = GND | | | 50 | µA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ = GND | | 0.1 | 1 | µA |
| $V_{FB}$ | Feedback voltage | $V_{IN}$ from 1.8 to 5.5 V | 490 | 500 | 510 | mV |
| $f_{SW}$ | Switching frequency | $T_A$ = 25 °C | 1.8 | 2 | 2.2 | MHz |
| | Frequency range for external synchronization | | 1.6 | | 2.4 | |
| $I_{OUT}$ | Continuous output current (1) | $V_{IN}$ from 1.8 to 5.5 V | 600 | | | mA |
| $I_{SWL}$ | Switch current limitation | $T_A$ = 25 °C | 2.8 | 3 | 3.65 | A |
| $I_{PK}$ | Switch current limitation | | 2.3 | 2.5 | 2.7 | A |
| $I_{PS-PWM}$ | PS to PWM transition | | | 730 | | mA |
| | PWM to PS transition | | | 680 | | |
| **Output voltage** | | | | | | |
| $V_{OUT}$ | Output voltage range | | 1.2 | | 5.5 | V |
| $\%\Delta_{OUT}$ | Maximum load regulation | $V_{IN}$ = 2.5 to 5.5 V, $V_{MODE}$ = $V_{IN}$ | -1.5 | | +1.5 | % |
| | | $V_{IN}$ = 2.5 to 5.5 V, $V_{MODE}$ = GND suitable output current to keep PS operation | -3 | | +3 | % |
| $\%V_{OUT}$ | Maximum load regulation | $I_{LOAD}$ = from 10 mA to 800 mA | | ± 0.5 | | % |
| $V_{OPP-PS}$ | Peak-to-peak ripple in PS mode | $I_{OUT}$ = 100 mA | | 100 | | mV |
| $I_{LKFB}$ | FB pin leakage current | $V_{FB}$ = 1.5 V | | | 1 | µA |
| **Control stage** | | | | | | |
| $V_{IL}$ | Low-level input voltage (EN, MODE pins) | | | | 0.4 | V |

**Table 6. Electrical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage (EN, MODE pins) | | 1.2 | | | V |
| $I_{LK-I}$ | Input leakage current (EN, MODE pins) | $V_{EN} = V_{MODE} = 5.5$ V | | 0.01 | 1 | µA |
| $T_{ON}$ | Turn on-time(2) | $V_{EN}$ from low to high, $I_{OUT} = 10$ mA | | 260 | 300 | µs |
| **Power switches** | | | | | | |
| $R_{DS(on)}$ | P-channel on-resistance | | | 100 | 300 | mΩ |
| | N-channel on-resistance | | | 100 | 300 | mΩ |
| $I_{LKG-P}$ | P-channel leakage current | $V_{IN} = V_{OUT} = 5.5$ V; $V_{EN} = 0$ | | | 1 | µA |
| $I_{LKG-N}$ | N-channel leakage current | $V_{SW1} = V_{SW2} = 5.5$ V; $V_{EN} = 0$ | | | 1 | µA |

1. Not tested in production. This value is guaranteed by correlation with $R_{DS(on)}$, peak current limit and operating input voltage.
2. Not tested in production.

# 6 Typical performance characteristics

**Table 7. Table of graphs**

| Parameter | Test conditions | Ref. |
|---|---|---|
| Efficiency | vs. output current (power save enabled, $V_{IN}$ = 1.8 V, 3.6 V, 5.5 V/$V_{OUT}$ = 3.3 V) | *Figure 4* |
| | vs. output current (power save disabled, $V_{IN}$ = 1.8 V, 3.6 V, 5.5 V/$V_{OUT}$ = 3.3 V) | *Figure 5* |
| | vs. output current (PWM/auto mode), $V_{IN}$ = 1.8 V, $V_{OUT}$ = 3.3 V | *Figure 6* |
| | vs. output current (PWM/auto mode), $V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.3 V | *Figure 7* |
| | vs. output current (PWM/auto mode), $V_{IN}$ = 5.5 V, $V_{OUT}$ = 3.3 V | *Figure 8* |
| Maximum output current | vs. input voltage ($V_{OUT}$ = 3.3 V, $V_{OUT}$ = 5.0 V) | *Figure 9* |
| Waveforms | Line transient response ($V_{IN}$ = 3.0 V to 3.6 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 mA) | *Figure 10* |
| | Line transient response ($V_{IN}$ = 3.6 V to 3.0 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 mA) | *Figure 11* |
| | Line transient response ($V_{IN}$ = 3.6 V to 4.0 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 mA) | *Figure 12* |
| | Line transient response ($V_{IN}$ = 4.0 V to 3.6 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 mA) | *Figure 13* |
| | Load transient response $V_{IN}$ = 1.8 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 to 300 mA | *Figure 14* |
| | Load transient response $V_{IN}$ = 1.8 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 to 100 mA | *Figure 15* |
| | Load transient response $V_{IN}$ = 3.6 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 to 300 mA | *Figure 16* |
| | Load transient response $V_{IN}$ = 3.6 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 to 100 mA | *Figure 17* |
| | Load transient response $V_{IN}$ = 5.5 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 to 300 mA | *Figure 18* |
| | Load transient response $V_{IN}$ = 5.5 V $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 300 to 100 mA | *Figure 19* |
| | Startup after enable ($V_{IN}$ = 1.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 10 mA) | *Figure 20* |
| | Startup after enable ($V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 10 mA) | *Figure 21* |
| | Startup after enable ($V_{IN}$ = 5.5 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 10 mA) | *Figure 22* |
| Output voltage | vs. output current ($V_{OUT}$ = 3.3 V) | *Figure 23* |

**Figure 5. Efficiency vs. output current (power save mode enabled $V_{OUT}$ = 3.3 V)**

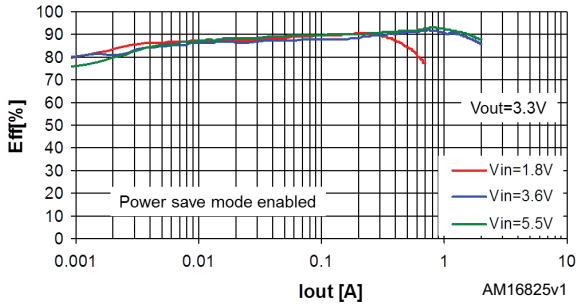



**Figure 6. Efficiency vs. output current (power save mode disabled $V_{OUT}$ = 3.3 V)**

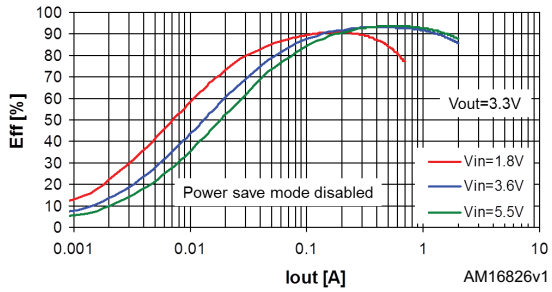



**Figure 7. Efficiency vs. output current (PWM/auto mode $V_{IN}$ = 1.8 V)**

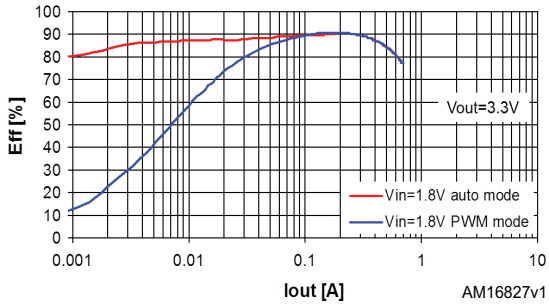



**Figure 8. Efficiency vs. output current (PWM/auto mode $V_{IN}$ = 3.6 V)**

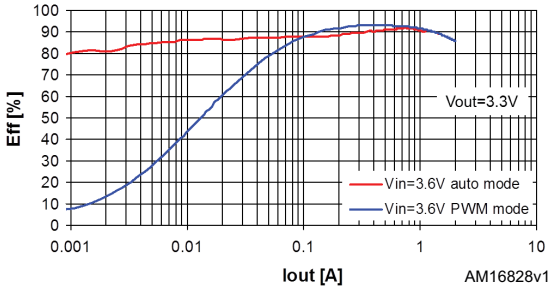



**Figure 9. Efficiency vs. output current (PWM/auto mode $V_{IN}$ = 5.0 V)**

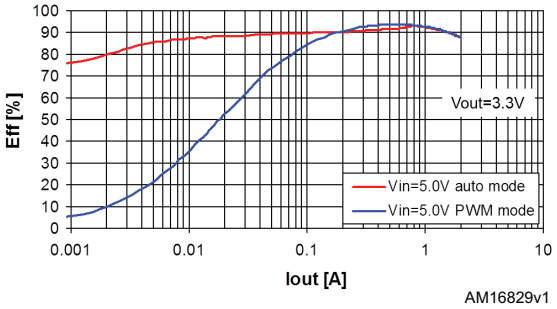



**Figure 10. Maximum output current vs. input voltage**

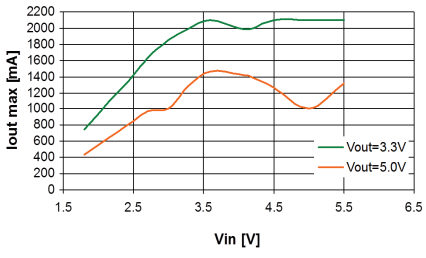
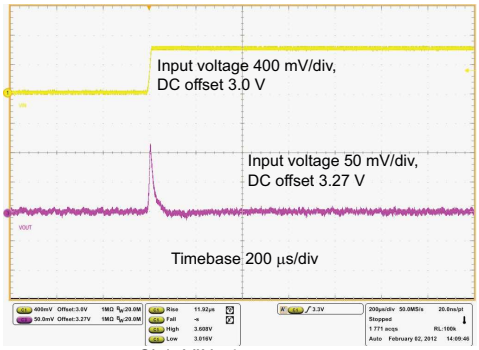
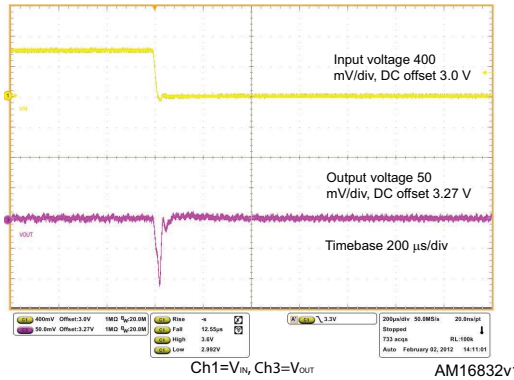


**Figure 11. Line transient response @ $V_{IN}$ = 3 V to 3.6 V**



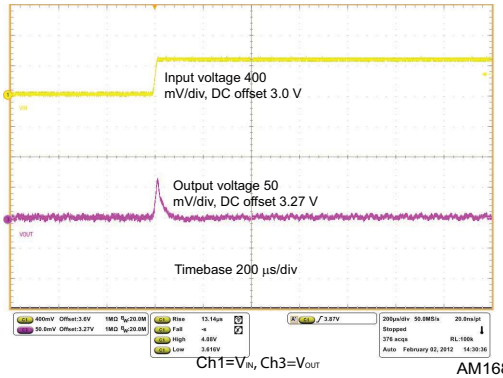

Ch1=VIN, Ch3=VOUT AM16831v1

**Figure 12. Line transient response @ $V_{IN}$ = 3.6 V to 3 V**



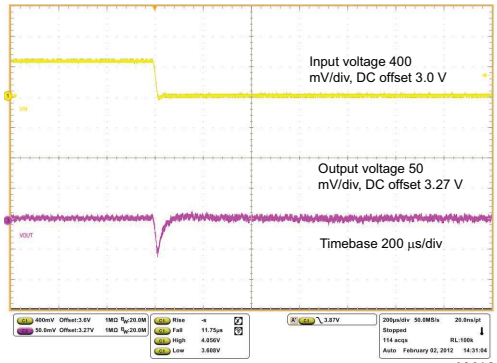

Ch1=$V_{IN}$, Ch3=$V_{OUT}$ AM16832v1

**Figure 13. Line transient response @ $V_{IN}$ = 3.6 V to 4 V**



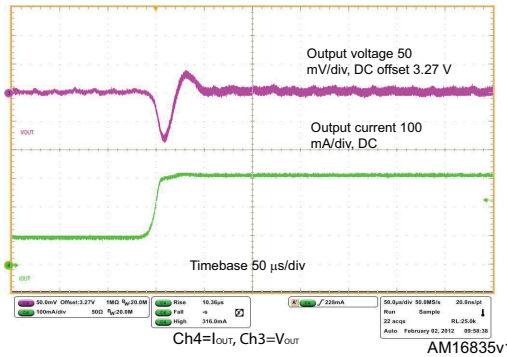

Ch1=$V_{IN}$, Ch3=$V_{OUT}$ AM16833v1

**Figure 14. Line transient response @ $V_{IN}$ = 4 V to 3.6 V**



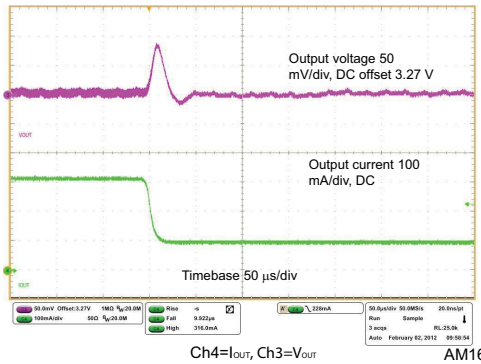

Ch1=$V_{IN}$, Ch3=$V_{OUT}$ AM16834v1

**Figure 15. Load transient response @ $V_{IN}$=1.8 V, $I_{OUT}$ = 100 to 300 mA**



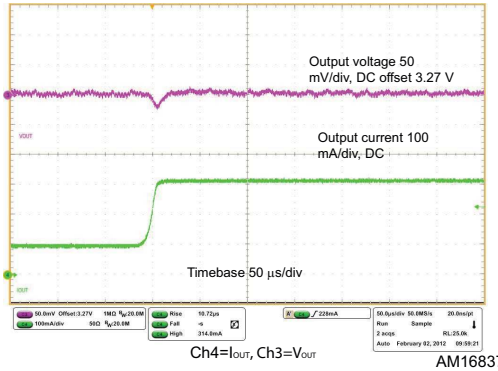

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16835v1

**Figure 16. Load transient response @ $V_{IN}$=1.8 V, $I_{OUT}$ = 300 mA to 100 mA**



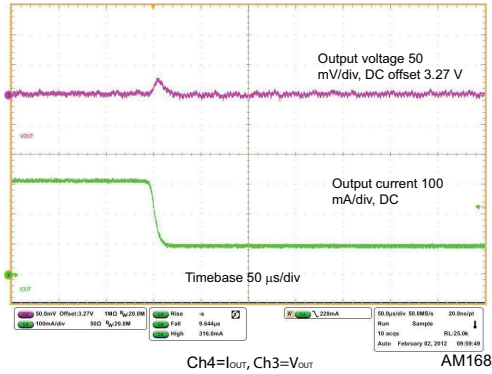

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16836v1

**Figure 17. Load transient response @ $V_{IN}$=3.6 V, $I_{OUT}$ = 100 to 300 mA**



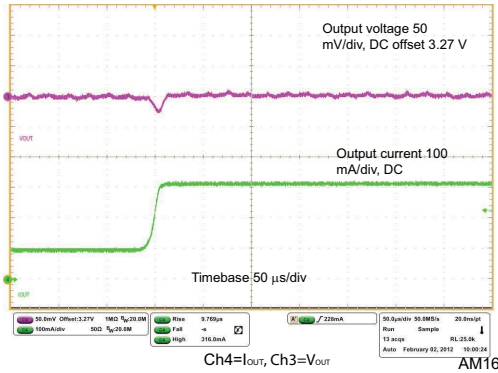

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16837v1

**Figure 18. Load transient response @ $V_{IN}$=3.6 V, $I_{OUT}$ = 300 mA to 100 mA**



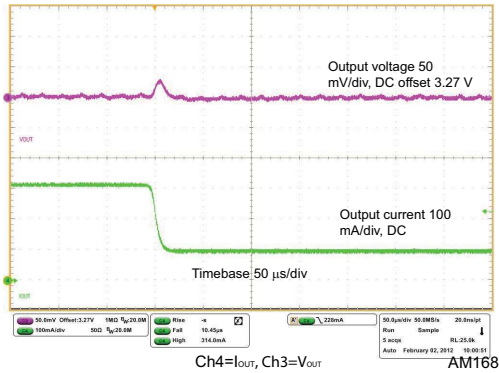

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16838v1

**Figure 19. Load transient response @ $V_{IN}$=5.5 V, $I_{OUT}$ = 100 to 300 mA**



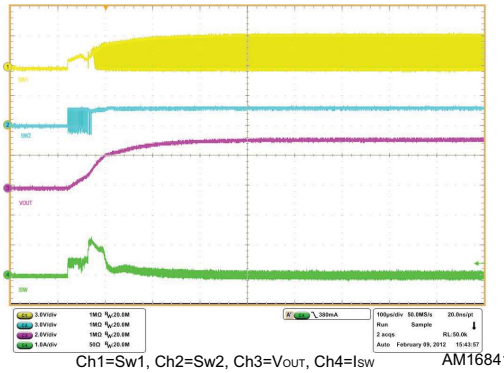

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16839v1

**Figure 20. Load transient response @ $V_{IN}$=5.5 V, $I_{OUT}$ = 300 to 100 mA**



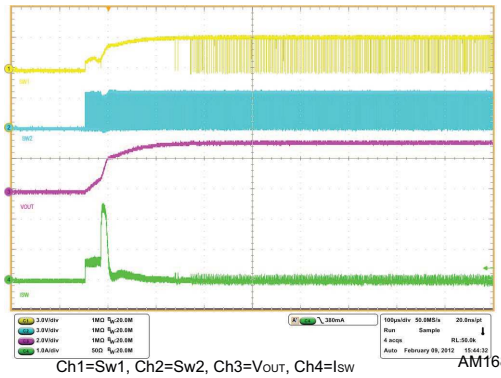

Ch4=$I_{OUT}$, Ch3=$V_{OUT}$ AM16840v1

**Figure 21. Startup after enable @ $V_{IN}$=1.8 V**



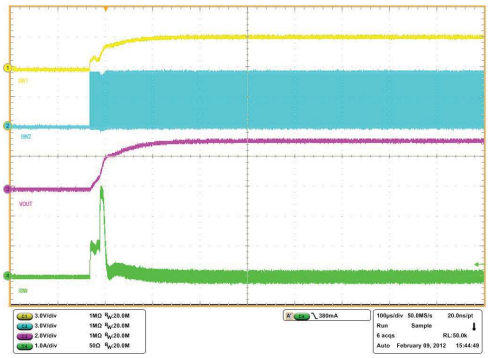
Ch1=Sw1, Ch2=Sw2, Ch3=$V_{OUT}$, Ch4=$I_{SW}$ AM16841v1

**Figure 22. Startup after enable @ $V_{IN}$=3.6 V**



Ch1=Sw1, Ch2=Sw2, Ch3=$V_{OUT}$, Ch4=$I_{SW}$ AM16842v1

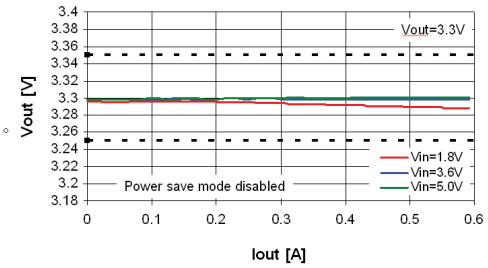
**Figure 23. Startup after enable @ $V_{IN}$=5.5 V**



Ch1=Sw1, Ch2=Sw2, Ch3=$V_{OUT}$, Ch4=Isw

AM16843v1

**Figure 24. Output voltage vs. output current**




AM16844v1

# 7 General description

The STBB3J is a high efficiency dual mode buck-boost switch mode converter. Thanks to the 4 internal switches, 2 P-channels and 2 N-channels, it is able to deliver a well-regulated output voltage using a variable input voltage which can be higher than, equal to, or lower than the desired output voltage. This solves most of the power supply problems that circuit designers face when dealing with battery-powered equipment.

The controller uses a peak current mode technique in order to obtain good stability in all possible conditions of input voltage, output voltage and output current. In addition, the peak inductor current is monitored to avoid saturation of the coil.

The STBB3J can work in two different modes: PWM mode or power save mode. Top-class line and load transients are achieved thanks to a feed-forward technique and due to the innovative control method specifically designed to optimize the performances in the buck-boost region where input voltage is very close to the output voltage.

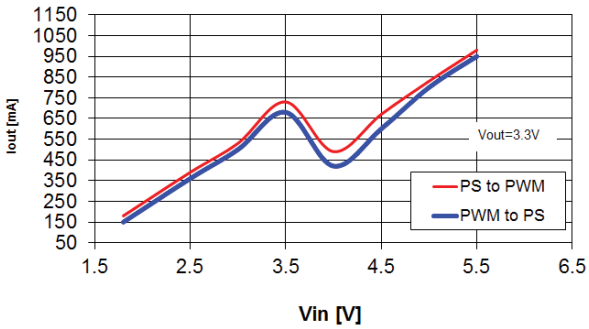
The STBB3J is self-protected from short-circuit and overtemperature. Undervoltage lockout and soft-start guarantee proper operation during startup.

Input voltage and ground connections are split into power and signal pins. This allows reduction of internal disturbances when the 4 internal switches are working. The switch bridge is connected between the $V_{IN}$ and PGND pins while all logic blocks are connected between $V_{INA}$ and GND.

## 7.1 Dual mode operation

The STBB3J works in PWM mode or in power save mode (PS) according to the different status of the MODE pin. If the MODE pin is pulled high the device works in PWM only. In this case the device operates at 2 MHz fixed frequency pulse width modulation (PWM mode) in all line/load conditions. In this condition, the STBB3J provides the best dynamic performance. If the MODE pin is pulled low, at low average current the STBB3J enters PS mode allowing very low power consumption and therefore obtaining very good efficiency event at light load. When the average current increases, the device automatically switches to PWM mode in order to deliver the power needed by the load. In PS mode the STBB3J implements a burst mode operation: if the output voltage increases above its nominal value the device stops switching; as soon the $V_{OUT}$ falls below the nominal value the device restarts switching with a programmed average current higher than the one needed by the load. *Figure 25* shows PS mode operation areas vs. output current in typical application conditions.

Figure 25. Auto mode vs. output current




## 7.2 External synchronization

The STBB3J implements the external synchronization function. If an external clock signal is applied to the MODE/SYN pin with a frequency between 1.6 MHz and 2.4 MHz and with proper low/high levels, the device automatically is in PWM mode and the external clock is used as switching oscillator.

## 7.3 Enable pin

The device turns on when the EN pin is pulled high. If the EN pin is low the device stops switching and all the internal blocks are turned off. In this condition the current drawn from $V_{IN}$/$V_{INA}$ is below 1 µA in the whole temperature range. In addition the internal switches are in off-state so the load is electrically disconnected from the input; this avoids unwanted current leakage from the input to the load.

## 7.4 Protection features

The STBB3J implements different types of protection features

### 7.4.1 Soft-start and short-circuit

After the EN pin is pulled high, or after a suitable voltage is applied to $V_{IN}$, $V_{INA}$ and EN, the device initiates the startup phase. The average current limit is gradually increased while the output voltage increases. As soon as the output voltage reaches 1.0 V, the average current limit is set to its nominal value.

### 7.4.2 Undervoltage lockout

The undervoltage lockout function prevents improper operation of the STBB3J when the input voltage is not high enough. When the input voltage is below the VUVLO threshold, the device is in shutdown mode. The hysteresis of 100 mV prevents unstable operation when the input voltage is close to the UVLO threshold.

### 7.4.3 Overtemperature protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 160 °C (typ.), the device stops operating. As soon as the temperature falls below 140 °C (typ.), normal operation is restored.

# 8 Application information

## 8.1 Programming the output voltage

The external resistor divider must be connected between $V_{OUT}$ and GND and the middle point of the divider must be connected to FB.

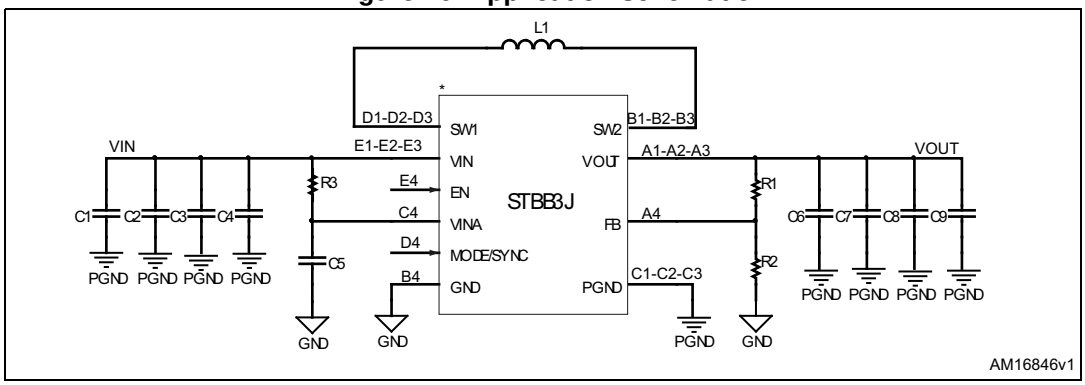
The value of the resistor R1, connected between $V_{OUT}$ and FB, is function of the output voltage and can be calculated using the equation 1:

**Equation 1**

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

The value for the resistor R2, placed between FB and GND must be selected in function of the FB pin leakage current and the $V_{OUT}$ accuracy.

**Figure 26. Application schematic**




## 8.2 Inductor selection

The inductor is the key passive component for switching converters. With a buck-boost device, the inductor selection must take into consideration the following two conditions in which the converter works:

- as buck region at the maximum input voltage
- as boost region at the minimum input voltage

Two critical inductance values are then obtained according to the following formulas:

**Equation 2**

$$L_{MIN\_BUCK} = \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{V_{IN\_MAX} \times f_S \times \Delta I_L}$$

**Equation 3**

$$L_{MIN\_BOOST} = \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{V_{OUT} \times f_S \times \Delta I_L}$$

where $f_S$ is the minimum value of the switching frequency and $\Delta I_L$ is the inductor ripple current. The amplitude of the inductor ripple current is typically set between 20% and 40% of the maximum inductor current. To guarantee an inductor ripple current always lower than the selected value $\Delta I_L$, the higher value between $L_{MIN\_BUCK}$ and $L_{MIN\_BOOST}$ have to be chosen.

In addition to the inductance value, also the maximum current which the inductor can handle must be calculated in order to avoid saturation.

**Equation 4**

$$I_{PEAK\_BUCK} = \frac{I_{OUT}}{\eta} + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{IN\_MAX} \times f_S \times L}$$

**Equation 5**

$$I_{PEAK\_BOOST} = \left(\frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN}}\right) + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times f_S \times L}$$

where $\eta$ is the estimated efficiency. The maximum of the two values above must be considered when selecting the inductor.

## 8.3 Input and output capacitor selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation.

Minimum values of 10 µF for both capacitors, $C_{IN}$ and $C_{OUT,}$ are needed to achieve good behavior of the device. The input capacitor must be placed as close as possible to the device.

An R-C filter is added to VINA pin (R3-C5 *Figure 26*) to assure a clean input voltage to the internal logic block.

## 8.4 Layout guidelines

Figure 27. Assembly layer

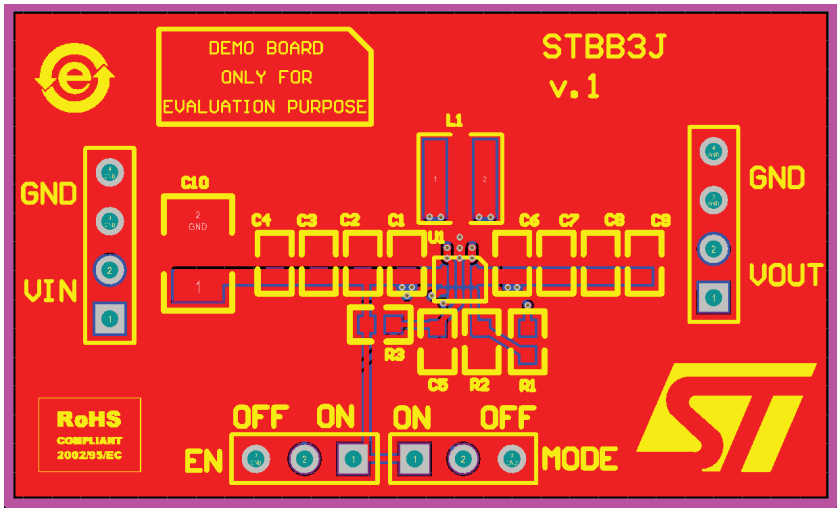



Figure 28. Top layer

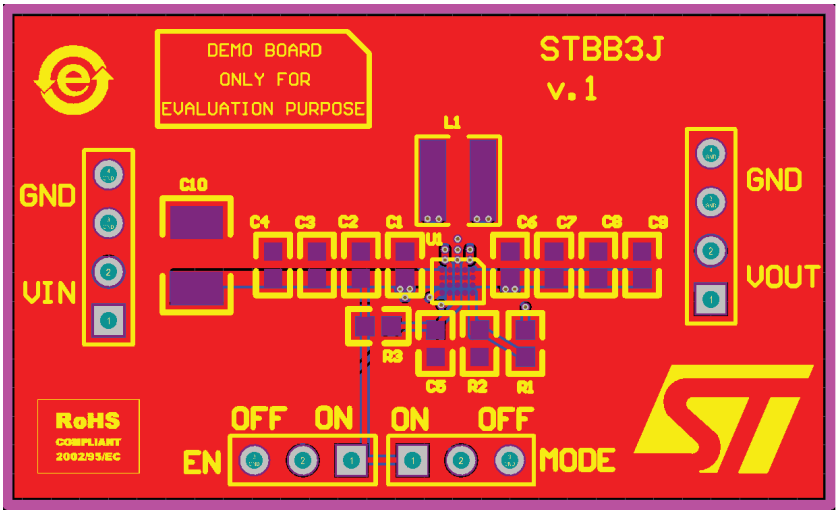
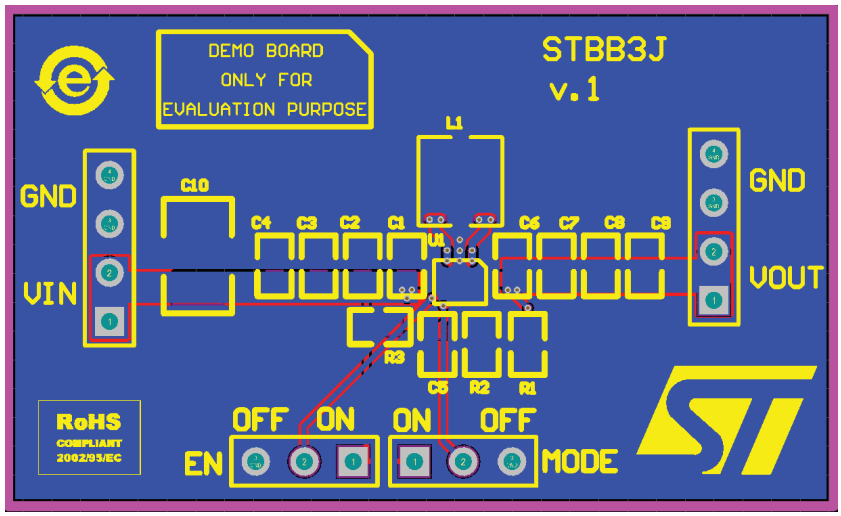


Figure 29. Bottom layer




AM16849v1

# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

**Figure 30. Flip Chip 20 (2.5 x 1.75 mm) outline**

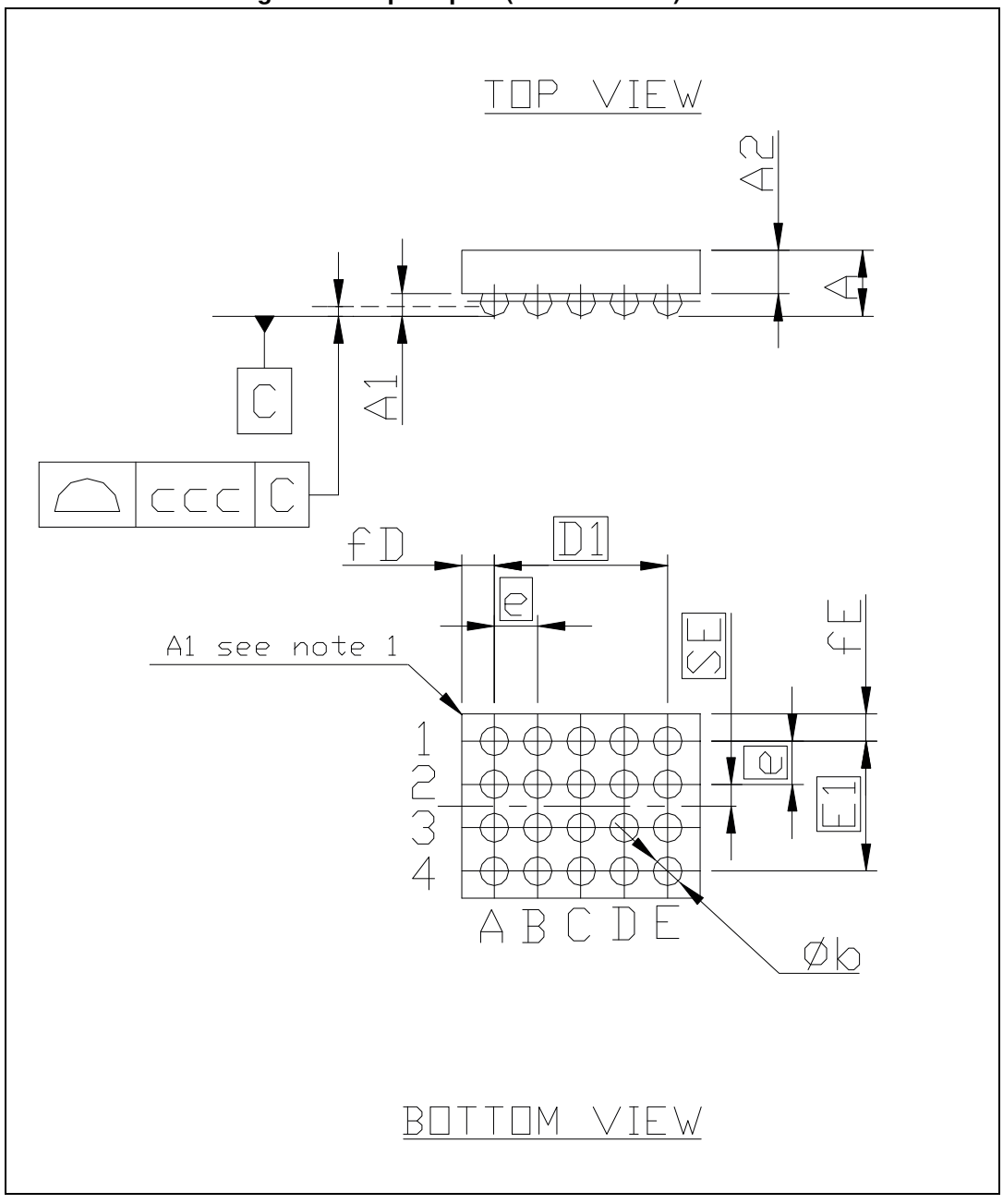


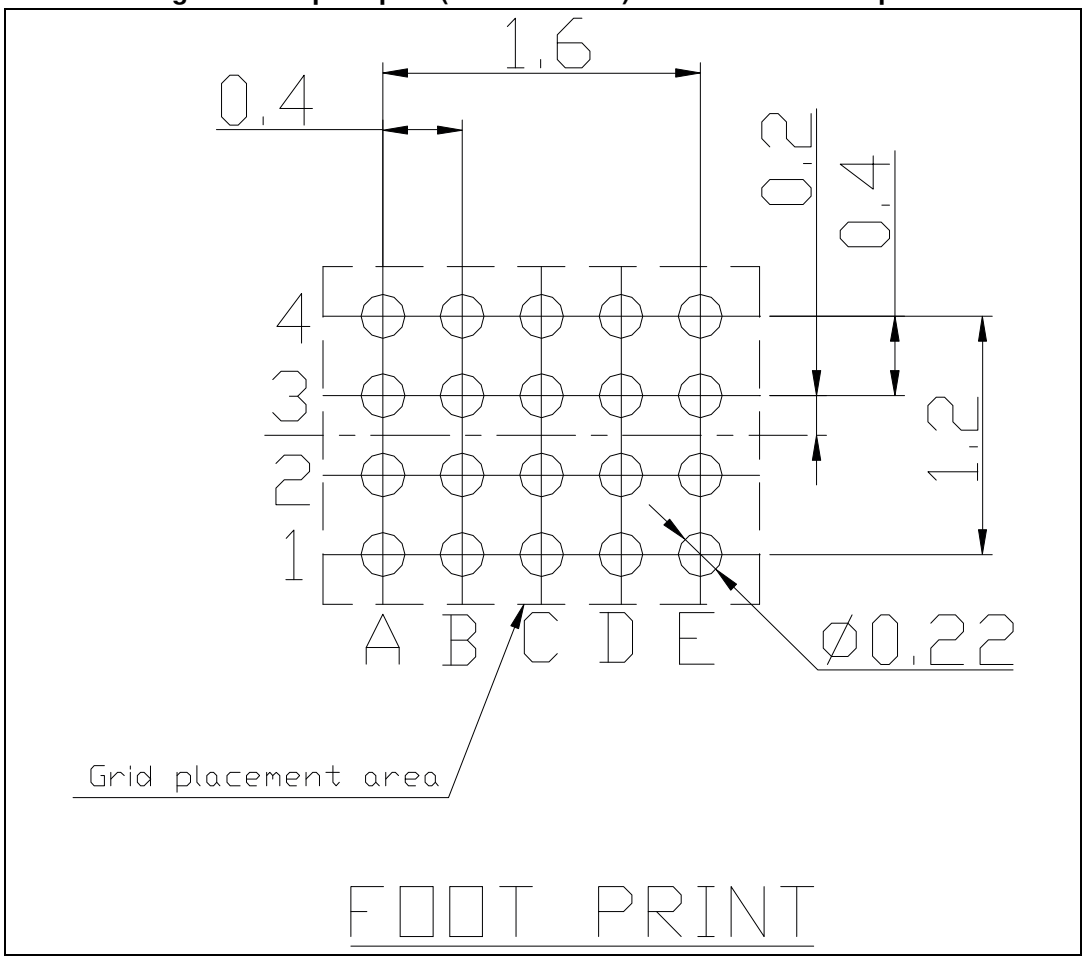
**Table 8. Flip Chip 20 (2.5 x 1.75 mm) mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.50 | 0.55 | 0.60 |
| A1 | 0.17 | 0.20 | 0.23 |
| A2 | 0.33 | 0.35 | 0.37 |
| b | 0.21 | 0.25 | 0.29 |
| D | 2.485 | 2.515 | 2.545 |
| D1 | | 1.6 | |
| E | 1.731 | 1.761 | 1.791 |
| E1 | | 1.2 | |
| e | | 0.40 | |
| fD | 0.447 | 0.457 | 0.467 |
| fE | 0.27 | 0.28 | 0.29 |
| SE | | 0.20 | |
| ccc | | 0.075 | |

*Note: The terminal A1 on the bump side is identified by a distinguishing feature (for instance by a circular “clear area” typically 0.1 mm diameter) and/or a missing bump.*

*The terminal A1 on the backside of the product is identified by a distinguishing feature (for instance by a circular “clear area” less than 0.5 mm diameter).*

Figure 31. Flip Chip 20 (2.5 x 1.75 mm) recommended footprint



# 10 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 26-Sep-2013 | 1 | Initial release. |
| 25-Jun-2014 | 2 | Document status promoted from preliminary to production data. |
| 25-Nov-2014 | 3 | Removed footnote from P-channel and N-channel on-resistance parameter in Table 6. |
| 28-Jan-2015 | 4 | Updated $I_{SWL}$ max.value in Table 6. |
| 10-Dec-2015 | 5 | Updated *Figure 1* and *Figure 26*. |
| 11-Dec-2020 | 6 | Updated *Figure 1* and *Figure 2*. |
| 29-Sep-2021 | 7 | Updated $I_{LKFB}$ parameter and max value in Table 6. |
| 06-Dec-2021 | 8 | Updated *Section 8.1*. |

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