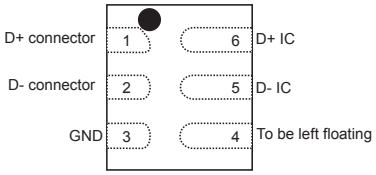
ECMF02-2HSMX6

Datasheet

ESD protected common mode filter for USB3.2 interface

µQFN-6L 1.7 X 1.5 mm

Pin out, top view



Product status link
ECMF02-2HSMX6

Features

- High common mode attenuation:
  - -10 dB at 300 MHz
  - -20 dB at 2.4 and 5 GHz
  - -15 dB from 500 MHz to 6 GHz
- Compliant with USB3.2 gen 2 eye diagram
- Small and thin package 1.5 x 1.7 x 0.5 mm
- RoHS compliant
- High reduction of parasitic elements through integration
- ESD protection compliant with IEC 61000-4-2 level 4 standards (8 kV contact)

Benefits

- Suppress the common mode noise but keep signal integrity
- Low PCB space consumption
- Save components count
- Make the application robust against ESD strikes from external environment

Applications

Consumer and computer electronics featuring USB3.2 such as:

- Mobile phones
- Notebook, laptop
- Portable devices
- PND

Description

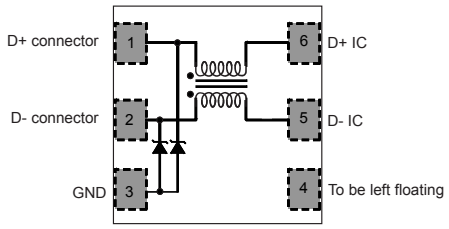
The ECMF02-2HSMX6 is a highly integrated common mode filter designed to suppress EMI/RFI common mode noise on high speed differential serial buses like USB3.2 transceiver.

1 Functional description

The ECMF02-2HSMX6 is an ESD protected common mode filter especially designed for USB3.2 Tx/Rx differential pair, for host and device. The USB3.2 is actually made of 3 differential pairs. The first differential pair supports the high speed USB mode (also called USB2.0 mode). The 2 other differential pairs are used to support the super speed USB mode in full duplex. Bit rate on super speed USB can reach 5 Gbps. The ECMF02-2HSMX6 is able to filter the common mode noise from 300 MHz to 6 GHz, helping to make the application compliant with the electromagnetic interference emission standard such as CISPR22 or FCC part 15, or EN55022 and avoiding antenna desense on mobile phones, WiFi/Bluetooth, GPS,/GNSS frequencies. At the same time, the ECMF02-2HSMX6 keeps the high speed signal integrity and provides an efficient ESD protection. More application information available in following AN:

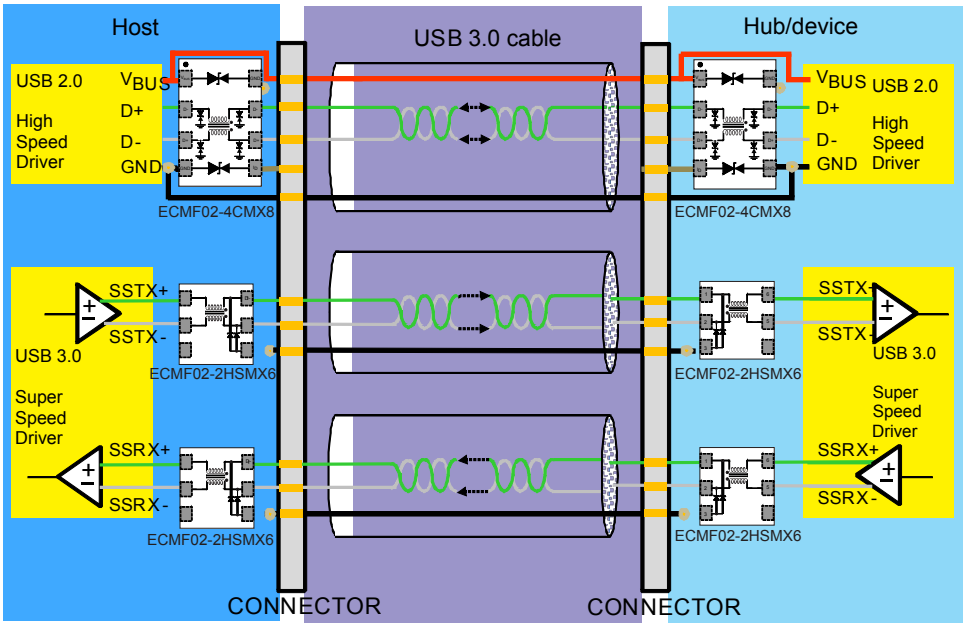
- Application Note AN4356: "Antenna desense on handheld equipment"
- Application Note AN4511: "Common Mode filters"
- Application Note AN4540: "MHL link filtering and protection"

Figure 1. Functional diagram



A typical application diagram is shown in Figure 2. ST offers a global approach to USB3.0 interface by providing a comprehensive range of dedicated products.

Figure 2. Typical application diagram



2 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge	 ±8 ±15	kV
I_{DC}	Maximum DC current		100	mA
T_{op}	Operating ambient temperature range		-55 to +125	°C
T_j	Maximum junction temperature		+125	
T_{stg}	Storage temperature range		-55 to +150	

Figure 3. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage at I_{PP}
I_{PP}	=	Peak pulse current
I_F	=	Forward current
V_F	=	Forward voltage

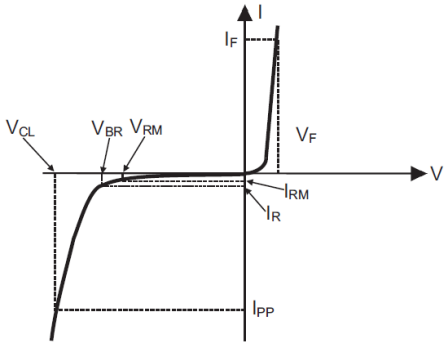


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3 V			100	nA
R_{DC}	DC serial resistance		7	9	Ω

2.1 Characteristics (curves)

Figure 4 shows that USB3.0 devices and cables can interfere with radio frequency devices operating between 700 MHz and 5 GHz.

Figure 4. USB3.2 frequency radiation measured with current loop

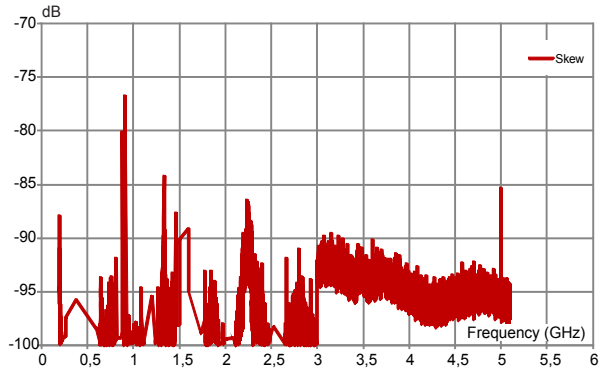


Figure 5. Differential and common mode impedance versus frequency

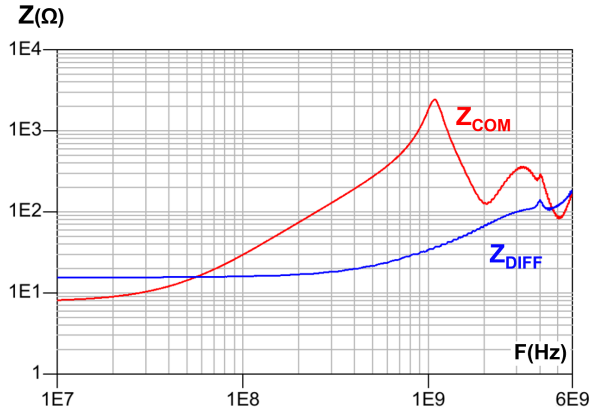


Figure 6. Differential attenuation versus frequency

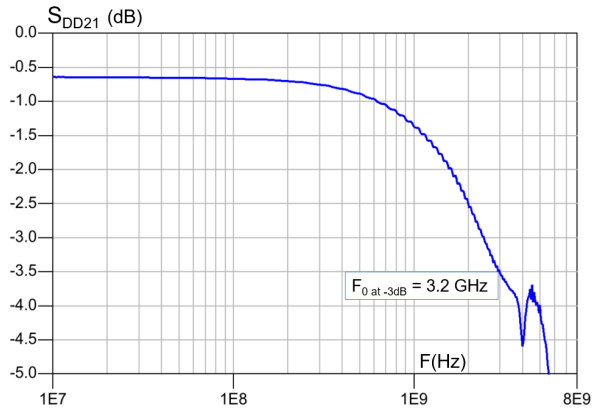


Figure 7. Common mode attenuation versus frequency

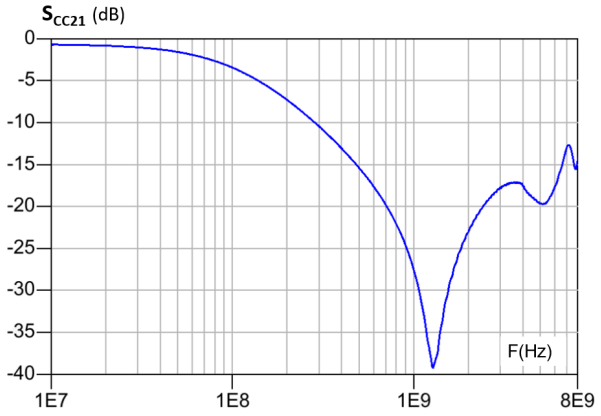


Figure 8. Return loss versus frequency ($Z_{0\ DIFF}$ = 100 Ω - S_{DD11})

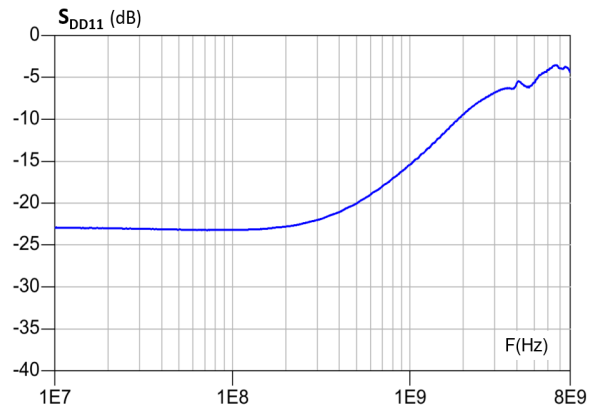


Figure 9. Return loss versus frequency ($Z_{0\ DIFF}$ = 100 Ω - S_{DD22})

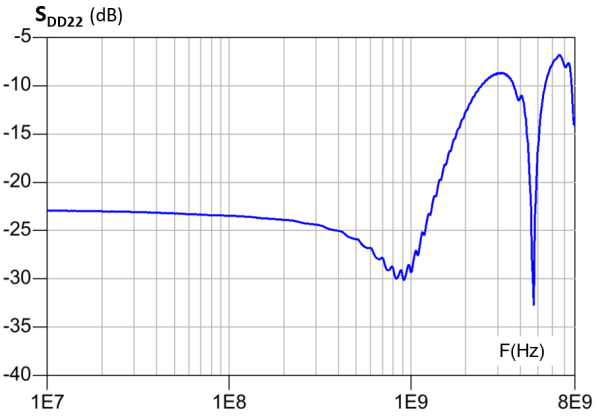


Figure 10. Typical ESD response to IEC 61000-4-2 +8kV contact

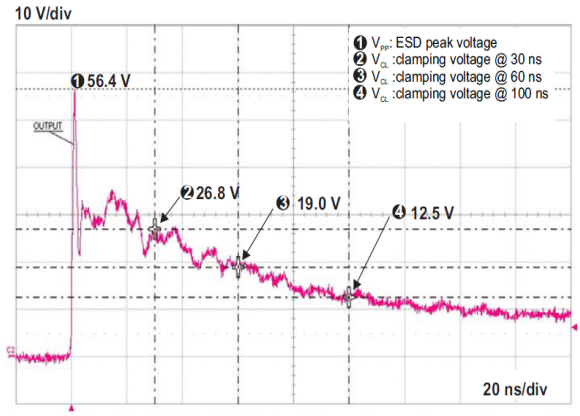


Figure 11. Typical ESD response to IEC 61000-4-2 -8kV contact

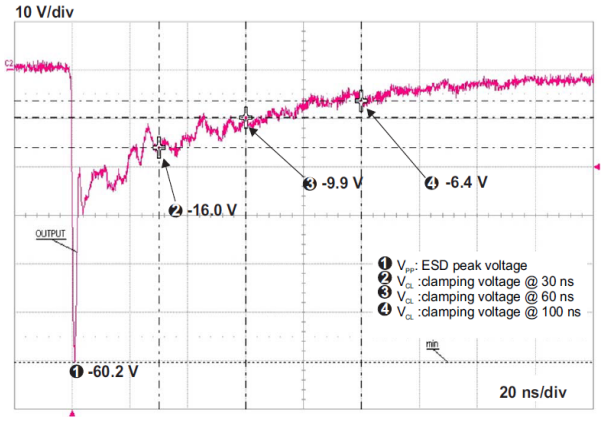


Figure 12. USB2.0 (480 Mbps) eye diagram without device

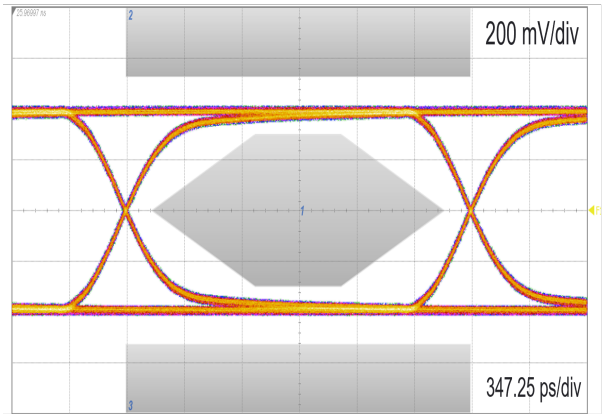


Figure 13. USB2.0 (480 Mbps) eye diagram with device

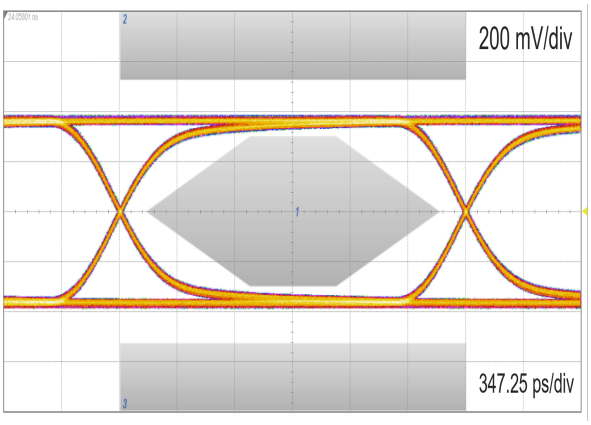


Figure 14. USB 3.2 Gen 1 - 5.0 Gbps eye diagram without ECMF02-2HSMX6 (with type C connector, reference cable and equalizer)

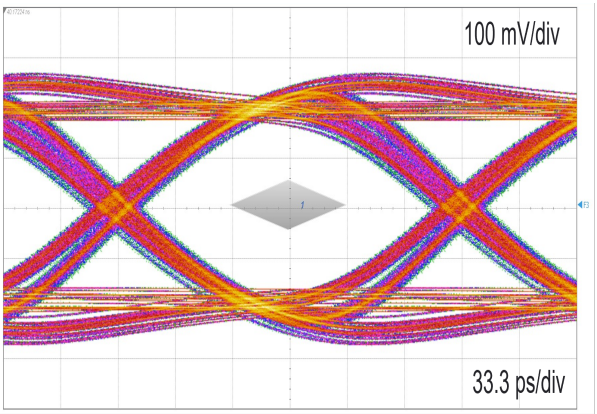


Figure 15. USB 3.2 Gen 1 - 5.0 Gbps eye diagram with ECMF02-2HSMX6 (with type C connector, reference cable and equalizer)

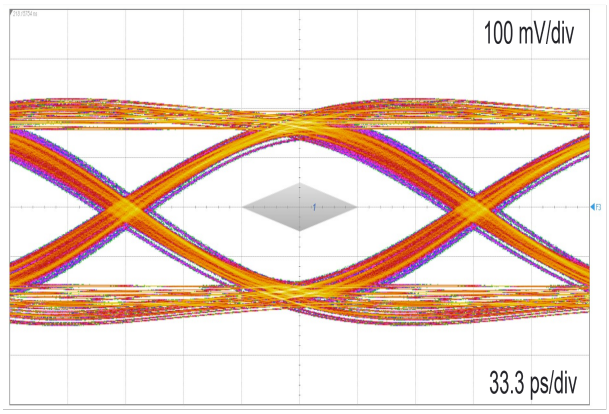


Figure 16. USB 3.2 Gen 2 - 10.0 Gbps eye diagram without ECMF02-2HSMX6 (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

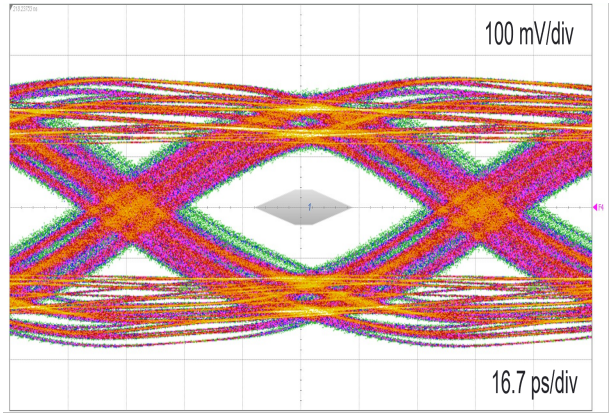


Figure 17. USB 3.2 Gen 2 - 10.0 Gbps eye diagram with ECMF02-2HSMX6 (with type C connector, reference cable, equalizer with ADC = 6 dB and DFE)

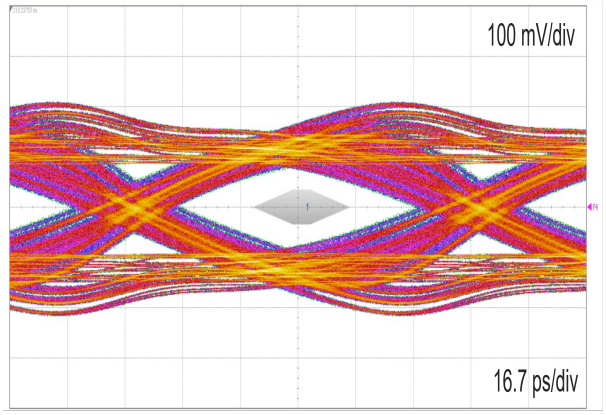


Figure 18. Display Port HBR2 5.4 Gbps eye diagram without ECMF02-2HSMX6

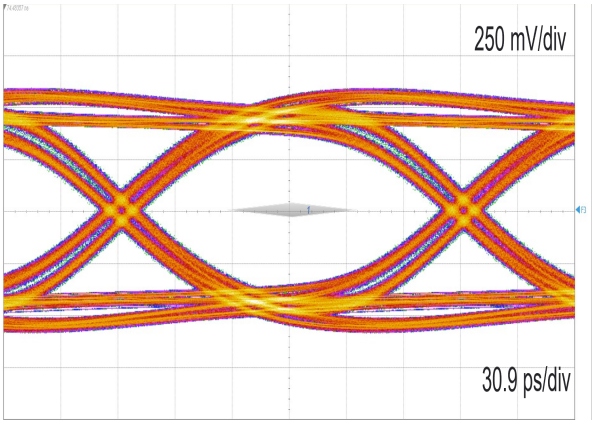
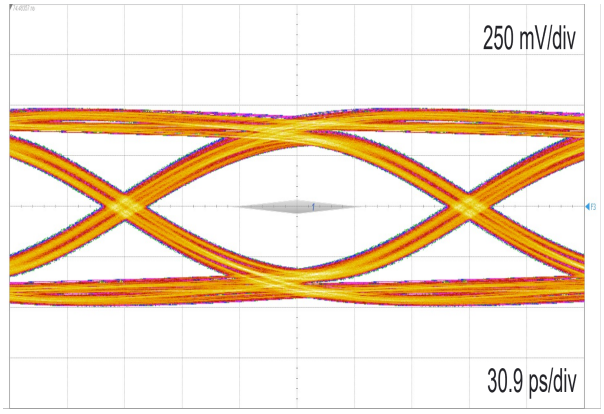


Figure 19. Display Port HBR2 5.4 Gbps eye diagram with ECMF02-2HSMX6



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 QFN-6L package information

Figure 20. QFN-6L package outline

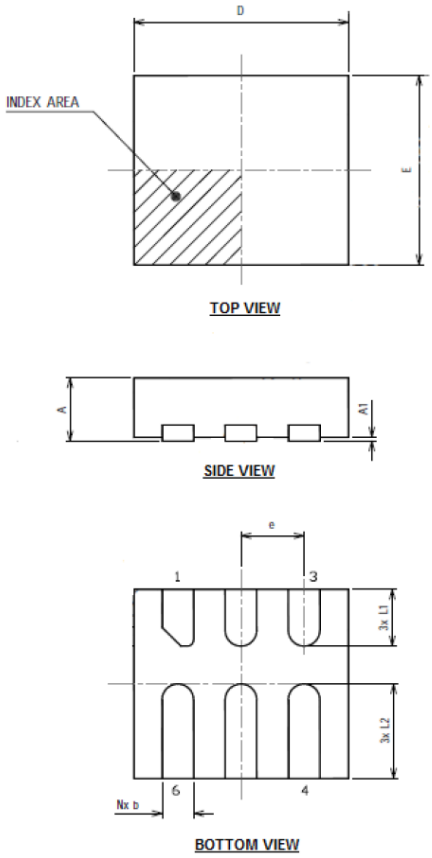
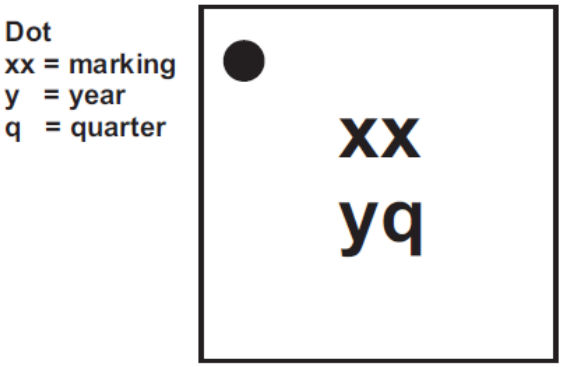


Table 3. QFN-6L mechanical data

Symbol	Dimesions (milimeters)		
	Min.	Typ.	Max.
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	1.65	1.70	1.75
E	1.45	1.50	1.55
e	0.45	0.50	0.55
L1	0.35	0.45	0.55
L2	0.65	0.75	0.85

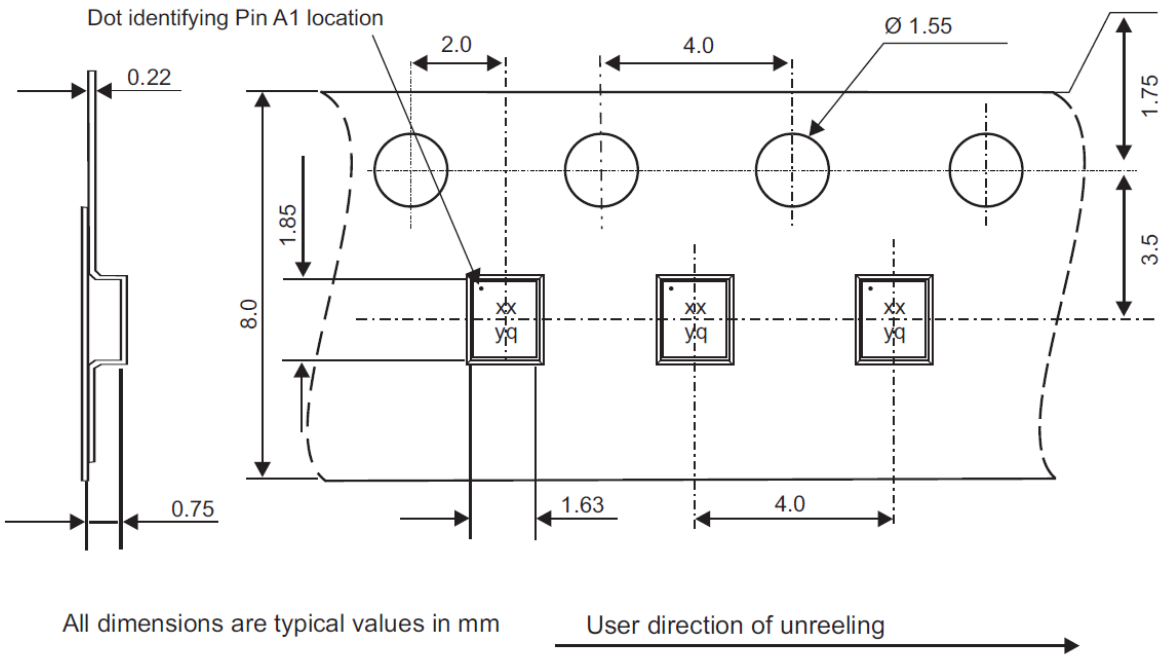
3.2 Packing information

Figure 21. **Marking**



Note: The marking can be rotated to differentiate assembly location. Refer to Table 4 for xx definition.

Figure 22. **Tape outline**

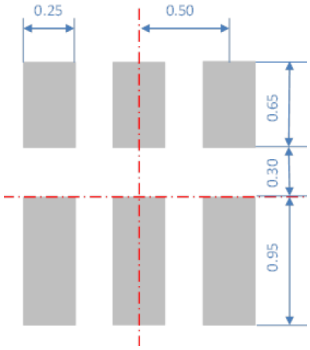


4 PCB assembly recommendation

4.1 Footprint

SMD footprint design is recommended.

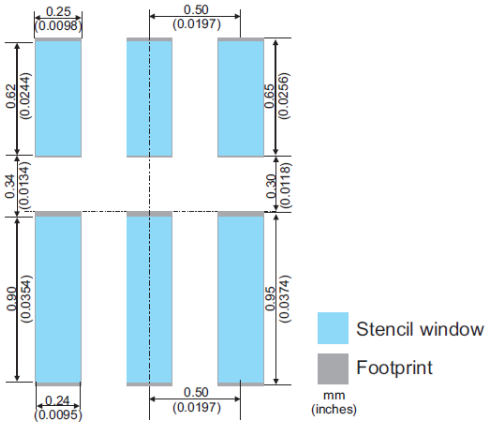
Figure 23. Footprint in mm



4.2 Stencil opening design

Stencil opening thickness: 100 µm

Figure 24. Stencil opening recommendations



4.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

4.4 Placement

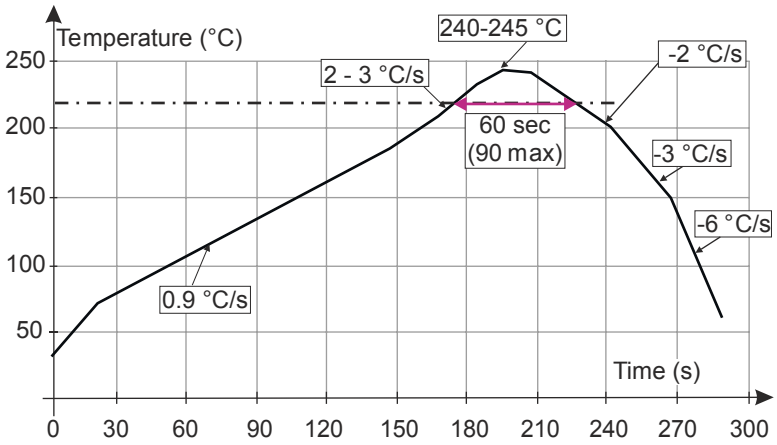
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm (25% offset allowed on the smallest dimension of the smallest pad) is recommended.
3. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

4.6 Reflow profile

Figure 25. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 26. **Ordering information scheme**

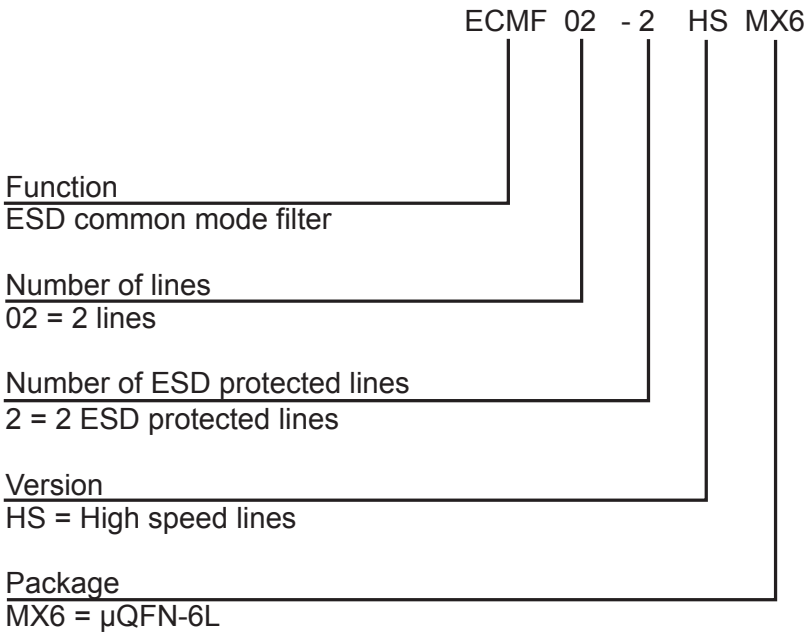


Table 4. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
ECMF02-2HSMX6	KR	µQFN-6L	3.4 mg	3000	Tape and reel

Revision history

Table 5. **Document revision history**

Date	Version	Changes
13-Nov-2013	1	Initial release.
25-Aug-2014	2	Inserted Figure 10: Differential (ZDD21) and common mode (ZCC21) impedance versus frequency.
13-Dec-2017	3	Updated Table 1.
20-Dec-2021	4	Updated title description, Section 2.1 Characteristics (curves) and removed PCB layout chapter. Minor text changes.

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