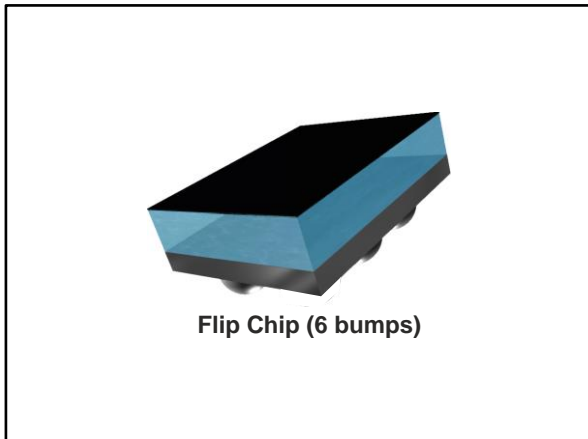


## Wide band directional coupler with ISO port

Datasheet - production data



Flip Chip (6 bumps)

**Description**

The CPL-WBF-00D3 is a low band coupler designed to measure RF antenna output power in GSM / WCDMA / TD-SCDMA / LTE applications. This coupler has been customized for wide band operating frequencies (EGSM, CELL, PCS, DCS, TD-SCDMA, WCDMA and LTE) with less than 0.30 dB insertion losses in the bandwidth (698 MHz to 2700 MHz).

The CPL-WBF-00D3 has been designed using STMicroelectronics IPD (integrated passive device) technology on non-conductive glass substrate to optimize RF performance. The device is delivered 100% tested, in tape and reel.

**Features**

- 50  $\Omega$  nominal input / output impedance
- Wide operating frequency range (698 MHz to 2700 MHz)
- Low insertion loss
- 30 dB coupling factor with high flatness
- High directivity
- High ESD robustness (IEC 61000-4-2 level 4)
- Flip Chip package
- Small footprint

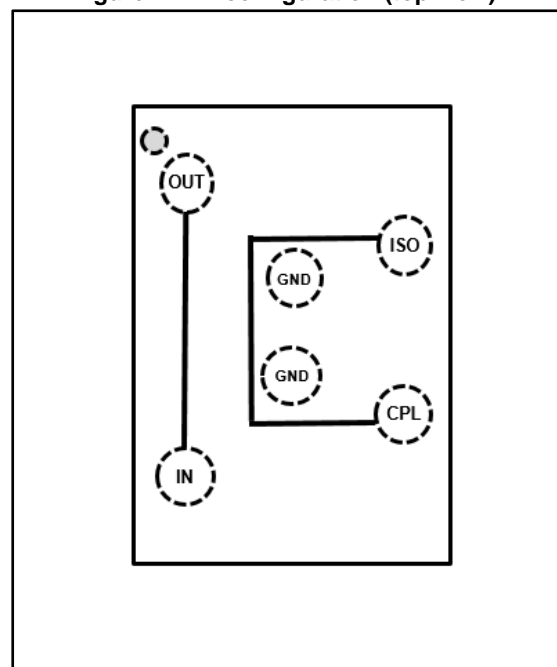
**Benefits**

- Very low profile (less than 560  $\mu\text{m}$  thickness after reflow)
- Lead-free package
- High RF performance
- RF module size reduction
- 50  $\Omega$  nominal input / output impedance
- Fully symmetrical design

**Applications**

- Quad-band power amplifier module
- Quad-band front end module
- GSM / WCDMA / LTE mobile phone

Figure 1: Pin configuration (top view)



# 1 Characteristics

**Table 1: Absolute maximum ratings (limiting values)**

Symbol	Parameter	Frequency band	Test condition	Value			Unit
				Min.	Typ.	Max.	
P <sub>IN</sub>	Input power RF <sub>IN</sub>	CW	698-880		-	30	dBm
		DC 50% CW	880-915		-	35	
		CW	1428-1661		-	30	
		DC 50% CW	1710-1910		-	33	
		CW	1920-2170		-	27	
		CW	1920-2025		-	30	
		CW	2500-2700		-	30	
V <sub>ESD</sub>	ESD ratings IEC61000-4-2 (C = 150 pF, R = 330 Ω, 10 shots with both polarities and each condition, cumulative method) RF <sub>IN</sub> , RF <sub>OUT</sub> , air discharge RF <sub>IN</sub> , RF <sub>OUT</sub> , contact discharge			±15 ±8	-		kV
V <sub>ESD(HBM)</sub>	Human body model, JESD22-A114-B, all I/O			500	-		V
V <sub>ESD(MM)</sub>	Machine model, JESD22-A115-A, all I/O			50	-		V
V <sub>ESD(CDM)</sub>	Charge device model, JESD22-C101-C, all I/O			500	-		
T <sub>OP</sub>	Operating temperature			-40	-	+85	°C

**Table 2: Electrical characteristics (T<sub>amb</sub> = 25 °C) – impedances**

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
Z <sub>OUT</sub>	Nominal output impedance	-	50	-	Ω
Z <sub>IN</sub>	Nominal input impedance	-	50	-	Ω
Z <sub>CPLD</sub>	Nominal coupling impedance	-	50	-	Ω
Z <sub>ISO</sub>	Nominal isolated port impedance	-	50	-	Ω

**Table 3: Electrical characteristics (T<sub>amb</sub> = 25 °C) – RF performance**

Symbol	Parameter		Value			Unit
			Min.	Typ.	Max.	
f	Frequency range (bandwidth)		698		2700	MHz
I <sub>L</sub>	Insertion loss in bandwidth	From 698 MHz to 2700 MHz		0.15	0.3	dB
RL	Return loss in bandwidth		15			
C <sub>PLD</sub>	Coupling factor		29		33	
DIR	Coupler directivity		20			

### 1.1 RF measurements

Warning: This device is tailored for custom SiP module and has been optimized in terms of performance for SiP module custom layout. In order to guarantee the integrity of the device, below measurements have been done on ST internal board, which may be different from customer application SiP layout.

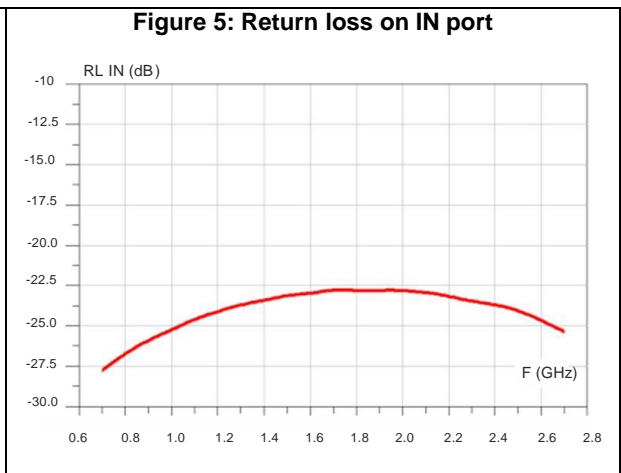
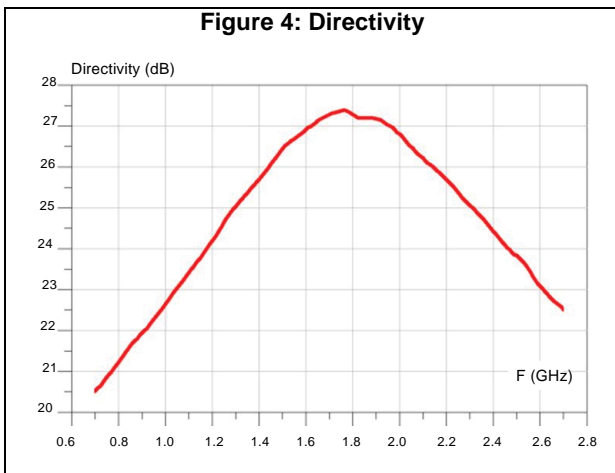
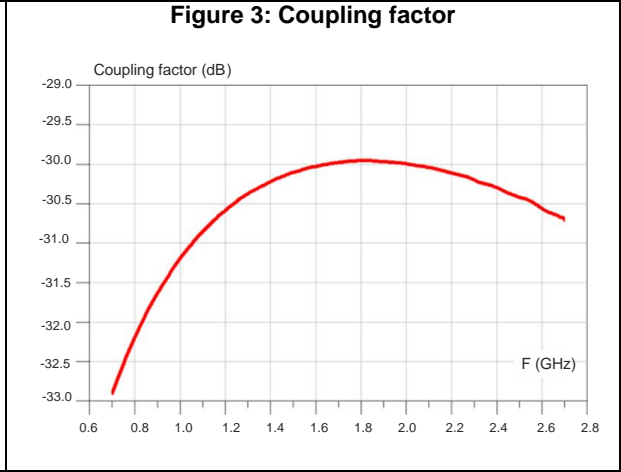


Figure 6: Return loss on OUT port

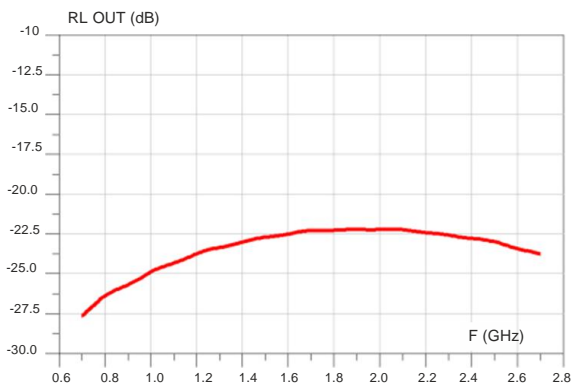


Figure 7: Return loss CPL port

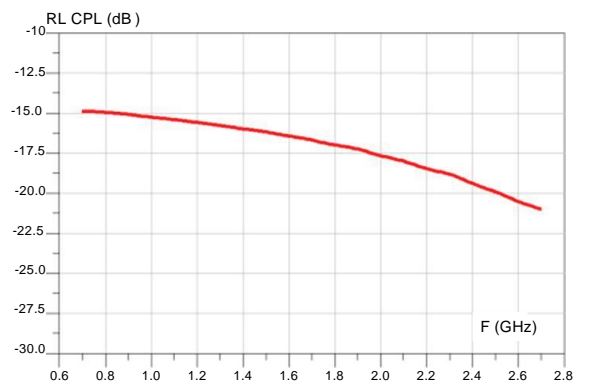
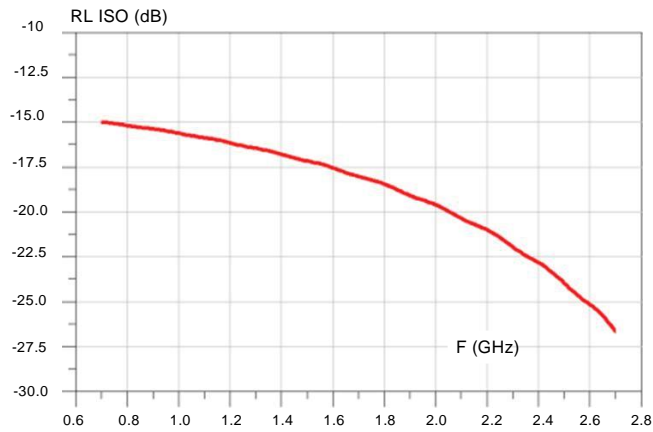


Figure 8: RL ISO



## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 2.1 Flip-Chip 6 bumps package information

Figure 9: Flip-Chip 6 bumps package outline

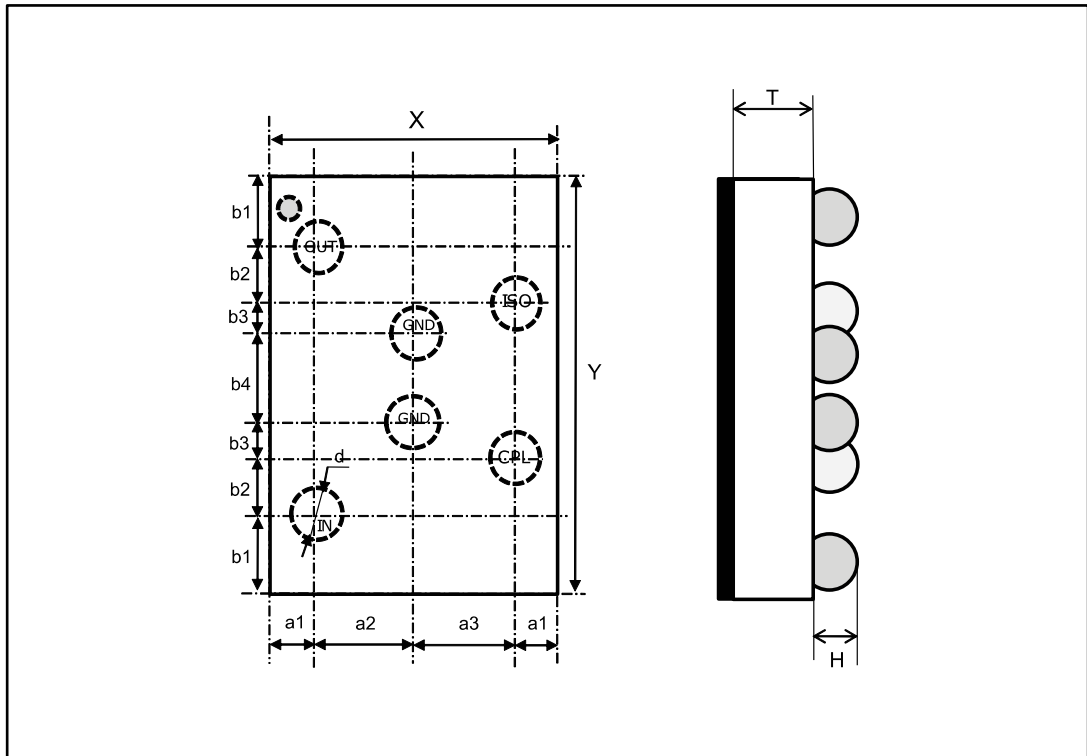


Table 4: Flip-Chip 6 bumps package mechanical data

Parameter	Description	Min.	Typ.	Max.	Unit
X	X dimension of the die	1060	1110	1160	μm
Y	Y dimension of the die	1850	1900	1950	
a1	Distance from edge of die to IN/OUT bumps and CPL/ISO bumps on X axis		218		
a2	Distance from IN/OUT bumps to GND bumps on X axis		274		
a3	Distance from GND bumps to CPL/ISO bumps on X axis		400		
b1	Distance from edge of die to IN/OUT bumps on Y axis		218		
b2	Distance from IN/OUT bumps to CPL/ISO bumps on Y axis		432		
b3	Distance from CPL/ISO bumps to GND bumps on Y axis		100		
b4	Distance between GND bumps on Y axis		400		
d	Bump diameter	240	255	270	
T	Substrate thickness	380	400	420	
H	Bump height	190	205	220	

## 2.2 Flip-chip 6 bumps packing information



More packing information is available in the technical note: TN1200: "IPAD™, micro-bump Flip chip: package description and recommendations for use"

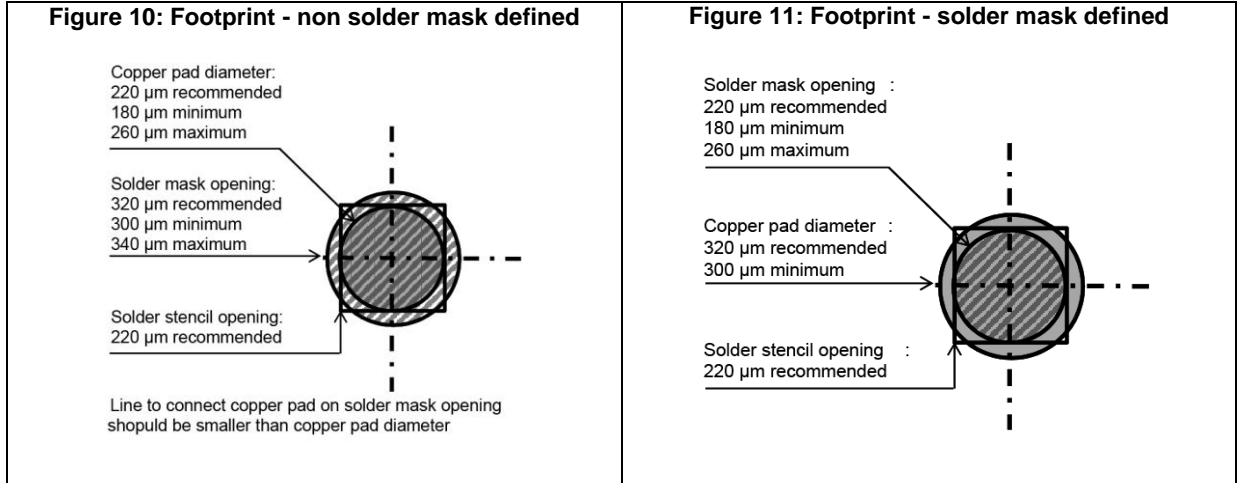


Figure 12: Marking

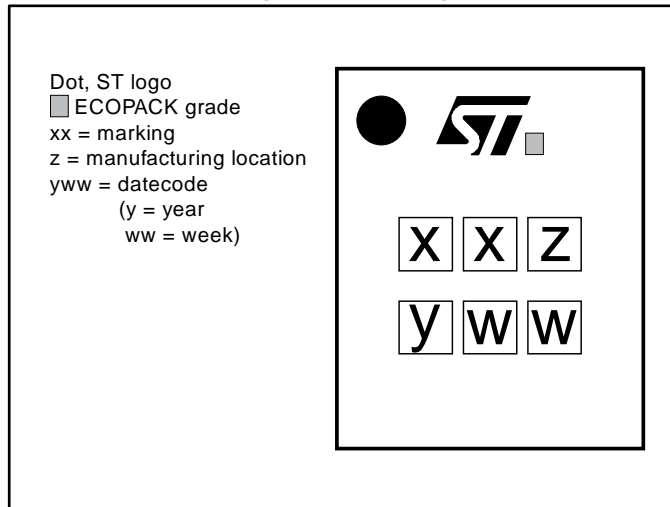


Figure 13: Top View land pattern recommendations

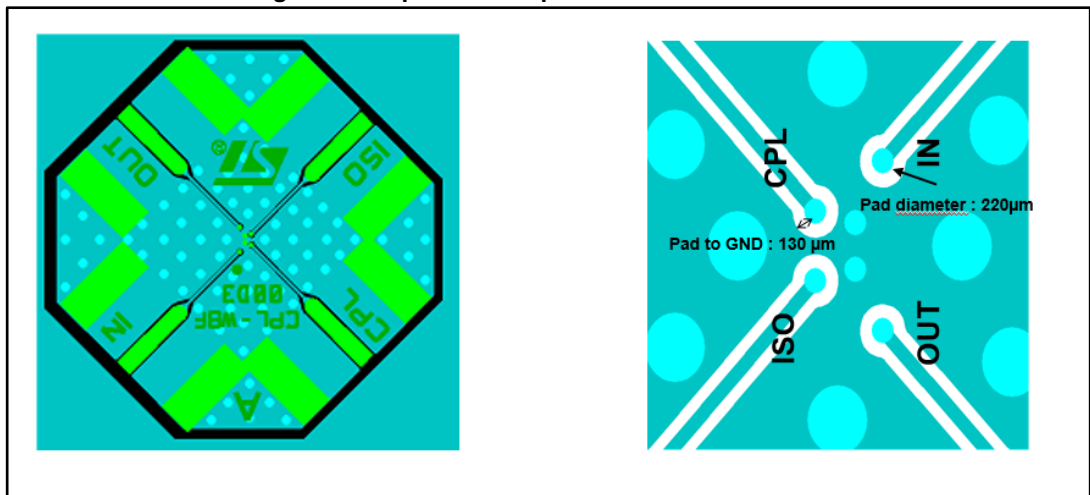
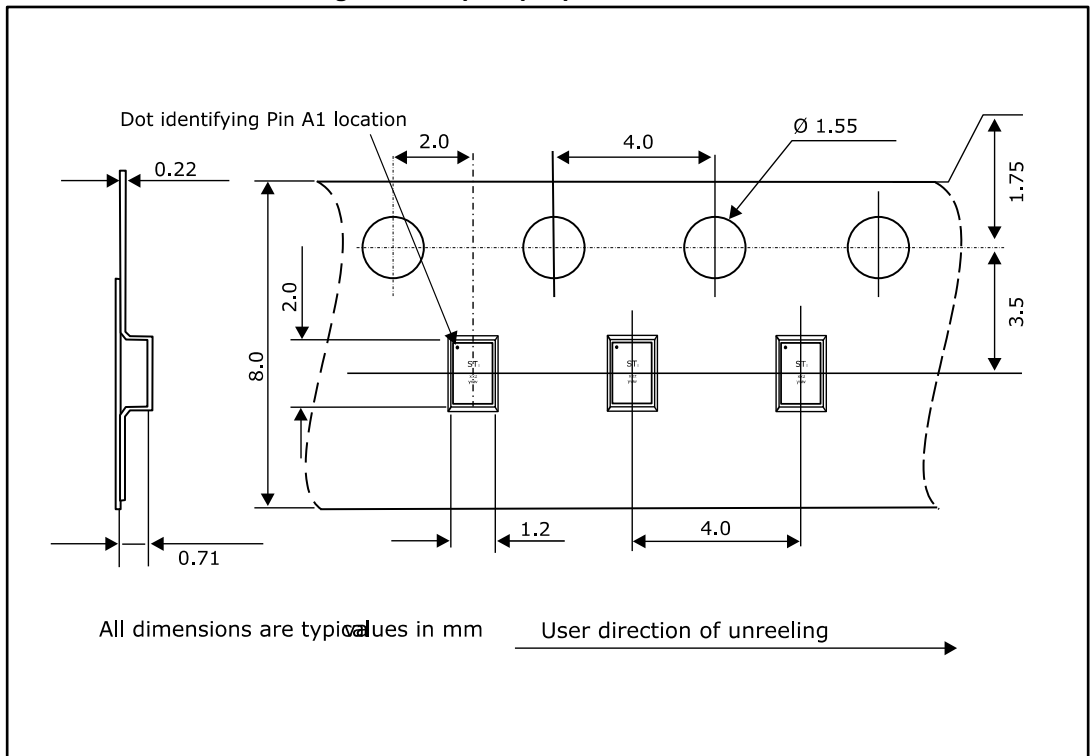


Figure 14: Flip-chip tape and reel outline





### 3 Ordering information

Table 5: Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
CPL-WBF-00D3	SD	Flip-Chip	2.35 mg	5000	Tape and reel (7")

### 4 Revision history

Table 6: Document revision history

Date	Revision	Changes
09-Jan-2013	1	Initial release.
09-Aug-2013	2	Updated footprint graphics.
05-Feb-2018	3	Updated <i>Figure 1: "Pin configuration (top view)"</i> , <i>Figure 9: "Flip-Chip 6 bumps package outline"</i> , <i>Figure 13: "Top View land pattern recommendations"</i> . Added <i>Table 4: "Flip-Chip 6 bumps package mechanical data"</i> .

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