Single line low capacitance Transil™, transient surge voltage suppressor (TVS) for ESD protection
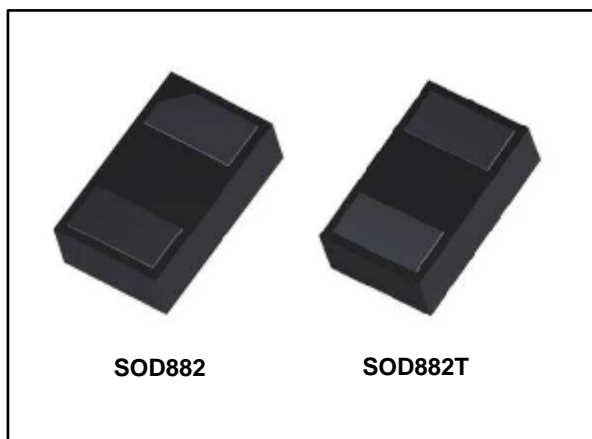
Datasheet - production data

SOD882 **SOD882T**

Features

- Single line bidirectional protection
- Breakdown voltage V_{BR} = 8.5 V min.
- Very low capacitance = 4.5 pF at 0 V
- Lead-free packages
- ECOPACK®2 compliant packages

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Benefits

- Very low capacitance for optimized data integrity
- Very low reverse current < 50 nA
- Low PCB space consumption: 0.6 mm² max.
- High reliability offered by monolithic integration

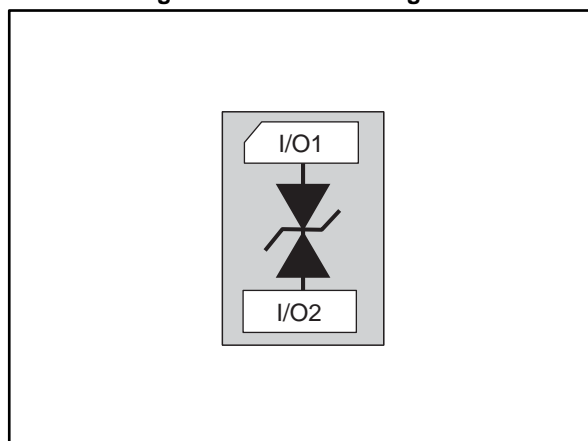## Complies with the following standards

- IEC 61000-4-2 (exceeds level 4)
  - 17 kV (air discharge)
  - 17 kV (contact discharge)
- MIL STD 883G - Method 3015-7: class 3
  - Human body model

Description

The ESDAVLC8-1BM2 (SOD882) and ESDAVLC8-1BT2 (SOD882T) are bidirectional single-line TVS diodes designed to protect data lines or other I/O ports against ESD transients.

These devices are ideal for applications where both printed circuit board space and power absorption capability are required.

Figure 1: Functional diagram

I/O1

I/O2

TM: Transil is a trademark of STMicroelectronics

This is information on a product in full production.

www.st.com

1   Characteristics

Table 1: Absolute maximum ratings (T$_{amb}$ = 25 °C)

Symbol	Parameter		Value	Unit
V$_{PP}$	Peak pulse voltage	IEC 61000-4-2: Contact discharge Air discharge MIL STD 883G - Method 3015-7: class 3	17 17 25	kV
P$_{PP}$	Peak pulse power	8/20µs, T$_j$ initial = T$_{amb}$	30	W
I$_{PP}$	Peak pulse current	8/20µs	1.3	A
T$_{OP}$	Operating junction temperature range		-55 to +150	°C
T$_{stg}$	Storage temperature range		-65 to +150	
T$_L$	Maximum lead temperature for soldering during 10 s		260	

Figure 2: Electrical characteristics (definitions)
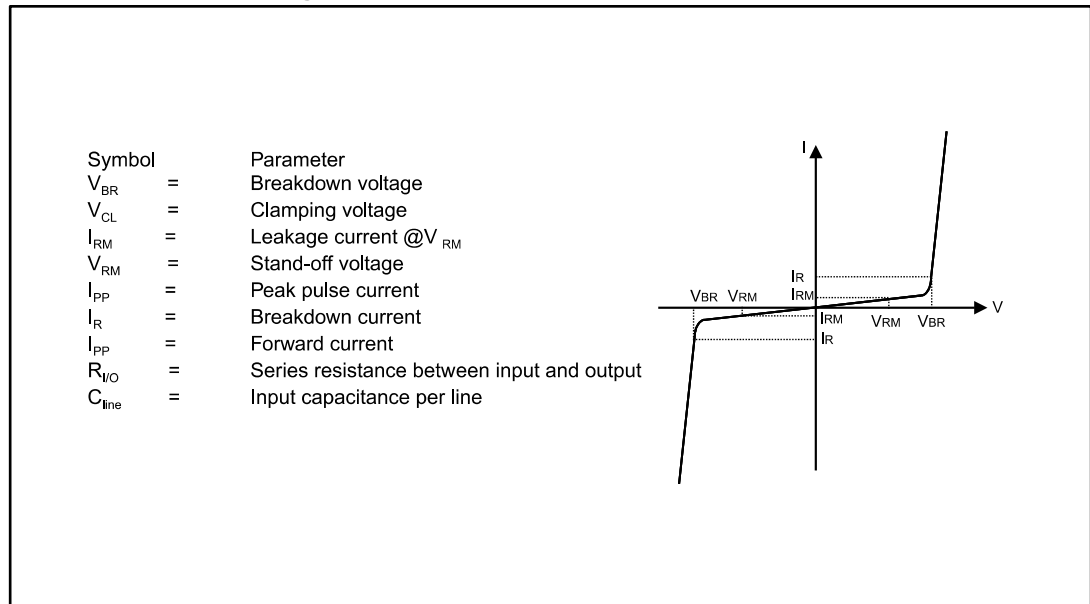
Table 2: Electrical characteristics (T$_{amb}$ = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V$_{BR}$	From I/O1 to I/O2, I$_R$ = 1 mA direct	14.5	17		V
	From I/O2 to I/O1, I$_R$ = 1 mA reverse	8.5	11		
I$_{RM}$	V$_{RM}$ = 3 V			50	nA
R$_d$	Square pulse, I$_{PP}$ = 1 A, t$_P$ = 2.5 µs		2		Ω
C$_{line}$	F = 1 MHz, V$_R$ = 0 V		4.5	5.5	pF

Characteristics (curves)

Figure 3: Relative variation of peak pulse power versus initial junction temperature
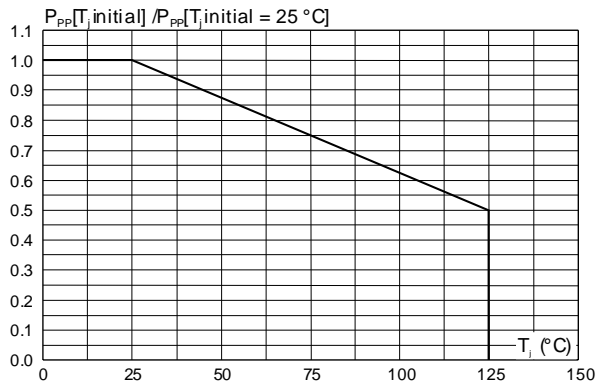

Figure 4: Junction capacitance versus reverse voltage applied (typical values, direct and reverse)
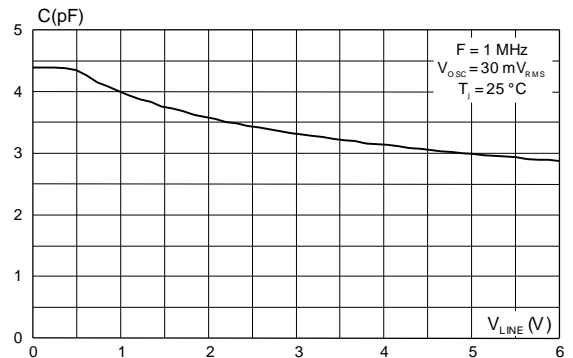

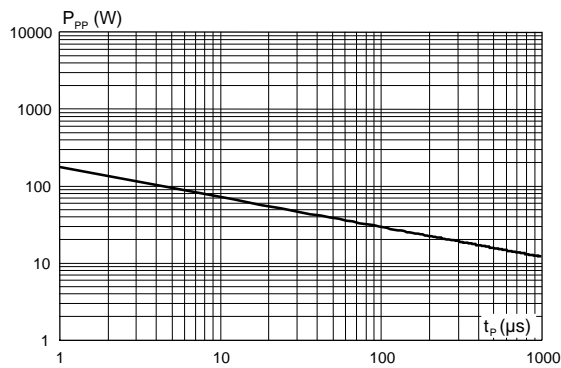**Figure 5: Peak pulse power versus exponential pulse duration (direct)**

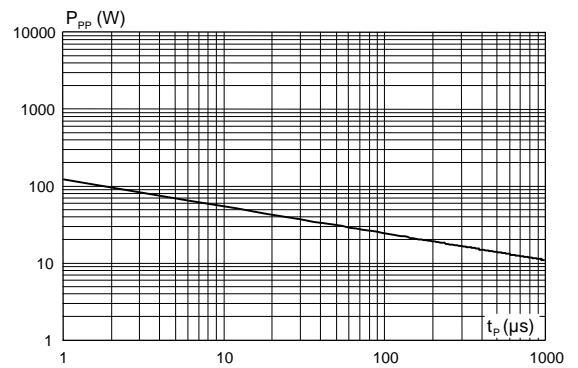**Figure 6: Peak pulse power versus exponential pulse duration (reverse)**

Figure 7: Clamping voltage versus peak pulse current (typical values, exponential waveform, direct)
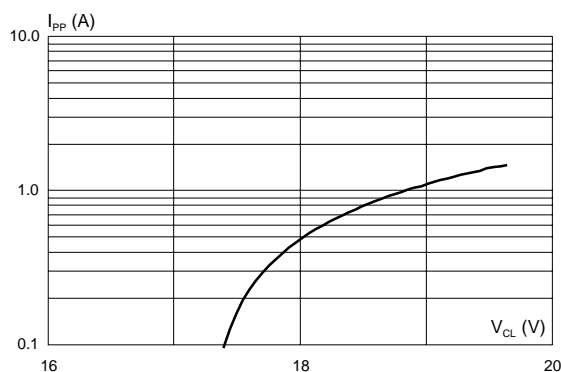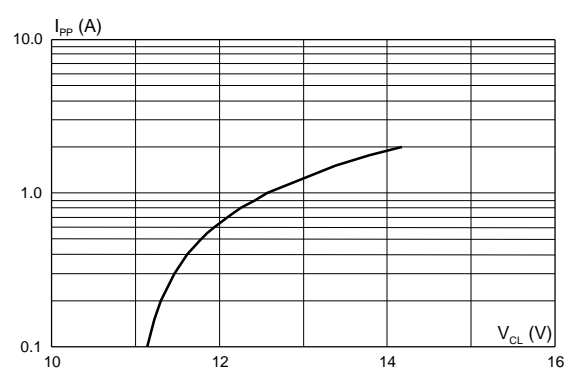

Figure 8: Clamping voltage versus peak pulse current (typical values, exponential waveform, reverse)

Figure 9: Relative variation of leakage current versus junction temperature (direct)
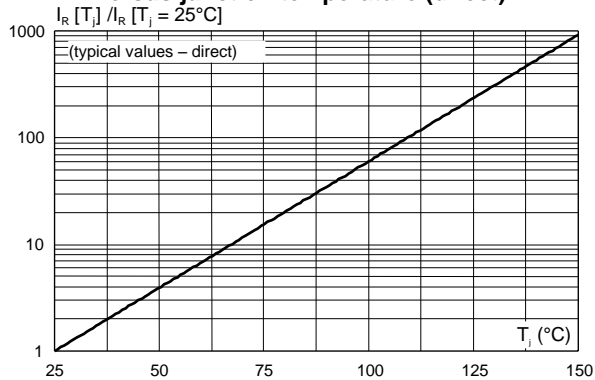

Figure 10: Relative variation of leakage current versus junction temperature (reverse)
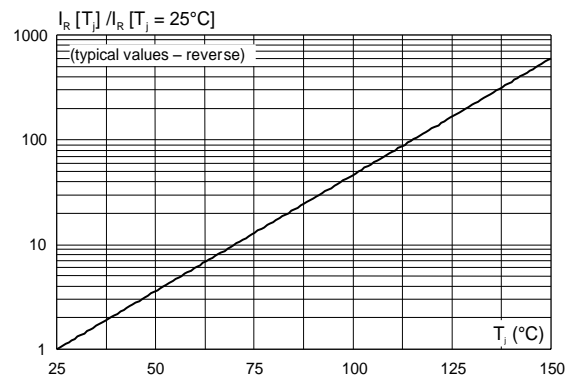

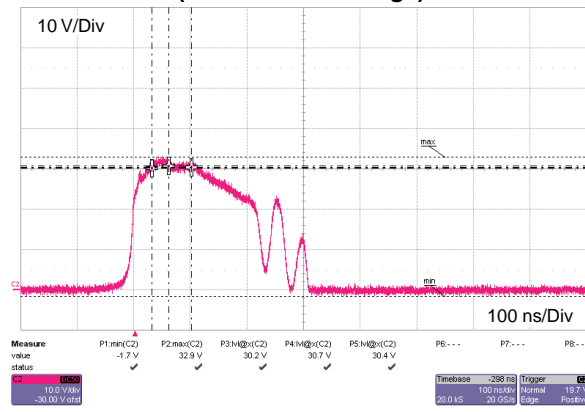**Figure 11: ESD response to IEC 61000-4-2 (+15 kV air discharge)**

Figure 12: ESD response to IEC 61000-4-2 (-15 kV air discharge)
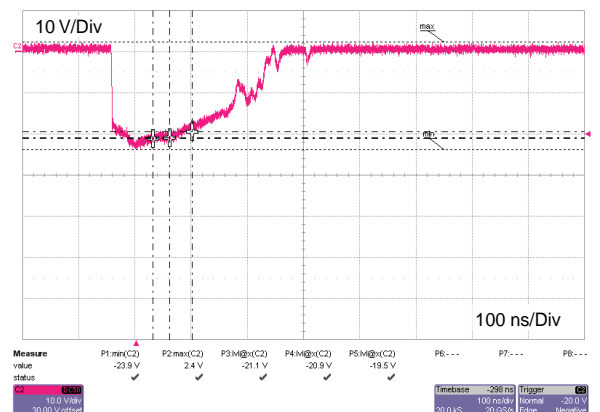

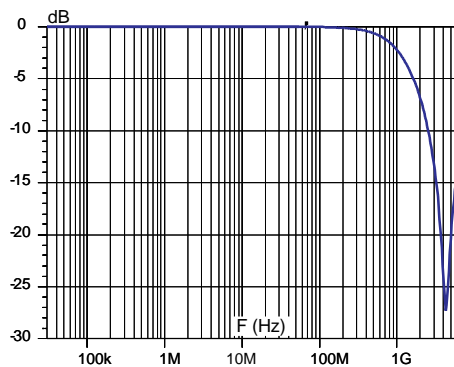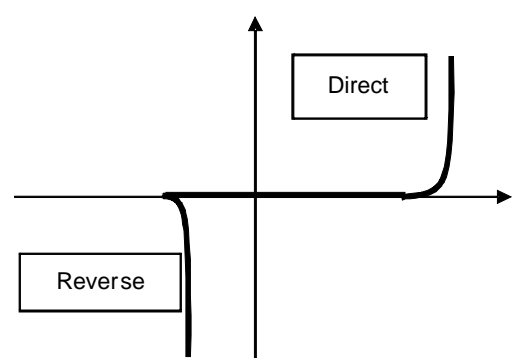**Figure 13: S21 attenuation measurement result**

Figure 14: Static characteristic

2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

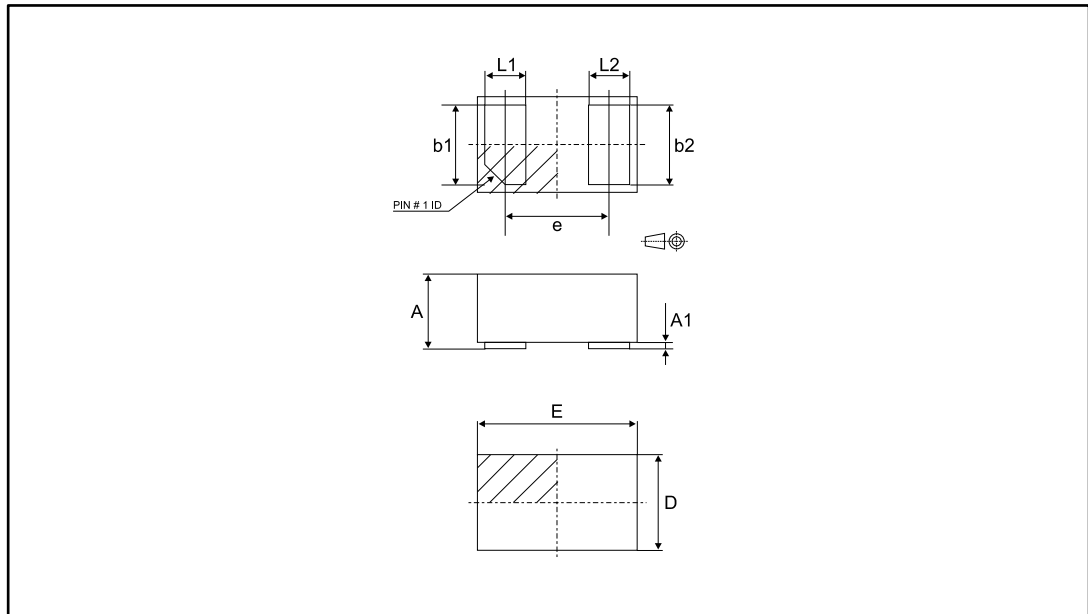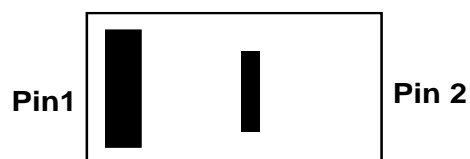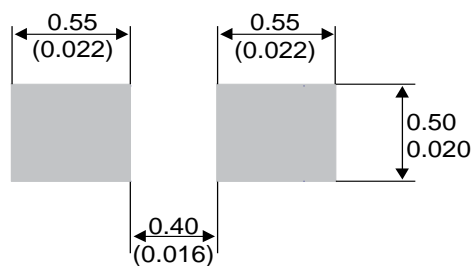## 2.1 SOD882 package information

Figure 15: SOD882 package outline

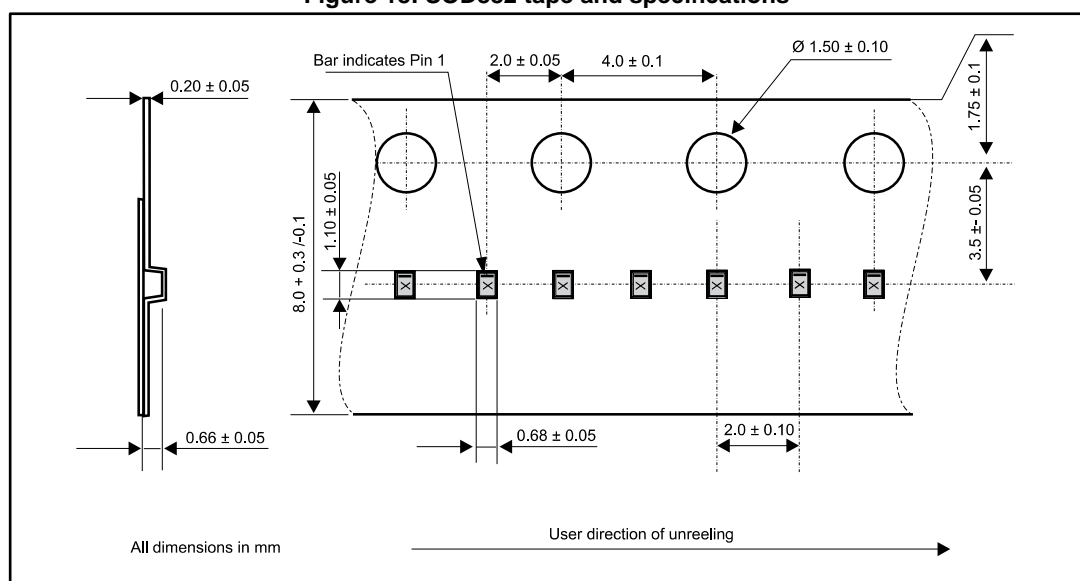

Table 3: SOD882 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 16: Footprint recommendations, dimensions in mm (inches)

Figure 17: Marking

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 18: SOD882 tape and specifications

2.2   SOD882T package information
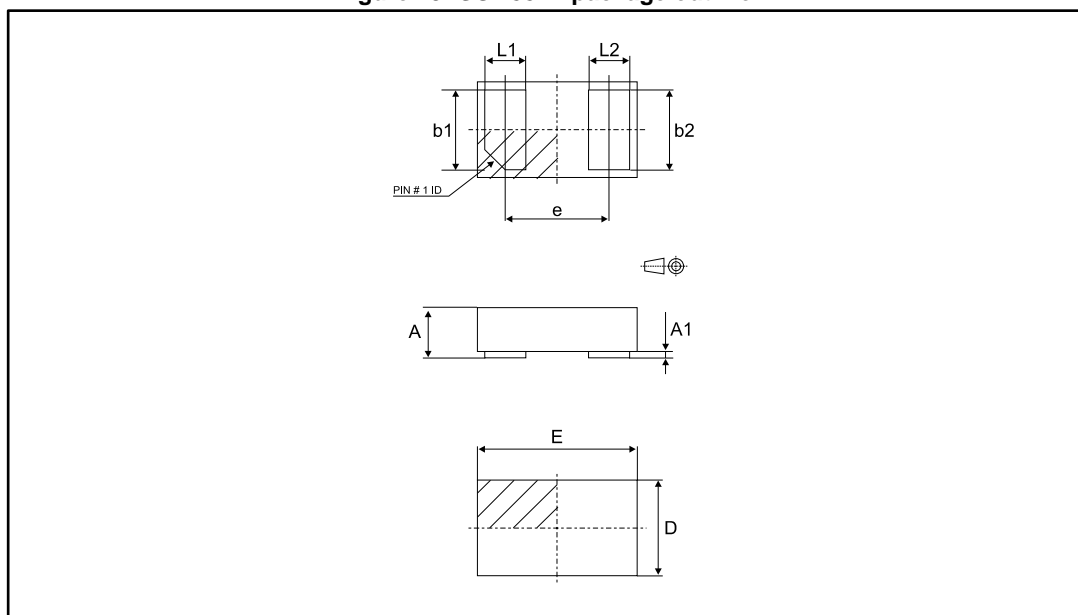
Figure 19: SOD882T package outline

Table 4: SOD882T package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.55	0.60	0.65	0.022	0.024	0.026
E	0.95	1.00	1.05	0.037	0.039	0.041
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

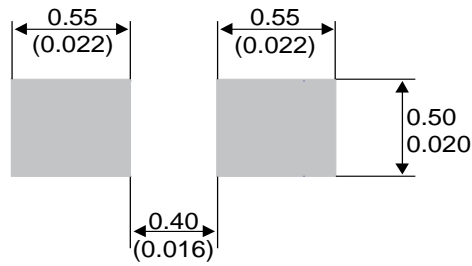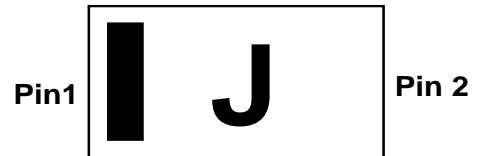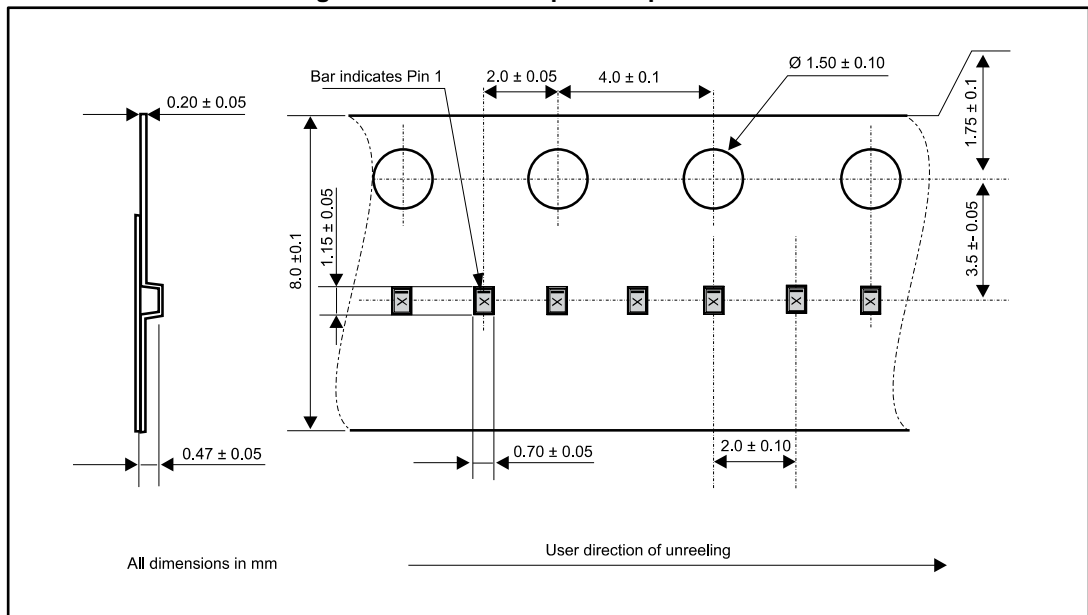**Figure 20: Footprint recommendations, dimensions in mm (inches)**

Figure 21: Marking

Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 22: SOD882T tape and specifications

3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$

   c. Aspect area = $\frac{L \times W}{2T(L+W)} \geq 0.66$

3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c. Stencil opening for leads: Opening to footprint ratio is 90%.
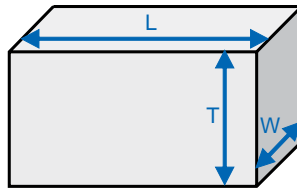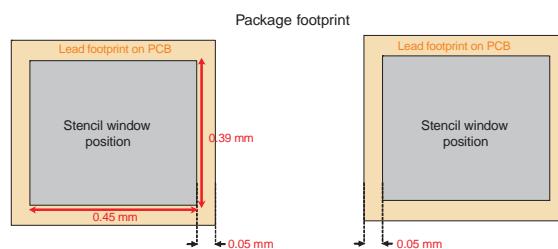
Figure 23: Stencil opening dimensions

Figure 24: Recommended stencil window position in mm (inches)

3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3   Placement

1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4   PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5   Reflow profile

Figure 25: ST ECOPACK® recommended soldering reflow profile for PCB mounting
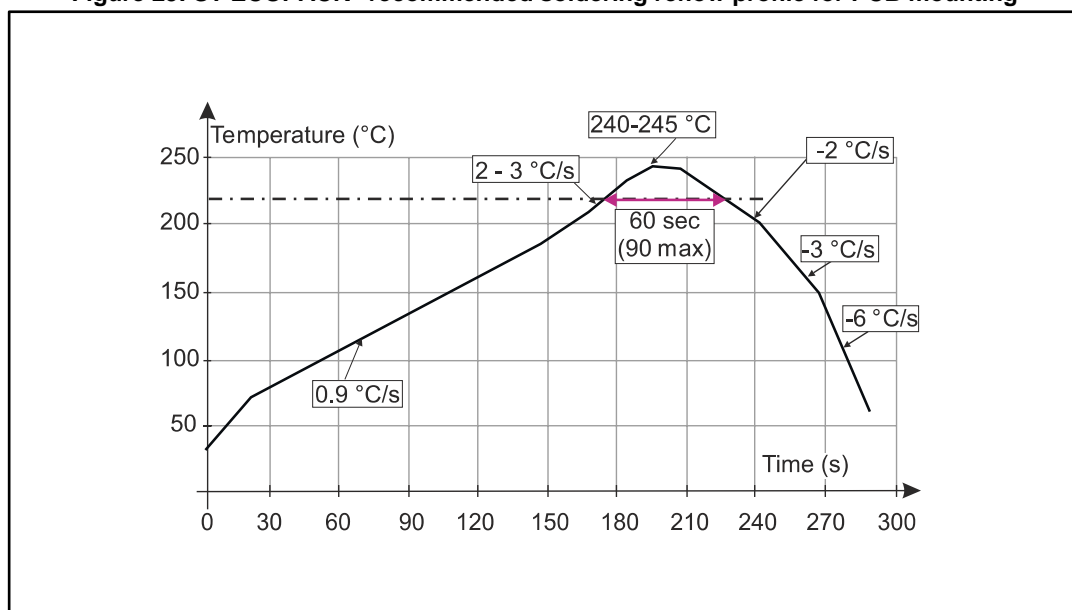
Minimize air convection currents in the reflow oven to avoid component movement.

Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4   Ordering information

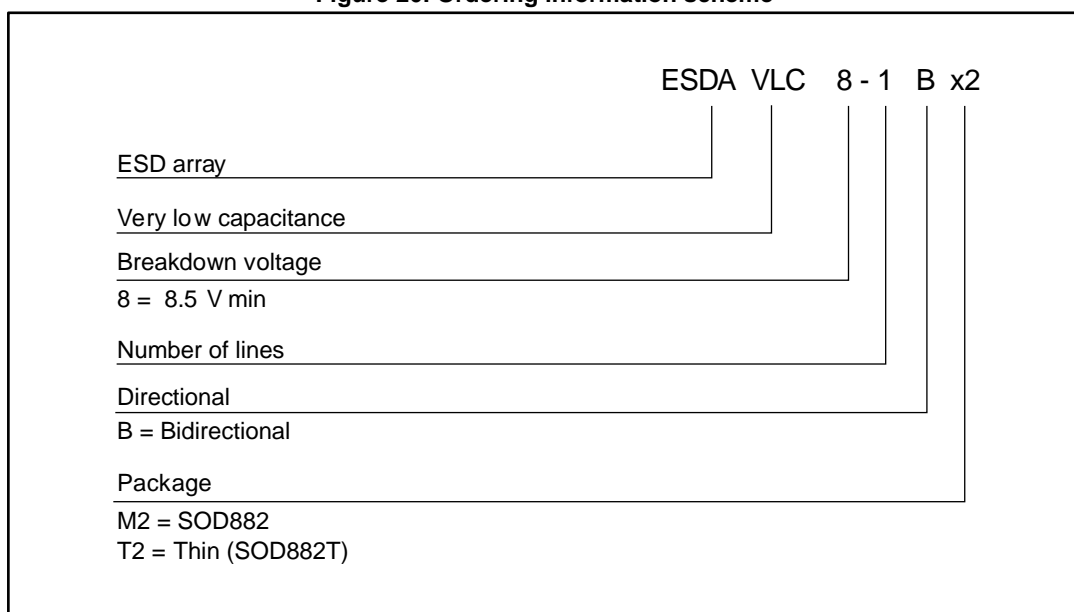**Figure 26: Ordering information scheme**

Table 5: Ordering information

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
ESDAVLC8-1BM2	I	SOD882	0.92 mg	12000	Tape and reel
ESDAVLC8-1BT2	J	SOD882T	0.76 mg	12000	Tape and reel

Notes:

[1]The marking can be rotated by multiples of 90° to differentiate assembly location

5   Revision history

Table 6: Document revision history

Date	Revision	Changes
22-Jan-2010	1	Initial release.
08-Jun-2012	2	Updated *Figure 11, Figure 12, Figure 16, Figure 19, Figure 20*, and added *Figure 23*. Updated *Table 3* and *Table 4*. Updated note on page 7, 8 and 13..
18-Nov-2016	3	Cover image updated.

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[ESDAVLC8-1BM2](#) [ESDAVLC8-1BT2](#)