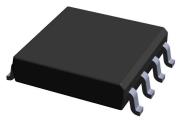
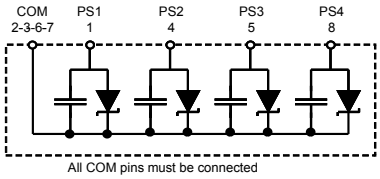
PEP01-5841

Datasheet

Quad 58 V TVS for PoE supplies in SO-8



SO-8



Features

- Peak pulse power: up to 2.7 kW (8/20 µs)
- Stand-off voltage: 58 V
- 4 unidirectional Transils and 4 decoupling capacitances
- Low clamping voltage: 100 V
- Low leakage current:
  - 0.2 µA at 25 °C
  - 1 µA at 85 °C
- Operating T_j max.: 150 °C
- JEDEC registered package outline

Complies with the following standards

- IEC61000-4-2 level
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)
- IEC61000-4-5 level 2
  - ±1 kV 42 Ω
- IEEE 802.3af-2003
- IEEE 802.3at-2008

Product status link
PEP01-5841

Description

The PEP01-5841 has been designed to protect power over Ethernet PSE equipment against line overvoltages. It embeds 4 decoupling capacitors to stabilize power supplies.

It is compatible with IEEE 802.3af-2003 and IEEE 802.3at-2008 requirements and it allows PoE based systems to be protected against both electrical overstress (EOS) and electrostatic discharges (ESD) according to IEC61000-4-5 and IEC61000-4-2.

The low clamping voltage (100 V) makes it compatible with PMOS and PSE controller technologies. Developed in Planar technology, it provides high reliability level.

Packaged in SO-8, it minimizes PCB consumption (footprint in accordance with the IPC 7531 standard).

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	Peak pulse voltage (IEC61000-4-2 contact discharge)	30	kV
P_{PP}	Peak pulse power dissipation	T_j initial = T_{amb}	2700	W
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Figure 1. Electrical characteristics - parameter definitions

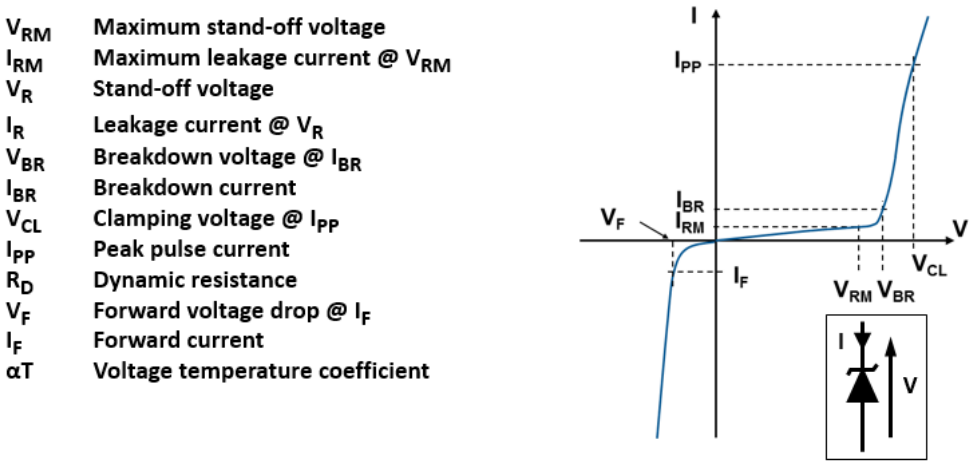


Figure 2. Pulse definition for electrical characteristics

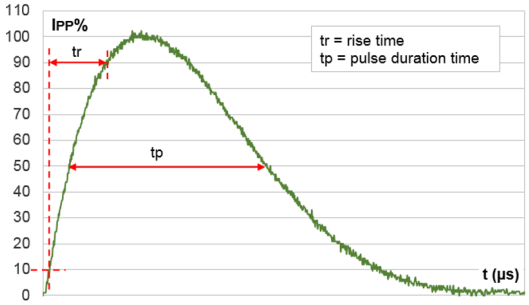


Table 2. Electrical characteristics - parameter values (T_{amb} = 25 °C, unless otherwise specified)

Type	I_{RM} max at V_{RM}			V_{BR} at I_{BR} (1)				8 / 20µs			C	αT
								V_{CL} (2)(3)	I_{PP}	R_D		
	25 °C	85 °C		Min.	Typ.	Max.		Max.		Max.	Typ.	Max.
	µA		V	V			mA	V	A	Ω	pF	10^{-4}/°C
PEP01-5841	0.2	1	58	64.4	67.8	71.2	1	100	24	1.2	55	10.4

1. *To calculate V_{BR} versus T_j : V_{BR} at T_j = V_{BR} at 25 °C x (1 + αT x (T_j - 25))*
2. *To calculate V_{CL} versus T_j : V_{CL} at T_j = V_{CL} at 25 °C x (1 + αT x (T_j - 25))*
3. *To calculate V_{CL} max versus $I_{PPappli}$: V_{CLmax} = V_{BR} max + R_D x $I_{PPappli}$*

1.1 Characteristics (curves)

Figure 3. Peak power dissipation versus initial junction temperature

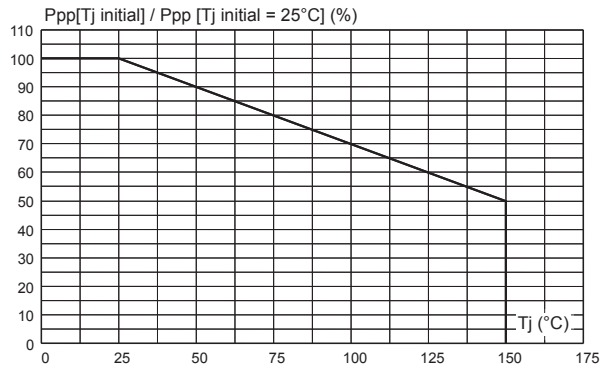


Figure 4. Peak pulse power versus exponential pulse duration (T_j initial = 25 °C)

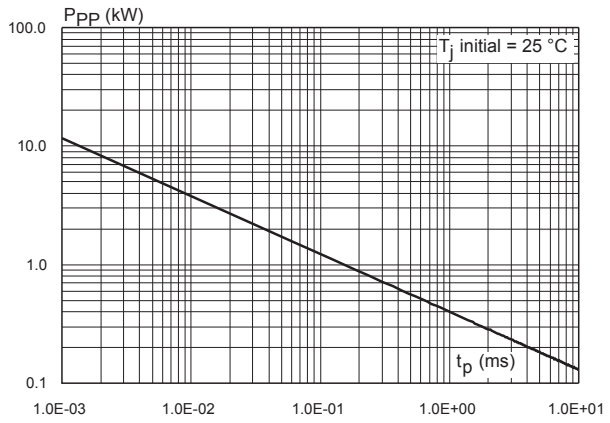


Figure 5. Clamping voltage versus peak pulse current (exponential waveform, maximum values)

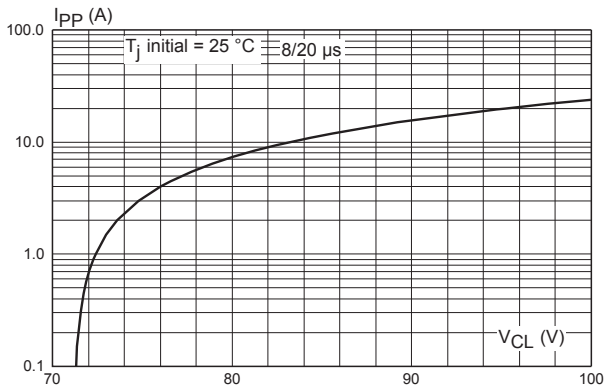


Figure 6. Capacitance versus voltage

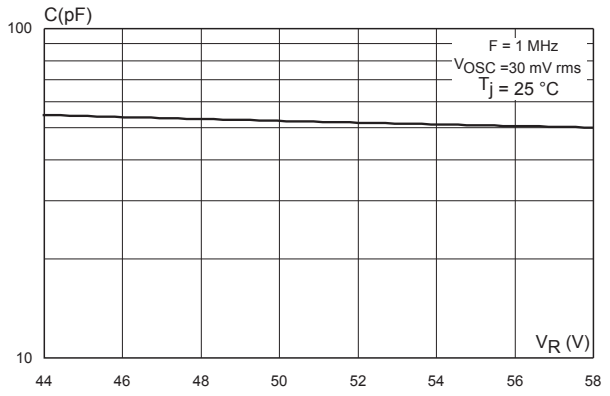


Figure 7. Peak forward voltage drop versus peak forward current

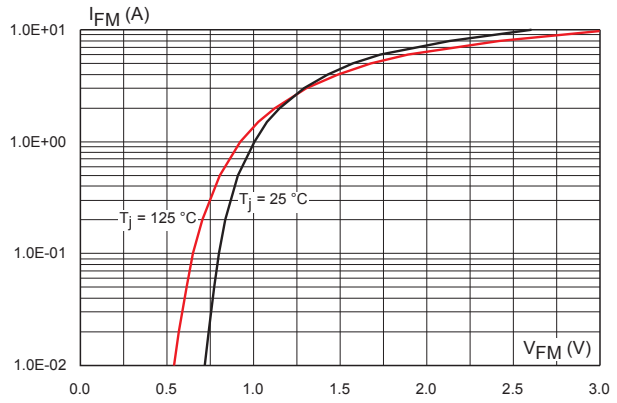


Figure 8. Relative variation of thermal impedance junction to ambient versus pulse duration

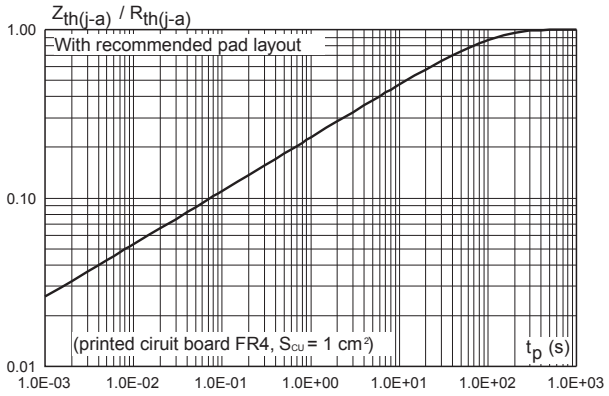
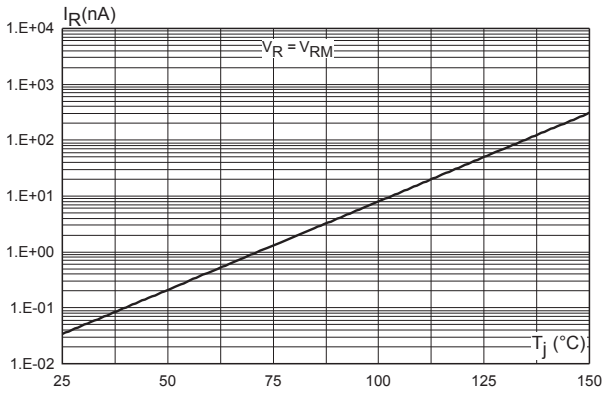


Figure 9. Leakage current versus junction temperature



2 Application

Figure 10. **Typical application circuit with PMOS integrated in PSE controller**

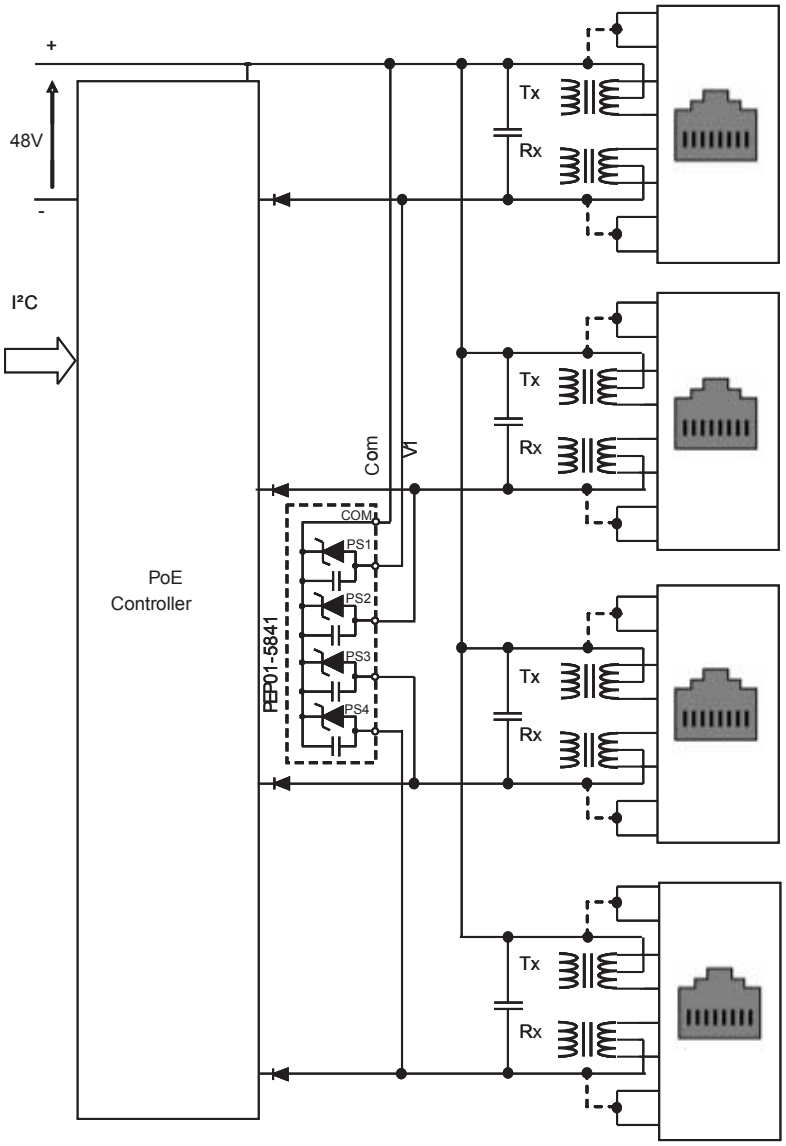


Figure 11. **Typical application circuit with external PMOS**

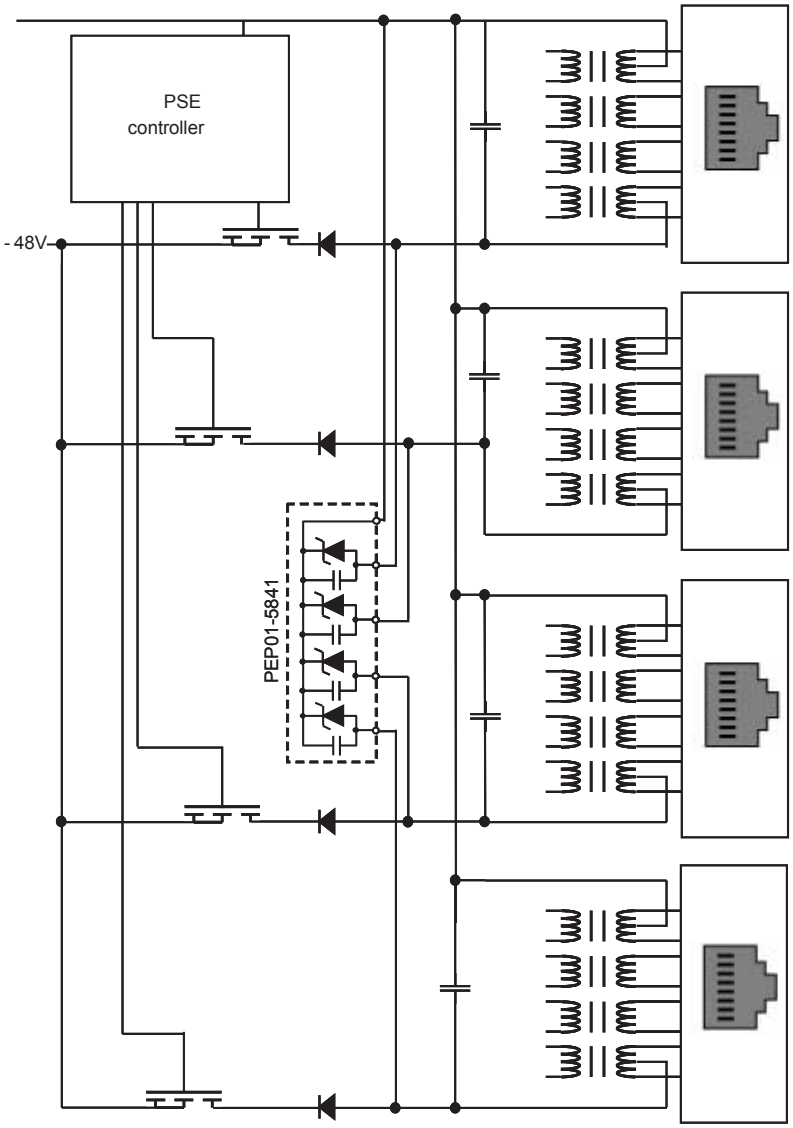
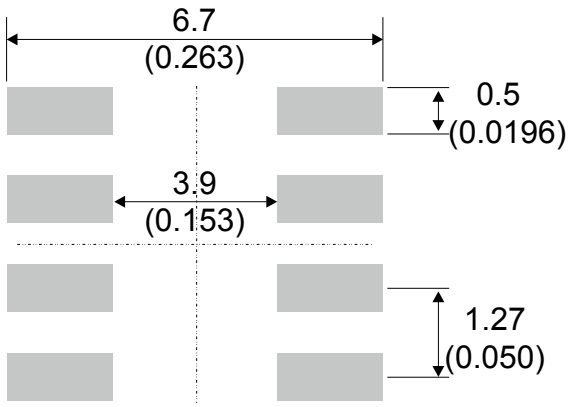


Figure 10. Typical application circuit with PMOS integrated in PSE controller and Figure 11. Typical application circuit with external PMOS show typical application schematics of PoE network. Power sourcing equipment (PSE) allows communication and power sourcing for several power devices (PD). The number of ways is generally a multiple of 4, this optimizes the PEP01-5841 for track layout and crosstalk, as well as PCB surface occupation. This protection device has been studied to comply with the latest IEEE 802.3af-2003 requirements and to withstand the surge defined in the IEC 61000-4-5 level 2 requirements.

3 Technical information

Figure 12. Footprint recommendation for improved clearance dimensions in mm (inches)



On top of the recommended SO-8 footprint described in Figure 14. Footprint recommendations, dimensions in mm (inches), the above footprint offers a better clearance for voltage higher than 50 V.

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

Figure 13. SO-8 package outline

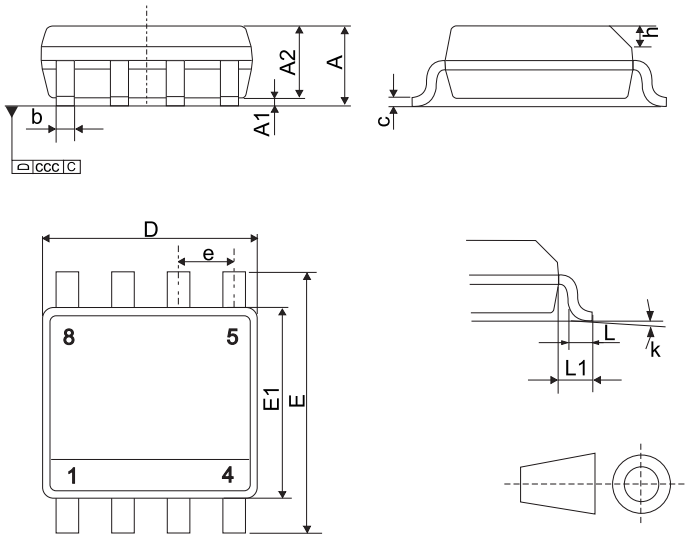


Table 3. SO-8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.31		0.51	0.012		0.020
c	0.10		0.25	0.004		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.05
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

Figure 14. Footprint recommendations, dimensions in mm (inches)

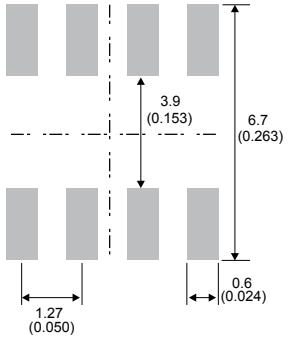
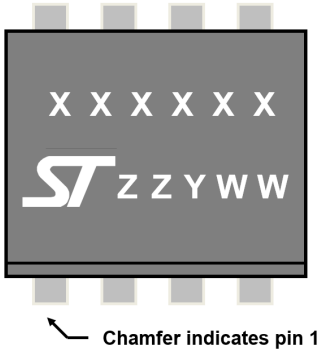
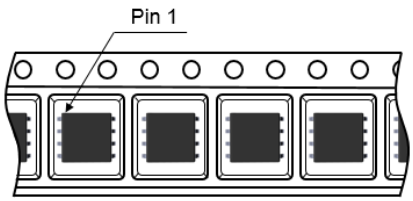


Figure 15. Marking layout (refer to ordering information table for marking)



XXXXX : Marking
ZZ : Manufacturing location
Y : Year
WW : week

Figure 16. Package orientation in reel



Taped according to EIA-481
Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Figure 17. Tape and reel orientation

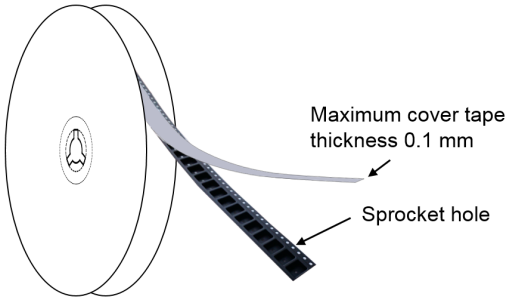


Figure 18. Reel dimensions (mm)

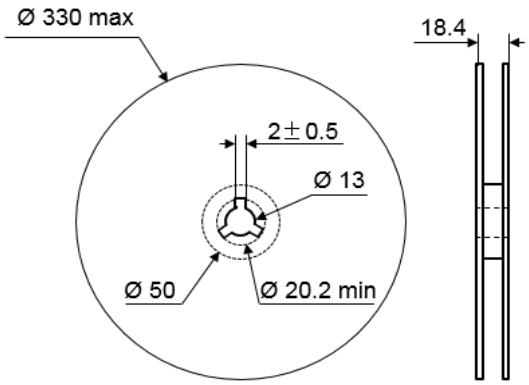


Figure 19. Inner box dimensions (mm)

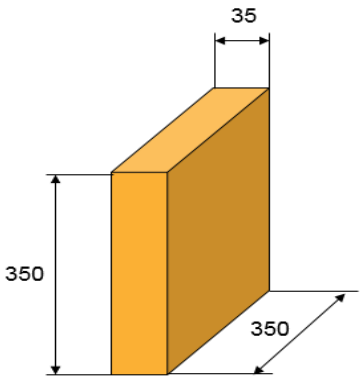
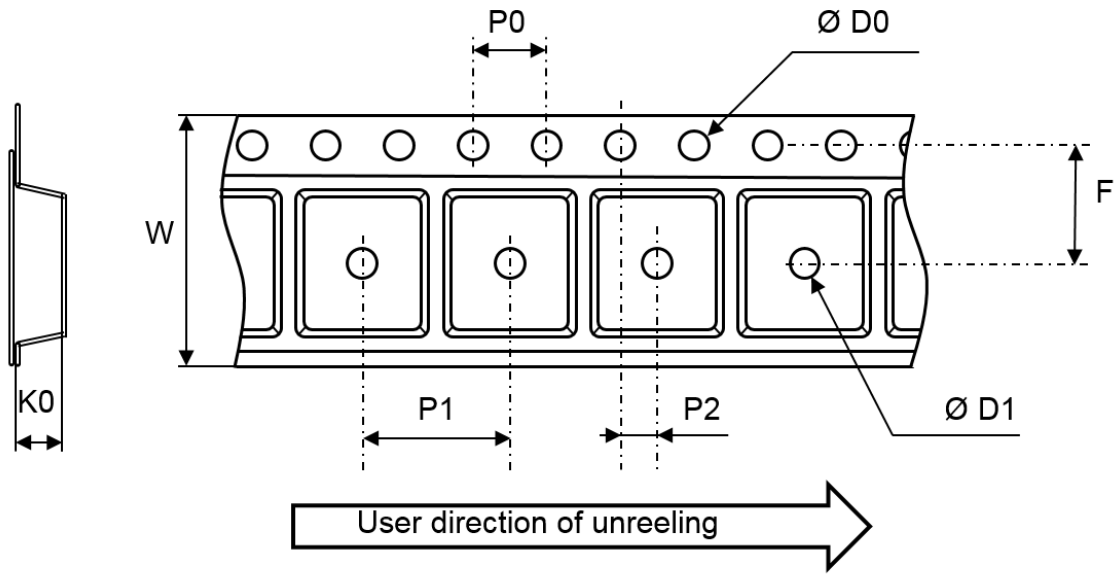


Figure 20. **Tape and reel outline**

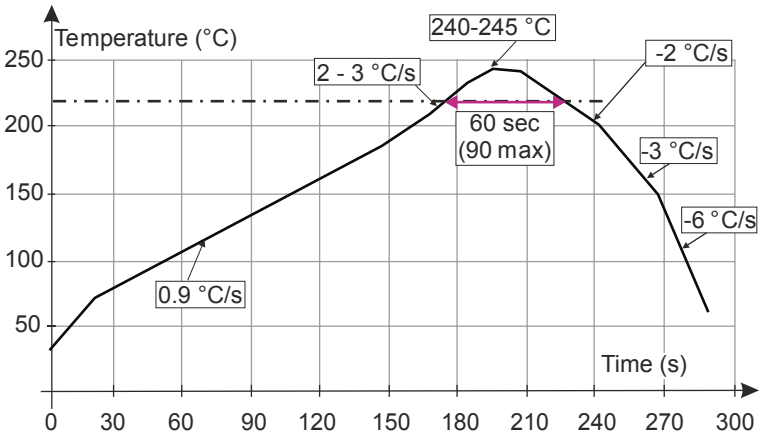


Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 4. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
P0	3.9	4	4.1
P1	7.9	8	8.1
P2	1.95	2	2.05
ØD0	1.45	1.5	1.6
ØD1	1.6		
F	5.45	5.5	5.55
K0	2.5	2.6	2.7
W	11.7	12	12.3

Figure 21. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

5 Ordering information

Figure 22. **Ordering information scheme**

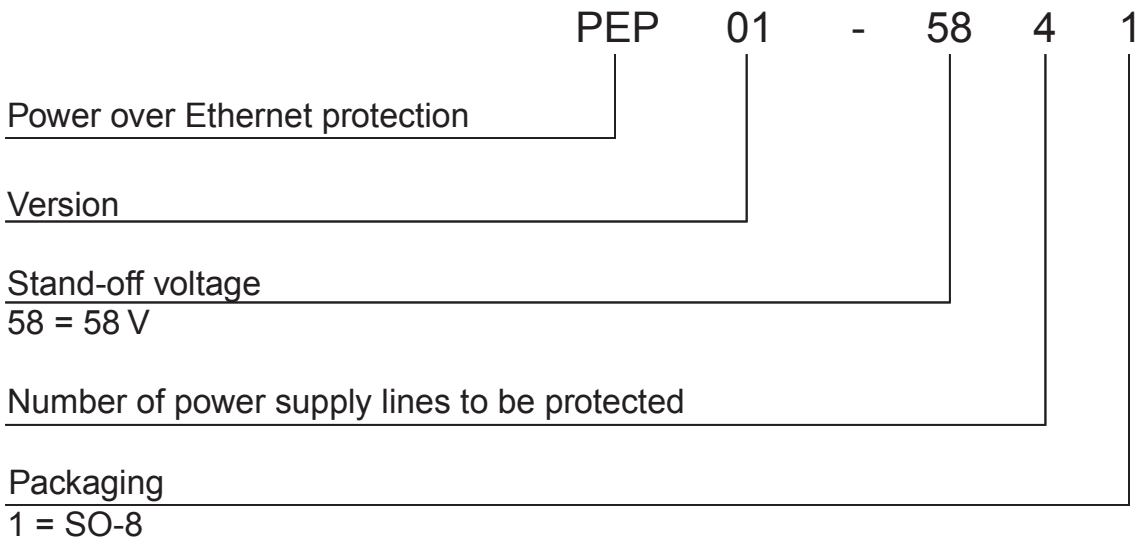


Table 5. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
PEP01-5841	58E1	SO-8	78 mg	2000	Tape and reel

Revision history

Table 6. **Document revision history**

Date	Version	Changes
06-May-2009	1	Initial release.
14-May-2009	2	Standards compliance updated.
17-Jan-2013	3	Added note on GND pins in Figure 1 and added Figure 15.
13-Nov-2013	4	Updated level 4 to level 2 under Figure 12.
15-May-2020	5	Updated Figure 12. Footprint recommendation for improved clearance dimensions in mm (inches) and Figure 10. Typical application circuit with PMOS integrated in PSE controller. Minor text change to improve the readability.

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