

Features

- Packaged in lead-free Flip Chip
- Very low resistance: $0.35\ \Omega$
- High attenuation: -45 dB at 900 MHz
- Very low PCB space consumption:
0.89 mm x 1.26 mm
- Very thin package: 0.65 mm
- High efficiency in ESD suppression
IEC6 1000-4-2 level 4
- High reliability offered by monolithic integration
- High reduction of parasitic elements through
integration and wafer level packaging

Complies with the following standards

- IEC 61000-4-2 level 4:
 - $\pm 15\text{ kV}$ (air discharge)
 - $\pm 8\text{ kV}$ (contact discharge)

Application

- Mobile phones

Description

The EMIF02-SPK02F2 chip is a highly integrated device designed to suppress EMI/RFI noise for interface line filtering.

The EMIF02-SPK02F2 flip-chip packaging means the package size is equal to the die size. That's why the EMIF02-SPK02F2 is a very small device.

Additionally, this filter includes ESD protection circuitry, which prevents damage to the protected device when subjected to ESD surges up to 30 kV.

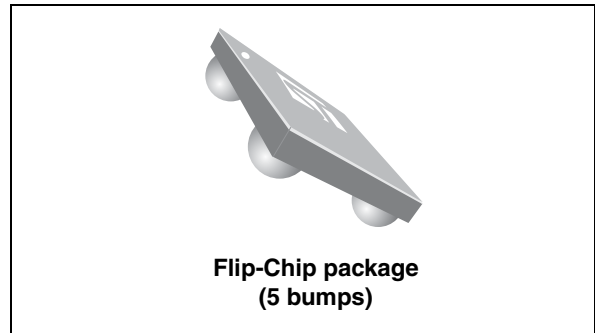


Figure 1. Pin configuration (bump side)

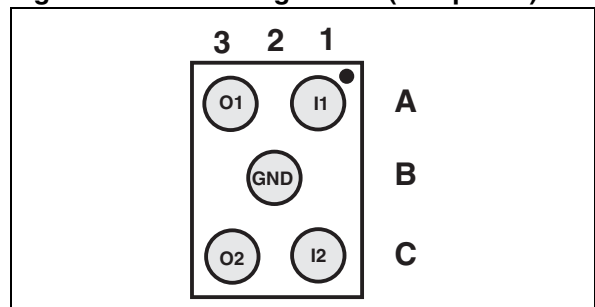
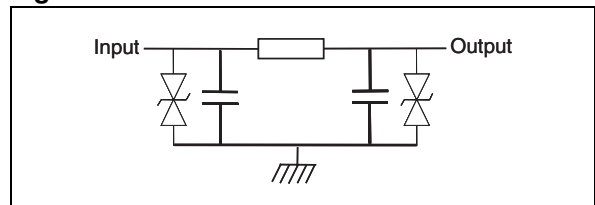


Figure 2. Functional schematic



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1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2		
	Air discharge	30	kV
	Contact discharge	30	
I_{SPK}	Maximum rms current per channel	350	mA
T_j	Junction temperature range	-30 to 125	$^{\circ}\text{C}$
T_{stg}	Storage temperature range	-55 to + 150	$^{\circ}\text{C}$

Figure 3. Electrical characteristics - definitions

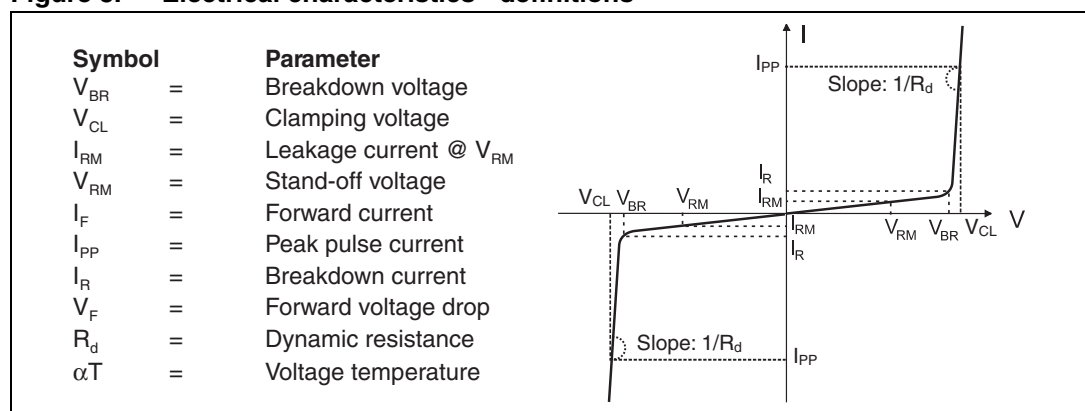


Table 2. Electrical characteristics - values ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	$I_R = 1\text{ mA}$	6			V
I_{RM}	$V_{RM} = 3\text{ V}$			400	nA
$R_{I/O}$			0.35	0.8	Ω
C_{LINE}	$V_R = 0\text{ V DC}$, 1 MHz	185	250	315	pF
F_c	Cut-off frequency: $Z_{SOURCE} = Z_{LOAD} = 50\text{ }\Omega$		20		MHz

Figure 4. Attenuation measurements versus frequency

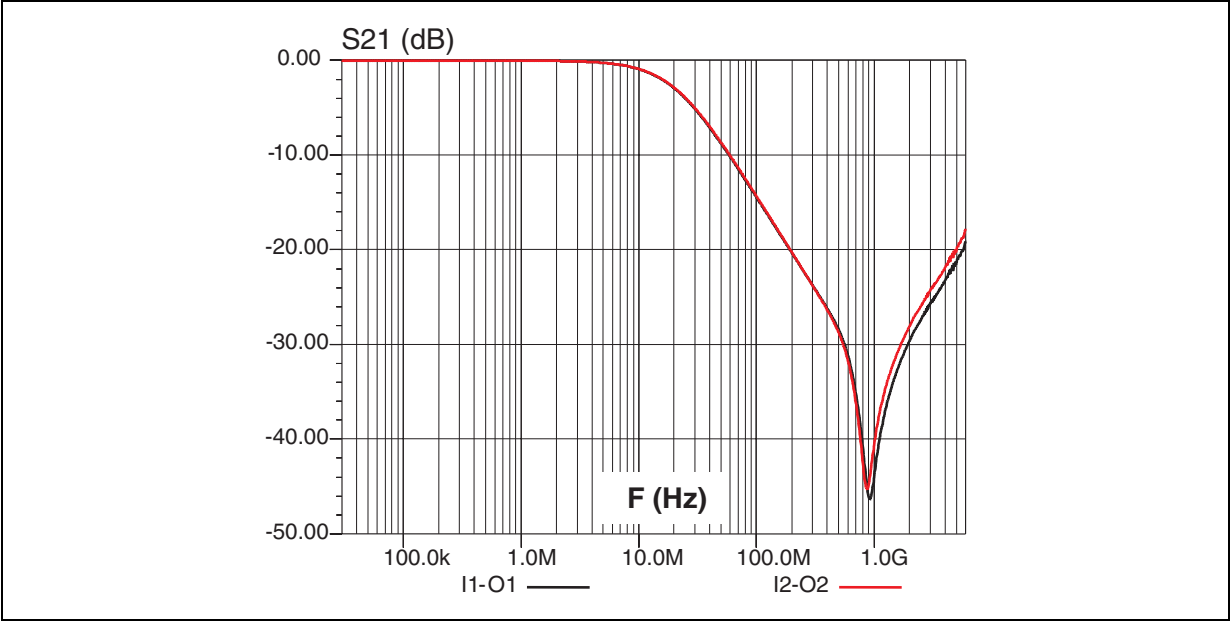


Figure 5. Crosstalk measurements versus frequency

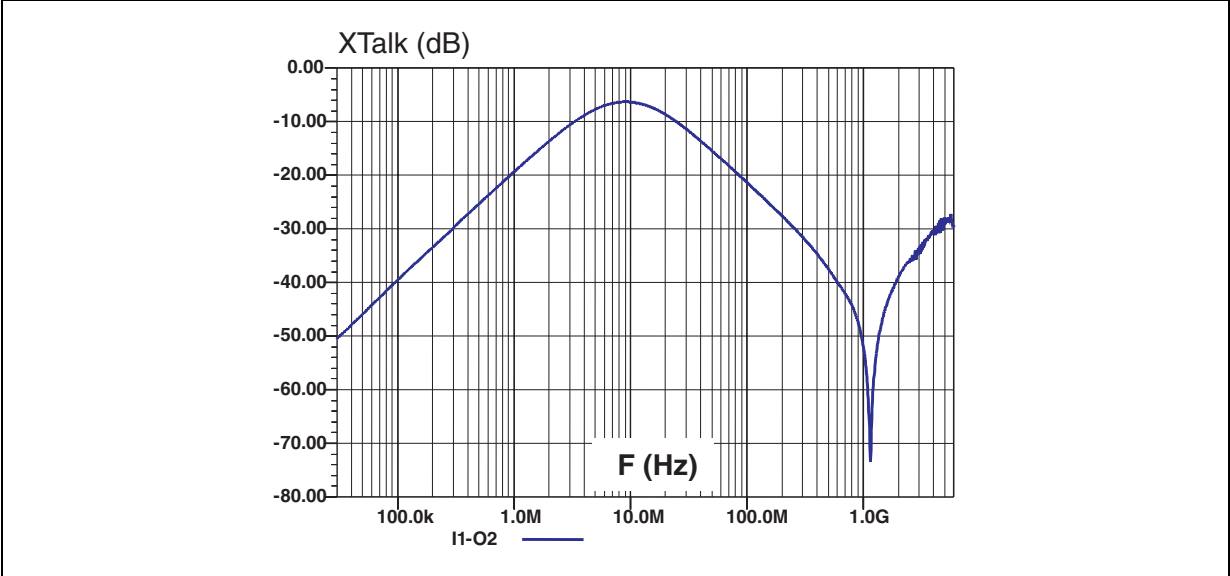
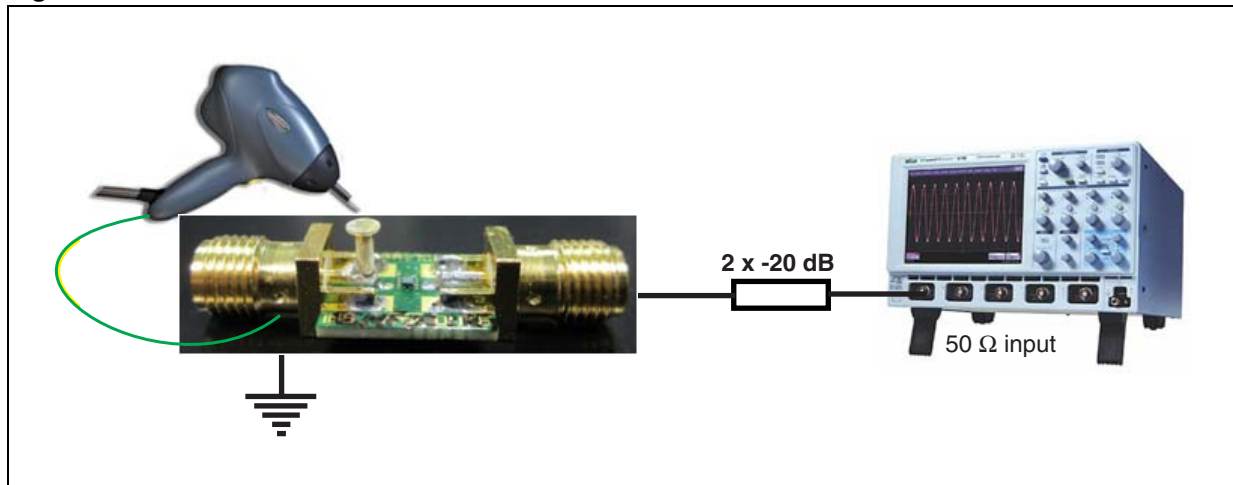
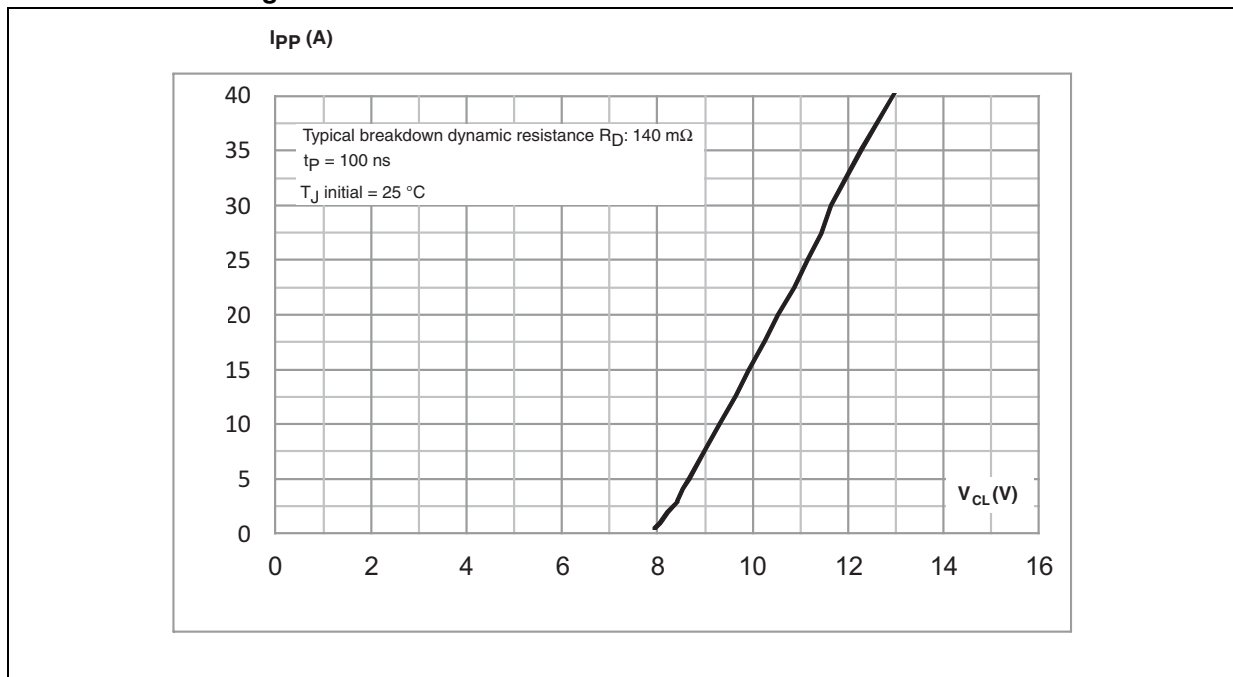


Figure 6. ESD test conditions

Figure 7. Clamping voltage V_{CL} versus peak pulse current I_{PP} for short pulse duration such as ESD surges

Note: For further information on the dynamic characteristic see the STMicroelectronics' application note AN4022, "TVS short pulse R_d measurement and correlation with TVS clamping voltage during ESD".

Figure 8. Output filter ESD response to IEC 61000-4-2 (+8 kV contact discharge) I1 to O1

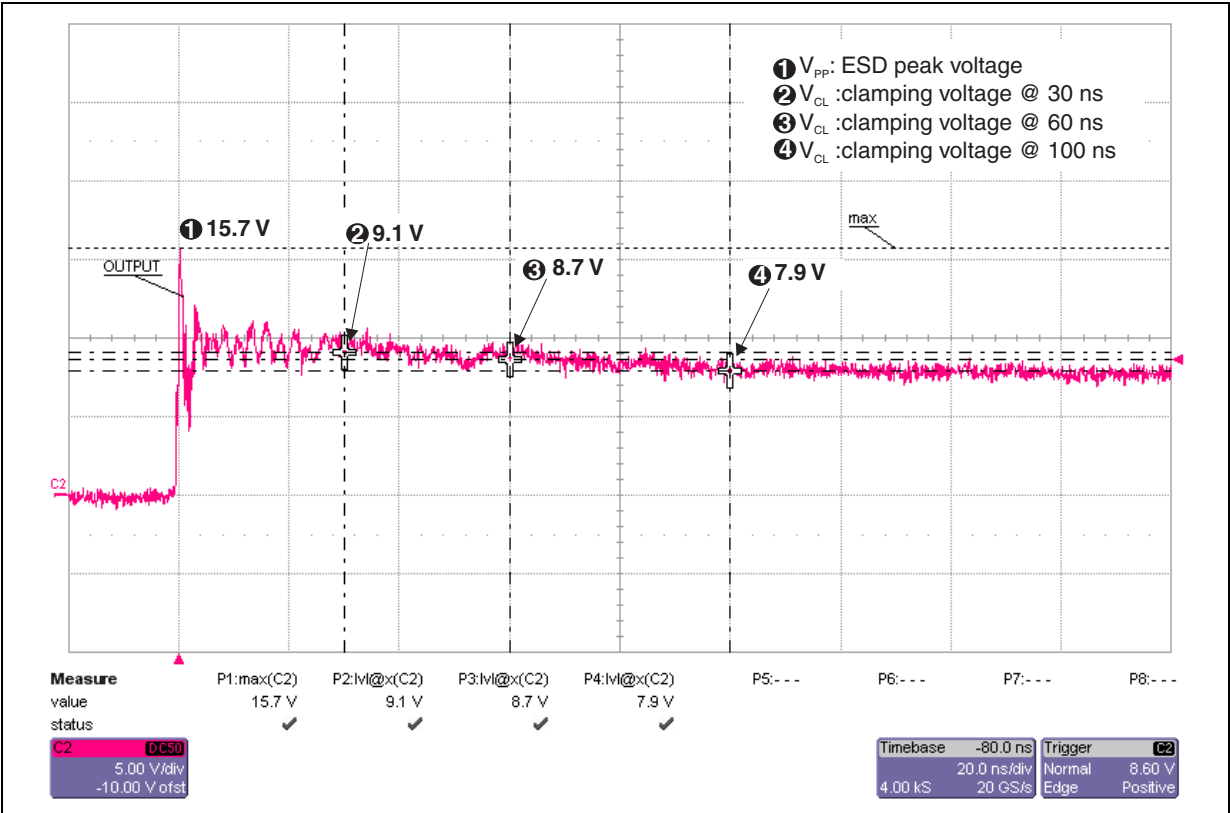


Figure 9. Output filter ESD response to IEC 61000-4-2 (-8 kV contact discharge) I1 to O1

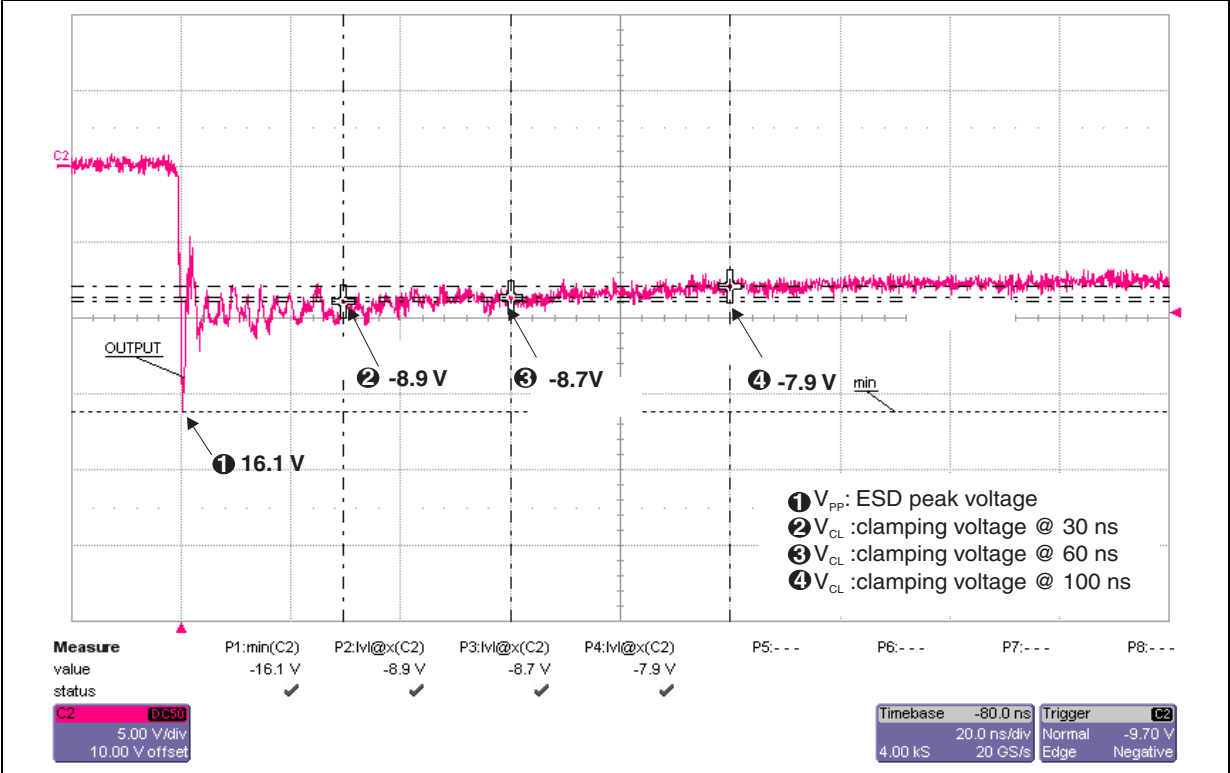


Figure 10. Output filter ESD response to IEC 61000-4-2 (+15 kV contact discharge) I1 to O1

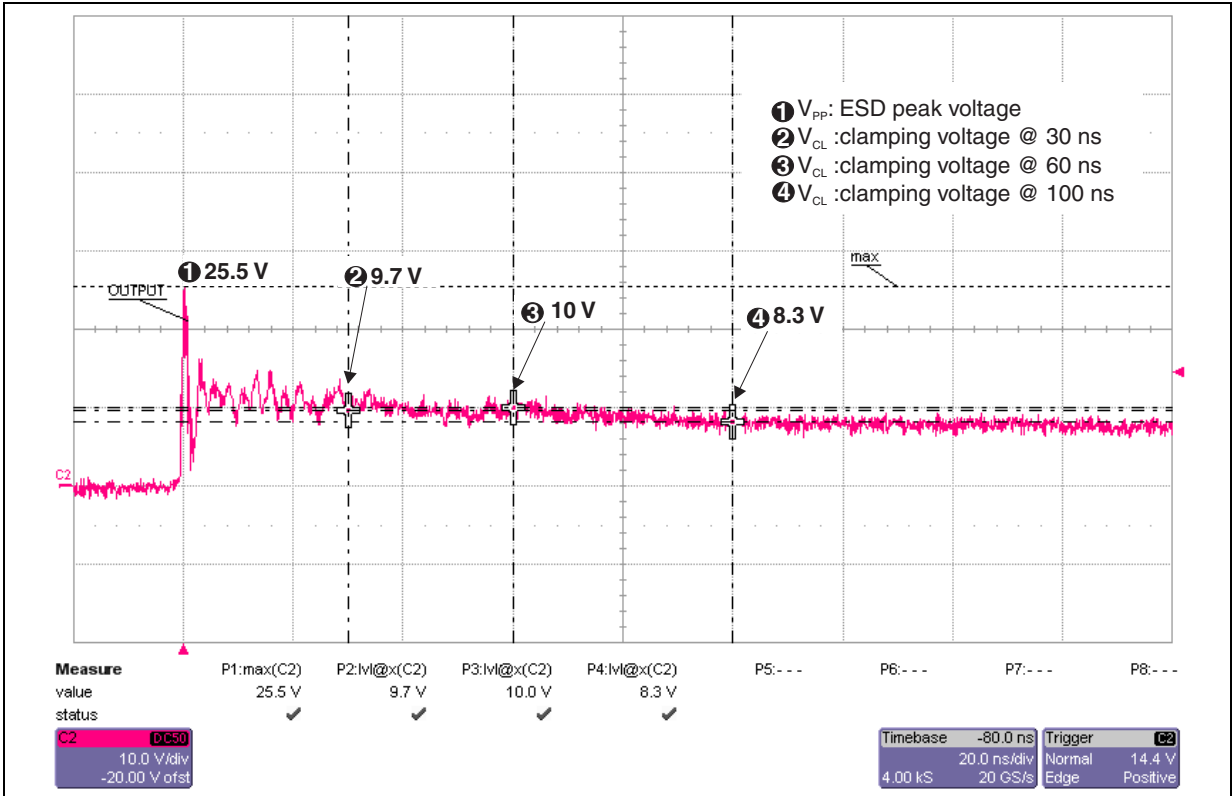


Figure 11. Output filter ESD response to IEC 61000-4-2 (-15 kV contact discharge) I1 to O1

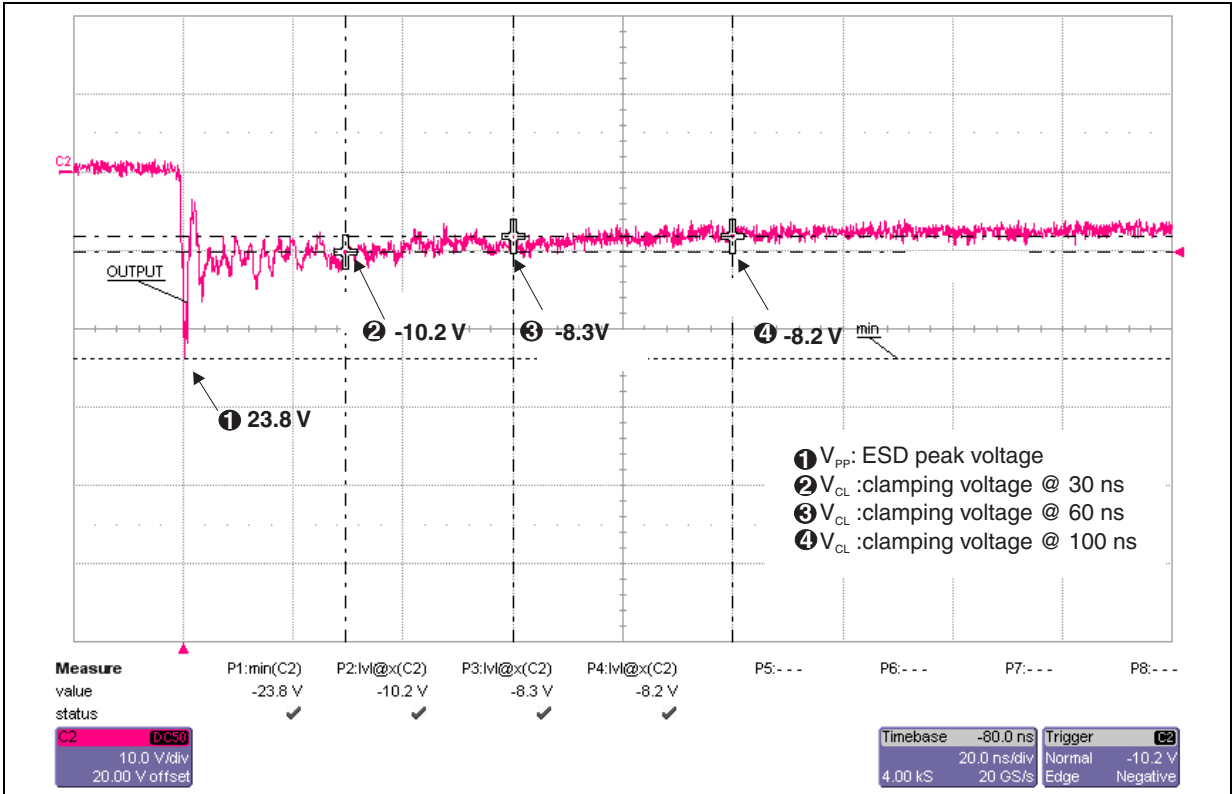


Figure 12. Output filter ESD response to IEC 61000-4-2 (+30 kV contact discharge) I1 to O1

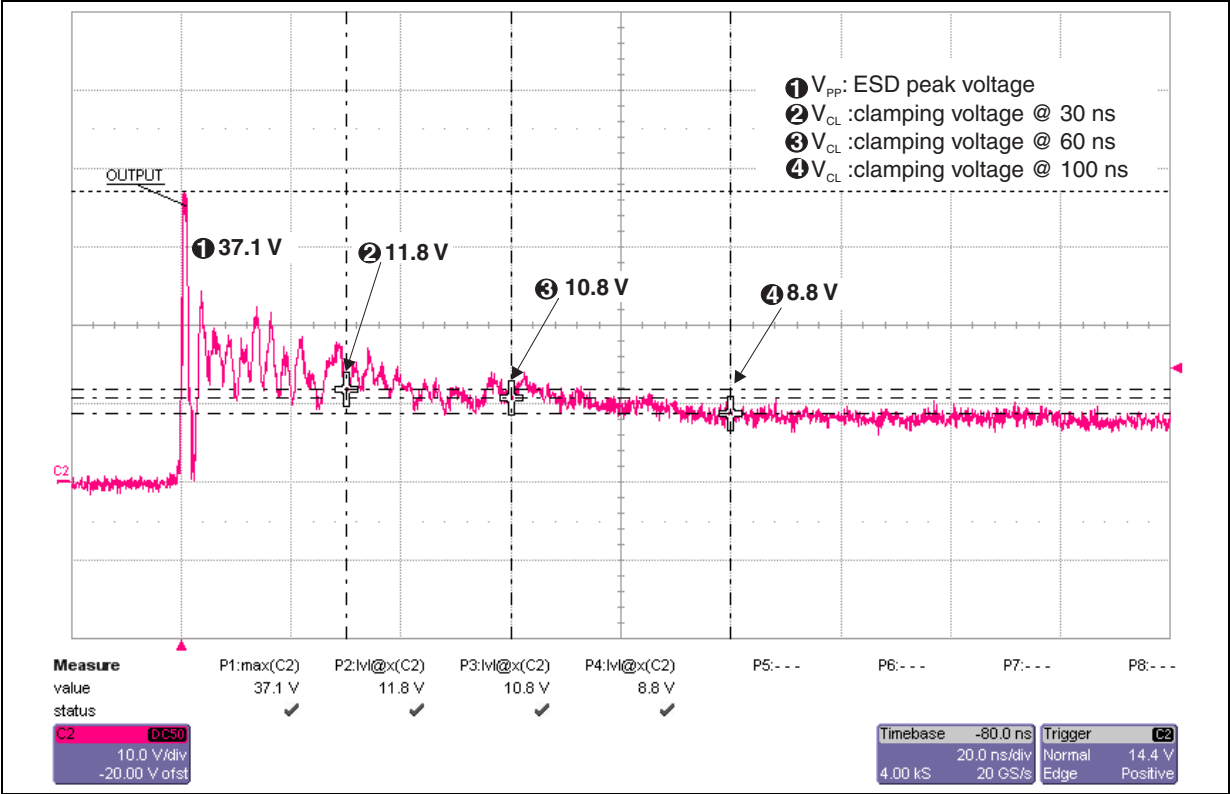
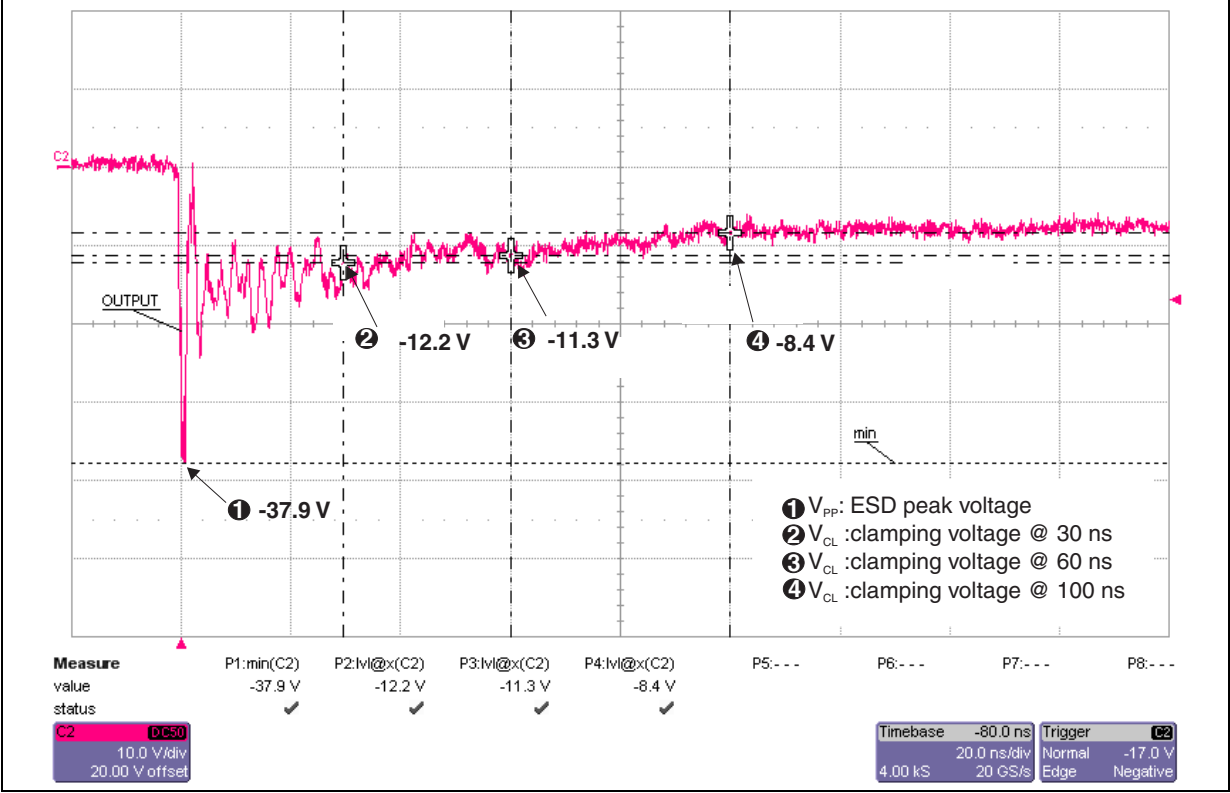
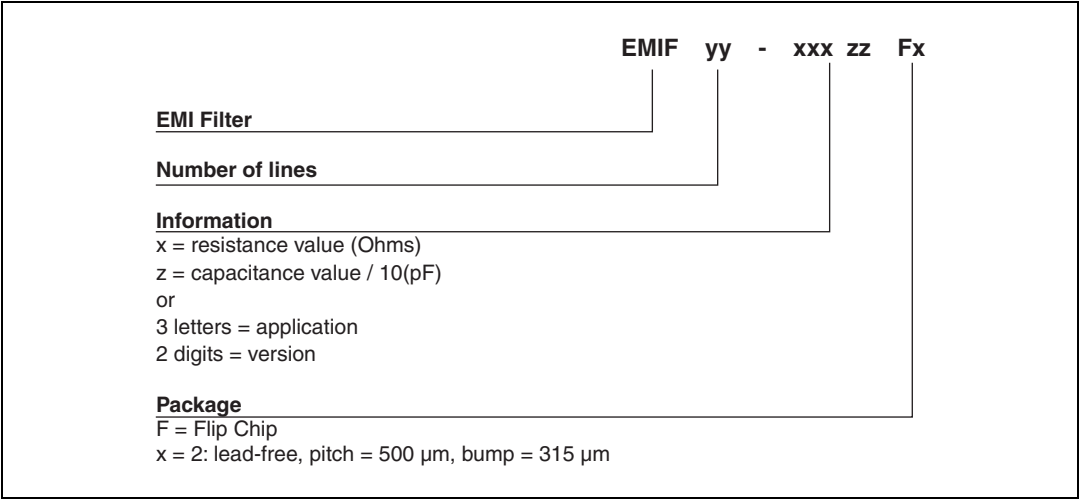


Figure 13. Output filter ESD response to IEC 61000-4-2 (-30 kV contact discharge) I1 to O1



2 Ordering information scheme

Figure 14. Ordering information scheme



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 15. Package dimensions

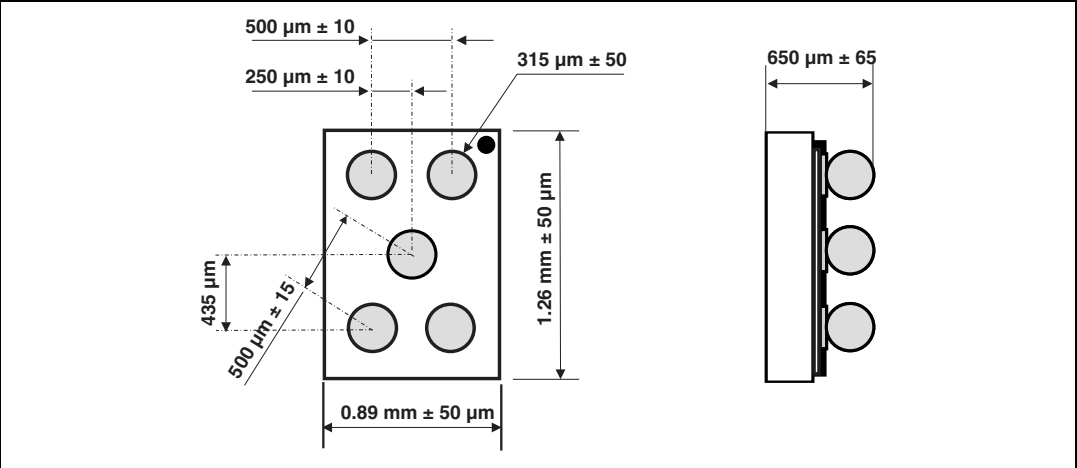


Figure 16. Footprint

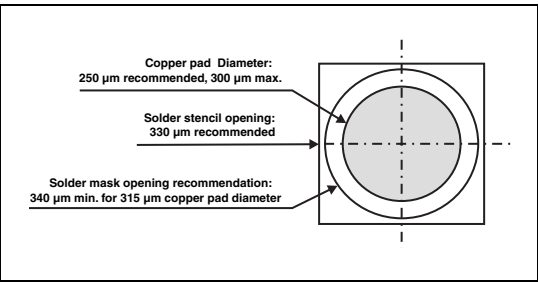
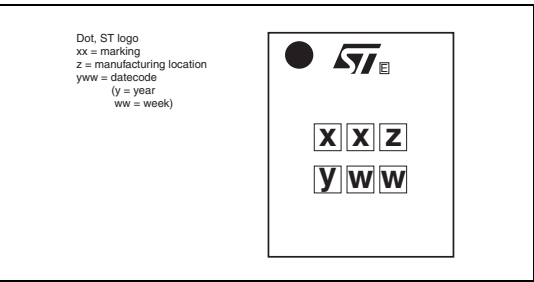


Figure 17. Marking



4 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-SPK02F2	JD	Flip Chip	1.8 mg	5000	Tape and reel 7"

5 Revision history

Table 4. Document revision history

Date	Revision	Changes
17-Sep-2008	1	Initial release.
12-Sep-2011	2	Updated Figure 15 and Figure 16 .
3-Apr-2012	3	Updated cover page features and description. Inserted Figure 6 to Figure 13 .

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