ESDALC6V1-5M6

5-line low capacitance Transil™ arrays for ESD protection

Datasheet - production data

Micro QFN package

Features

- High ESD protection level
- High integration
- Suitable for high density boards
- 5 unidirectional Transil diodes
- Breakdown voltage V_{BR} = 6.1 V min.
- Low diode capacitance (12 pF typ at 0 V)
- Low leakage current < 70 nA
- Very small PCB area: 1.45 mm^2
- 500 microns pitch
- Lead-free package

Complies with the following standards

- IEC 61000-4-2
- 15 kV (air discharge)
- 8 kV (contact discharge)
- MIL STD 883G- Method 3015-7: class3B
- >8 kV (human body model)

Applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

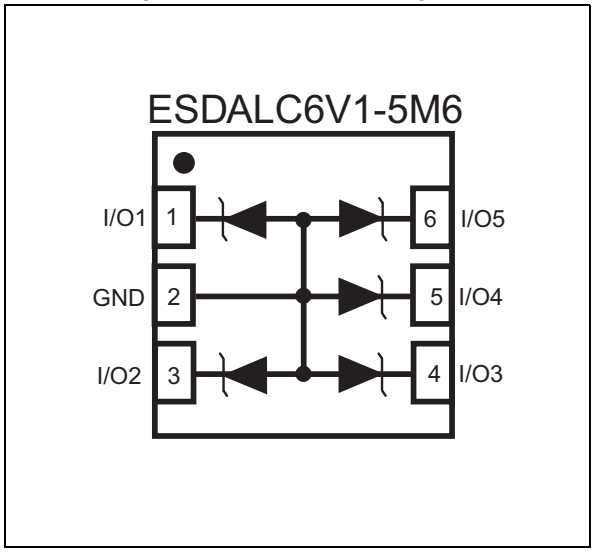
- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC6V1-5M6 is a monolithic array designed to protect up to 5 lines against ESD transients.

The device is ideal for applications where both reduced print circuit board space and power absorption capability are required.

Figure 1. Functional diagram



TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	ESD IEC 61000-4-2, air discharge ESD IEC 61000-4-2, contact discharge MIL STD 883G- Method 3015-7: class3B, (human body model)		±15 ±8 25	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)(1)	T_j initial = T_{amb}	30	W
I_{pp}	Repetitive peak pulse current typical value (8/20 µs)		3	A
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C
T_{OP}	Operating temperature range		-40 to +125	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definition)

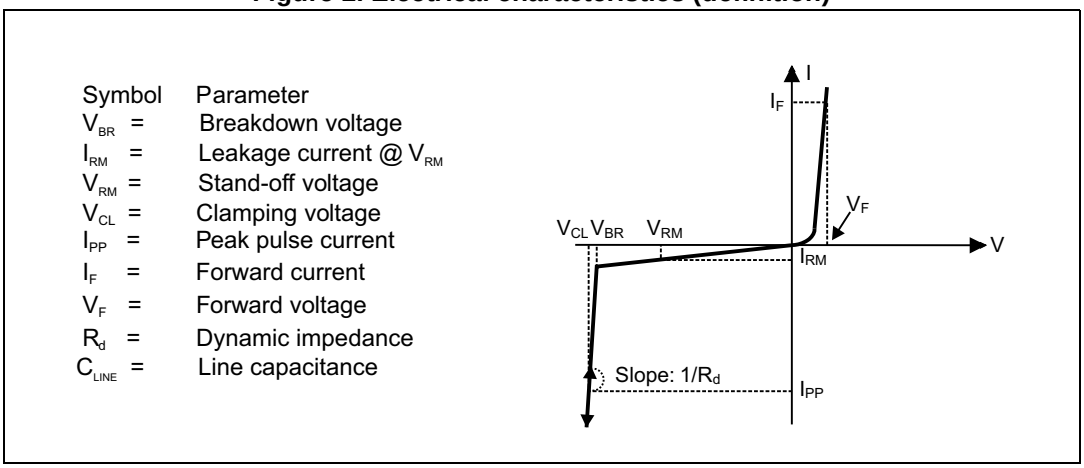


Table 2. Electrical characteristics (value T_{amb} = 25 °C)

Symbol	Test condition	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6.1		7.2	V
I_{RM}	V_{RM} = 3 V			70	nA
V_F	I_F = 10 mA			1	V
R_d				3	Ω
αT(1)	I_R = 1 mA		2	5	10^{-4}/ °C
C	V_R =0 V DC, F = 1 MHz, V_{osc} = 30 mV_{RMS}		12	15	pF

1. $\Delta V_{BR} = \alpha T * (T_{amb} - 25\ °C) * V_{BR}$ (25 °C)

Figure 3. Relative variation of peak pulse power versus initial junction temperature

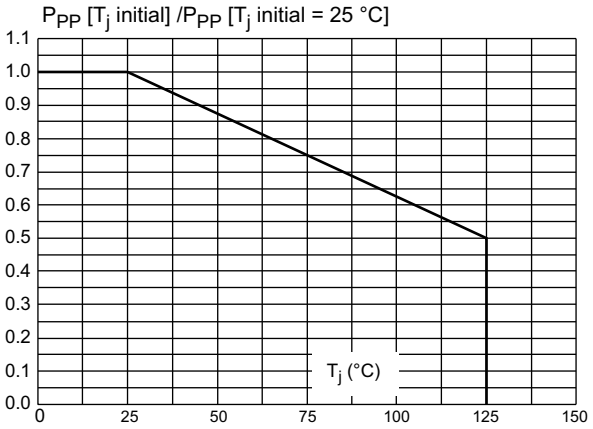


Figure 4. Peak pulse power versus exponential pulse duration

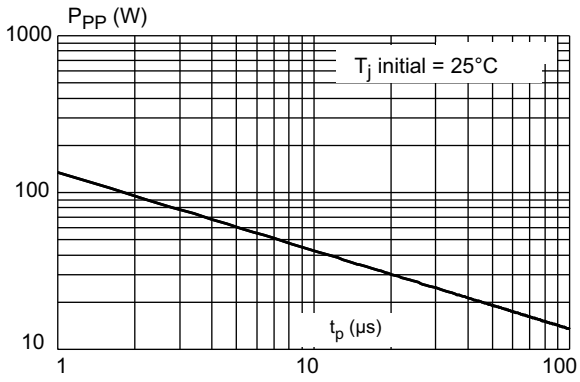


Figure 5. Clamping voltage versus peak pulse current (typical values, 8/20 µs waveform)

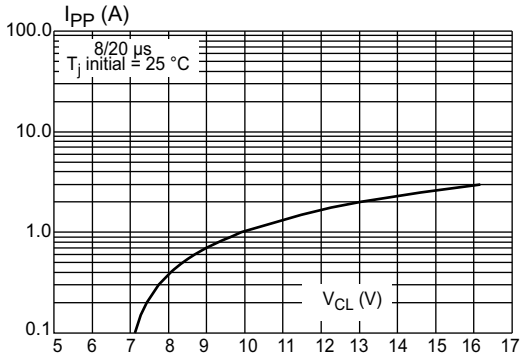


Figure 6. Forward voltage drop versus peak forward current (typical values)

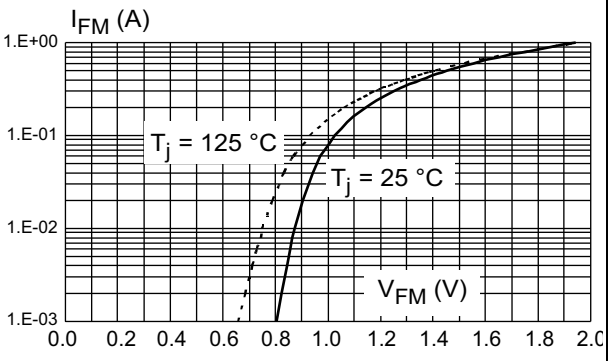


Figure 7. Junction capacitance versus reverse voltage applied (typical values)

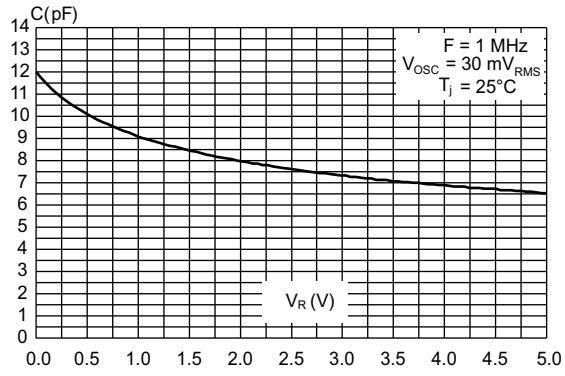


Figure 8. Relative variation of leakage current versus junction temperature (typical values)

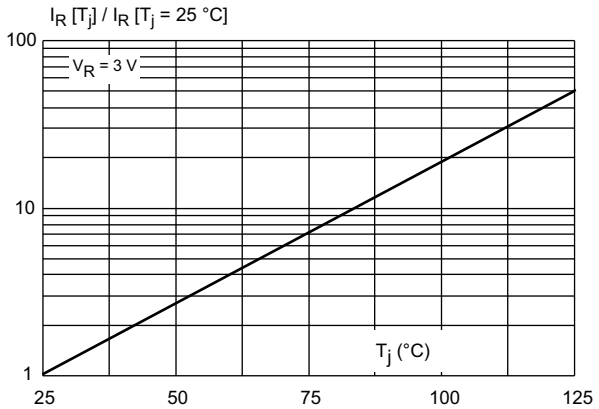


Figure 9. S21 attenuation measurement results of each channel

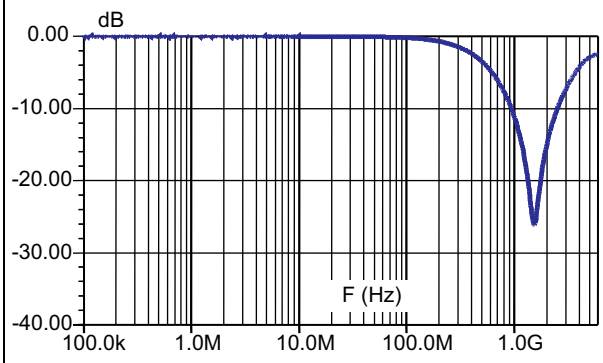


Figure 10. Analog crosstalk measurements between channels

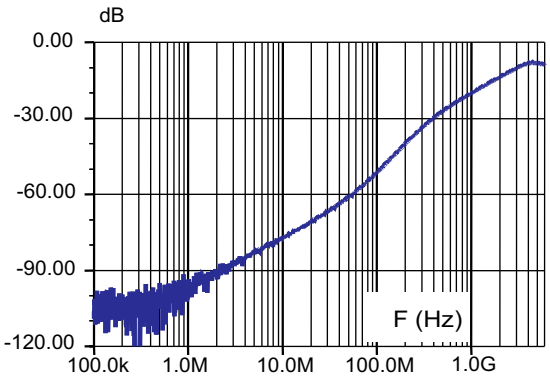


Figure 11. ESD response to IEC 61000-4-2 (+8 kV contact discharge) on each channel

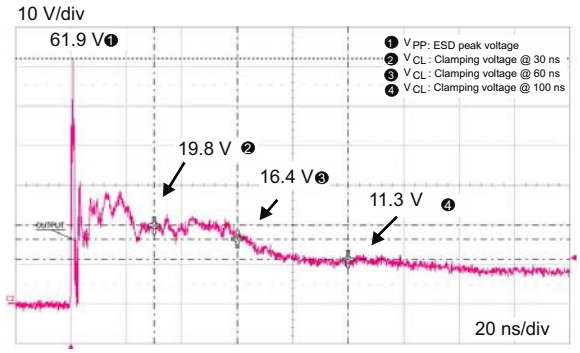
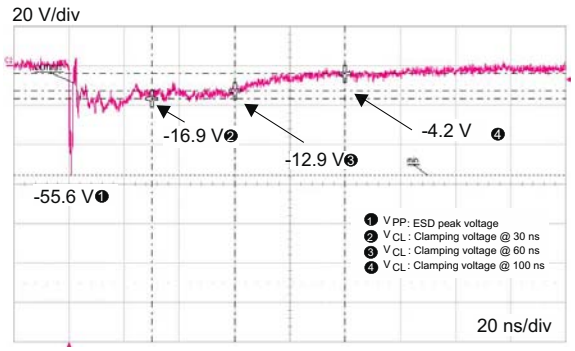


Figure 12. ESD response to IEC 61000-4-2 (-8 kV contact discharge) on each channel



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

2.1 Micro QFN package information

Figure 13. Micro QFN package outline

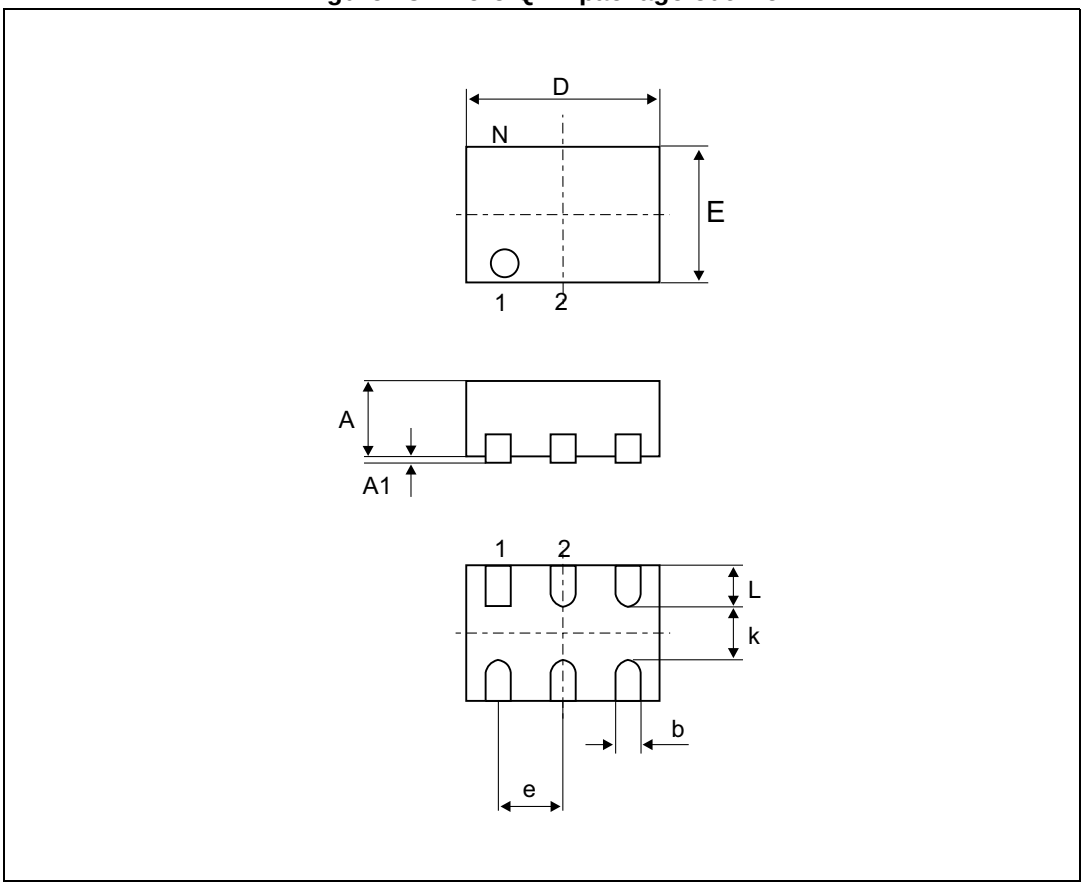


Table 3. Micro QFN package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.55	0.50	0.60	0.022	0.020	0.024
A1	0.02	0.00	0.05	0.001	0.000	0.002
b	0.25	0.18	0.30	0.010	0.007	0.012
D[2]	1.45			0.057		
E[2]	1.00			0.039		
e[3]	0.50			0.020		
k		0.20			0.008	
L	0.35	0.30	0.40	0.014	0.012	0.016

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. ± 0.1 mm
3. ± 0.05 mm

Figure 14. Footprint dimensions in mm [inches]

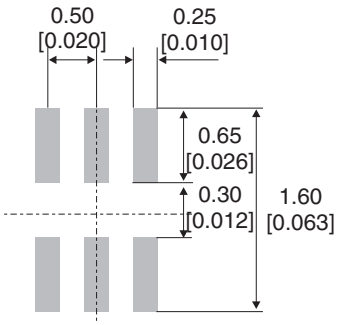
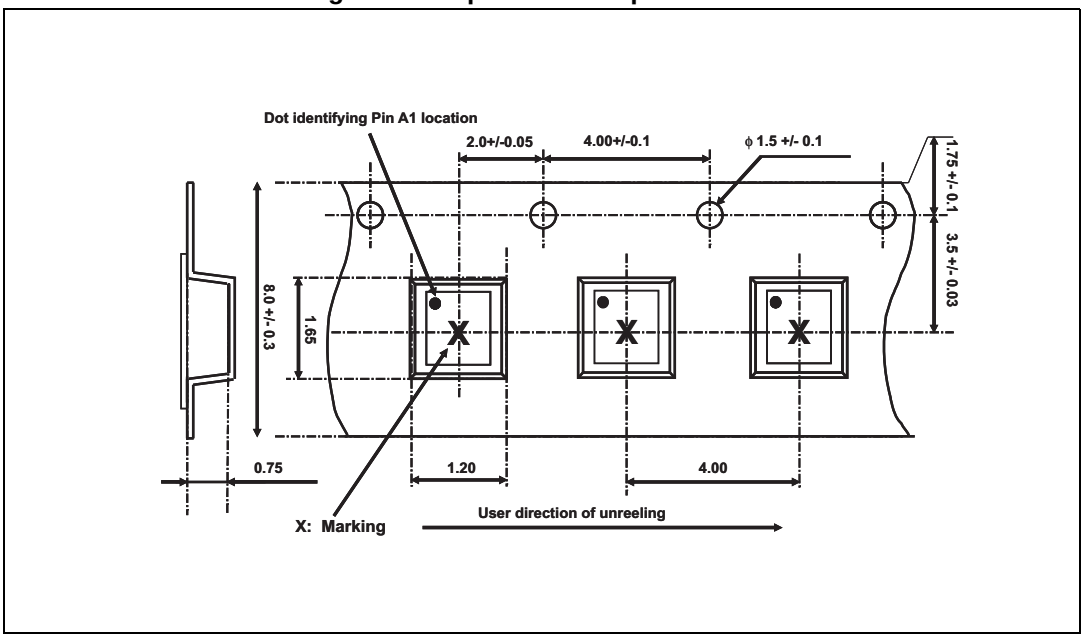


Figure 15. Tape and reel specification



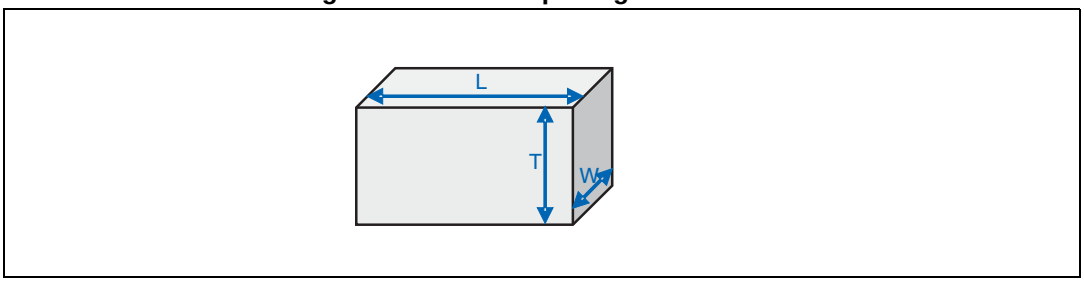
Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 16. Stencil opening dimensions



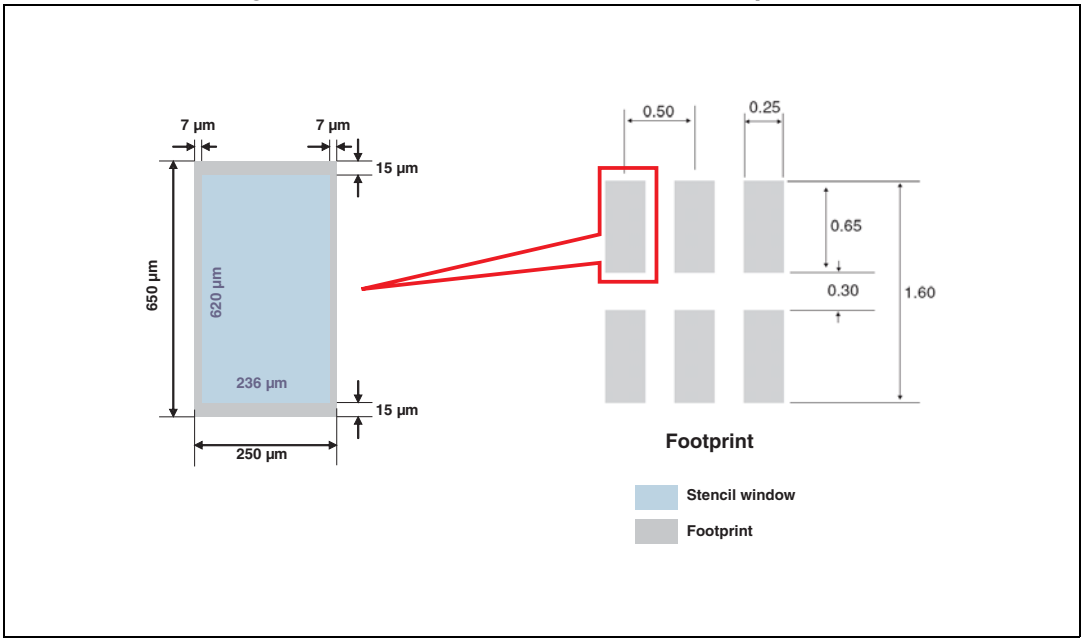
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 17. Recommended stencil window position



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3 Placement

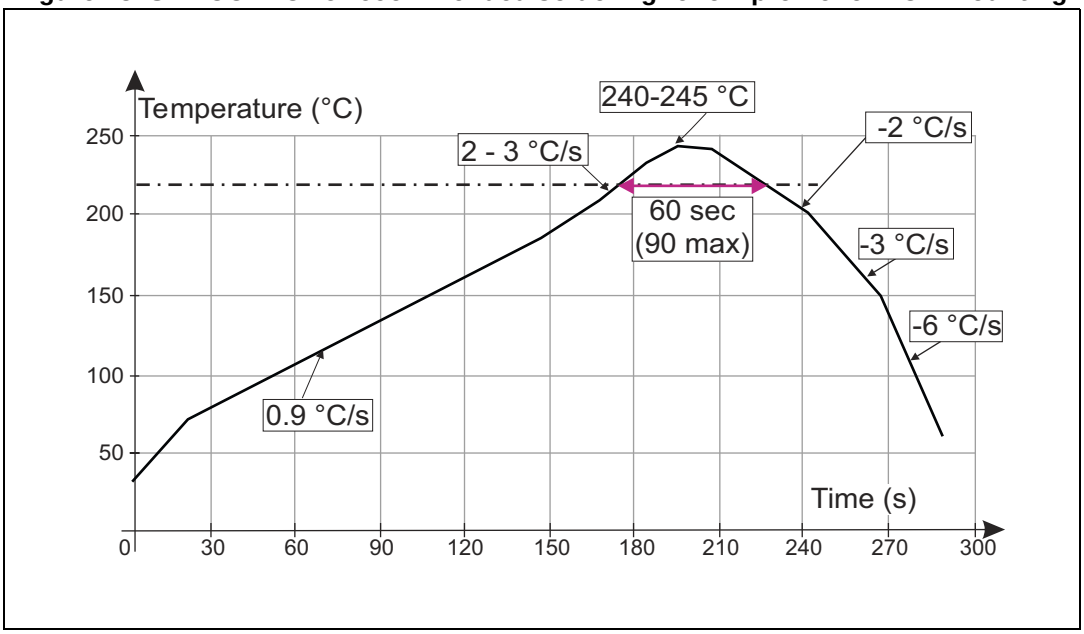
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

3.5 Reflow profile

Figure 18. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 19. Ordering information scheme

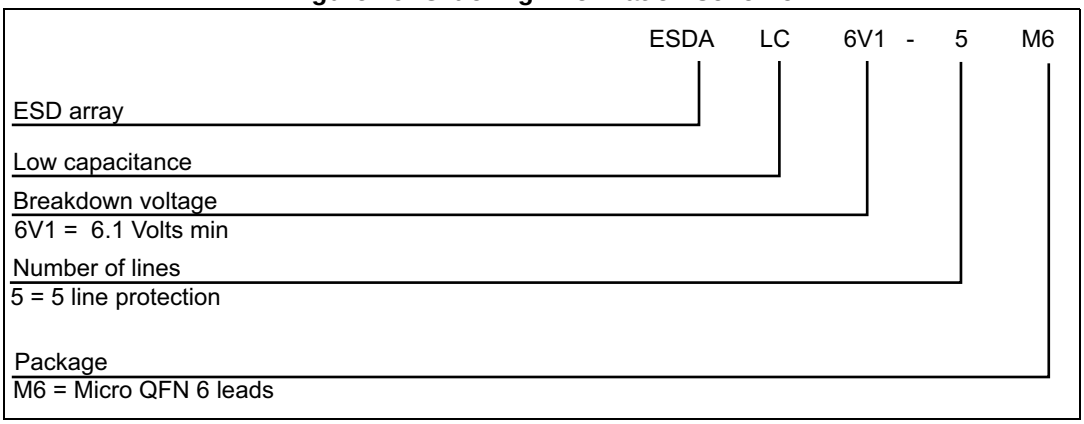


Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDALC6V1-5M6	H(1)	Micro QFN	2.2 mg	3000	Tape and reel

1. The marking can be rotated by 90° to differentiate assembly location

5 Revision history

Table 5. Document revision history

Date	Revision	Changes
19-Sep-2005	1	Initial release.
10-Oct-2005	2	Package title changed from DFN to QFN. No technical changes.
21-Dec-2005	3	Updated package dimensions in Table 1.
01-Feb-2007	4	Reformatted to current standard. Added note on marking rotation in section 3. Package information.
14-Feb-2008	5	Reformatted to current standards. Corrected inch measurements in Table 3. Added Section 3: Recommendation on PCB assembly.
30-May-2011	6	Updated Figure 6. Updated ECOPACK statement.
12-Mar-2015	7	Title properties changed. Updated features and description on cover page. Updated Figure 1: Functional diagram and Table 4: Ordering information and Figure 19. Format updated to current standard.
05-Oct-2015	8	Updated *Figure 11* and *Figure 12*.

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