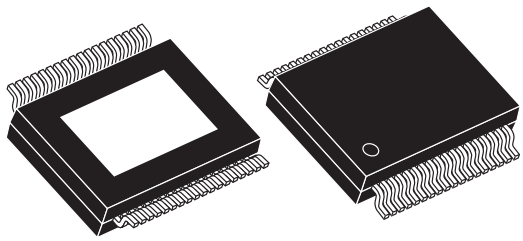
STA515W

40 V, 3 A, quad power half bridge

Datasheet - production data



PowerSO36 package with exposed pad up

Features

- Multipower BCD technology
- Low input/output pulse width distortion
- 200 mΩ R_{dsON} complementary DMOS output stage
- CMOS-compatible logic inputs
- Thermal protection
- Thermal warning output
- Undervoltage protection
- Short-circuit protection

Description

The STA515W is a monolithic quad half-bridge stage in Multipower BCD Technology. The device can be used as a dual bridge or reconfigured, by connecting pin CONFIG to pins VDD, as a single bridge with double-current capability.

The device is designed, particularly, to be the output stage of a stereo all-digital high-efficiency amplifier. It is capable of delivering 10 W x 4 channels into 4 Ω loads with 10% THD at V_{CC} = 18 V in single-ended configuration.

It can also deliver 20 W + 20 W into 8 Ω loads with 10% THD at V_{CC} = 18 V in BTL configuration or, in single parallel BTL configuration, 40 W into a 8 Ω load with 10% THD at V_{CC} = 26 V.

The input pins have a threshold proportional to the voltage on pin V_L.

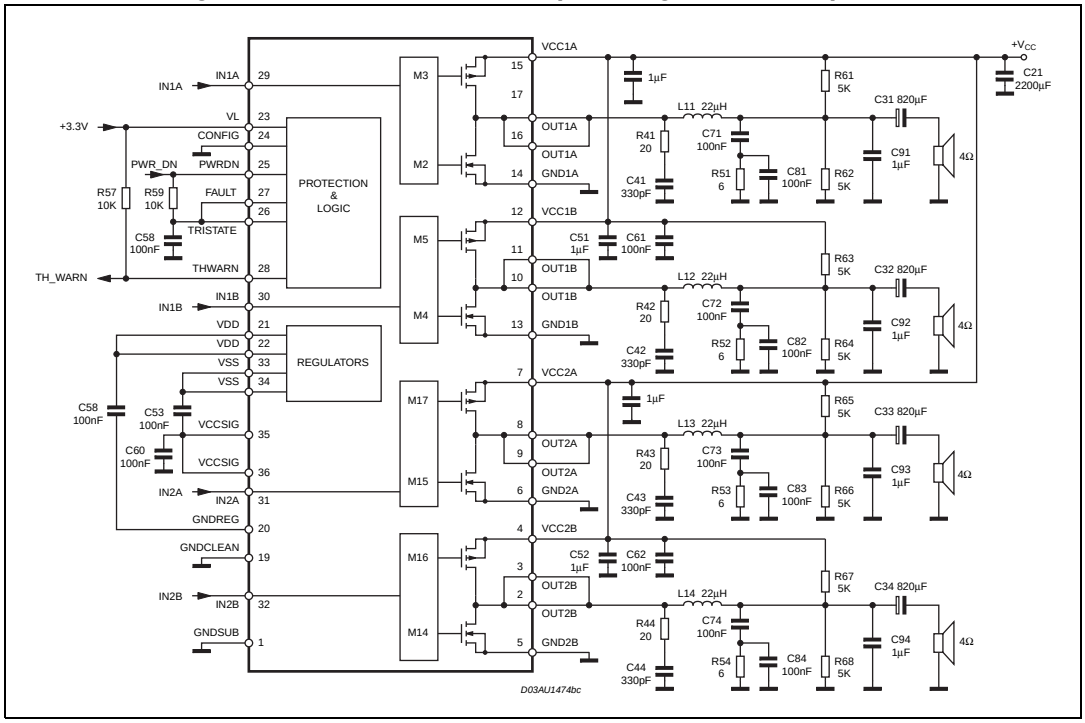
The STA515W comes in a 36-pin PowerSSO package with exposed pad down (EPD).

Table 1. Device summary

Order code	Ambient temp. range	Package	Packaging
STA515W13TR	0 to 70 °C	PowerSSO36 EPD	Tape and reel

1 Introduction

Figure 1. STA515W circuit for quad single-ended amplifiers



2 Pin description

Figure 2. Pin out

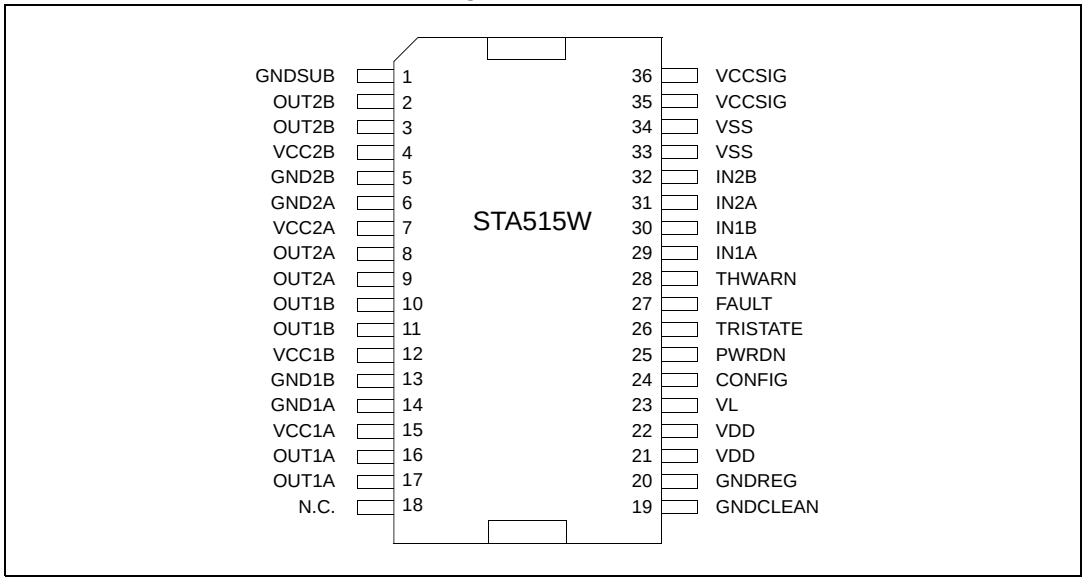


Table 2. Pin list

Pin	Name	Type	Description
1	GNDSUB	PWR	Substrate ground
2, 3	OUT2B	O	Output half bridge 2B
4	VCC2B	PWR	Positive supply
5	GND2B	PWR	Negative supply
6	GND2A	PWR	Negative supply
7	VCC2A	PWR	Positive supply
8, 9	OUT2A	O	Output half bridge 2A
10, 11	OUT1B	O	Output half bridge 1B
12	VCC1B	PWR	Positive supply
13	GND1B	PWR	Negative supply
14	GND1A	PWR	Negative supply
15	VCC1A	PWR	Positive supply
16, 17	OUT1A	O	Output half bridge 1A
18	N.C.	-	No internal connection
19	GNDCLEAN	PWR	Logical ground
20	GNDREG	PWR	Ground for regulator V_{DD}
21, 22	VDD	PWR	5-V regulator referred to ground
23	VL	PWR	High logical state setting voltage, V_L

Table 2. Pin list (continued)

Pin	Name	Type	Description
24	CONFIG	I	Configuration pin: 0: normal operation 1: bridges in parallel, see *Parallel-output and high-current operation on page 10*
25	PWRDN	I	Stand-by pin: 0: low-power mode 1: normal operation
26	TRISTATE	I	Hi-Z pin: 0: all power amplifier outputs in high-impedance state 1: normal operation
27	FAULT	O	Fault pin advisor (open-drain device, needs pull-up resistor): 0: fault detected (short circuit or thermal, for example) 1: normal operation
28	THWARN	O	Thermal-warning advisor (open-drain device, needs pull-up resistor): 0: temperature of the IC >130 ^{o}C 1: normal operation
29	IN1A	I	Input of half bridge 1A
30	IN1B	I	Input of half bridge 1B
31	IN2A	I	Input of half bridge 2A
32	IN2B	I	Input of half bridge 2B
33, 34	VSS	PWR	5-V regulator referred to +V_{CC}
35, 36	VCCSIG	PWR	Signal positive supply

3 Electrical characteristics

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage (Pins 4, 7, 12, 15)	40	V
V_{max}	Maximum voltage on pins 23 to 32	5.5	V
T_{op}	Operating temperature range	0 to 70	°C
P_{tot}	Power dissipation (Tcase = 70 °C)	21	W
T_{stg}, T_j	Storage and junction temperature	-40 to 150	°C

Table 4. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	DC supply voltage (Pins 4, 7, 12, 15)	10	-	36	V
V_L	Input logic reference	2.7	3.3	5.0	V
T_{amb}	Ambient temperature	0	-	70	°C

Table 5. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$T_{j\text{-}case}$	Thermal resistance junction to case (thermal pad)	-	-	1.5	°C/W
T_{jSD}	Thermal shut-down junction temperature	-	150	-	°C
T_{warn}	Thermal warning temperature	-	130	-	°C
t_{hSD}	Thermal shut-down hysteresis	-	25	-	°C

Unless otherwise stated, the test conditions for *Table 6* below are V_L = 3.3 V, V_{CC} = 30 V, R_L = 8 Ω, f_{SW} = 384 kHz and T_{amb} = 25 °C

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
R_{dsON}	Power P-channel/N-channel MOSFET R_{dsON}	I_{dd} = 1 A	-	200	270	mΩ
I_{dss}	Power P-channel/N-channel leakage Idss	V_{CC} = 35 V	-	-	50	µA
g_N	Power P-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
g_P	Power N-channel R_{dsON} matching	I_{dd} = 1 A	95	-	-	%
Dt_s	Low current dead time (static)	see *Figure 3*	-	10	20	ns

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Dt_d	High current dead time (dynamic)	L = 22 µH, C = 470 nF R_L = 8 Ω, I_{dd} = 3.0 A see *Figure 4*	-	-	50	ns
$t_{d\ ON}$	Turn-on delay time	Resistive load	-	-	100	ns
$t_{d\ OFF}$	Turn-off delay time	Resistive load	-	-	100	ns
t_r	Rise time	Resistive load see *Figure 3*	-	-	25	ns
t_f	Fall time	Resistive load see *Figure 3*	-	-	25	ns
V_{CC}	Supply operating voltage	-	10	-	36	V
$V_{IN\text{-}Low}$	Half-bridge input, low level voltage	-	-	-	V_L / 2 - 300 mV	V
$V_{IN\text{-}High}$	Half-bridge input, high level voltage	-	V_L / 2 + 300 mV	-	-	V
$I_{IN\text{-}H}$	High level input current	$V_{IN} = V_L$	-	1	-	µA
$I_{IN\text{-}L}$	Low level input current	V_{IN} = 0.3 V	-	1	-	µA
$I_{PWRDN\text{-}H}$	High level PWRDN pin input current	V_L = 3.3 V	-	35	-	µA
V_{Low}	Low logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V	-	-	0.8	V
V_{High}	High logical state voltage (pins PWRDN, TRISTATE) (see *Table 7*)	V_L = 3.3 V	1.7	-	-	V
$I_{VCC\text{-}PWRDN}$	Supply current from V_{CC} in power down	V_{PWRDN} = 0 V	-	-	3	mA
I_{FAULT}	Output current on pins FAULT, THWARN with fault condition	V_{pin} = 3.3 V	-	1	-	mA
$I_{VCC\text{-}HiZ}$	Supply current from V_{CC} in 3-state	$V_{TRISTATE}$ = 0 V	-	22	-	mA
I_{VCC}	Supply current from V_{CC} in operation (both channels switching)	Input pulse width = 50% duty, switching frequency = 384 kHz, no LC filters	-	50	-	mA
I_{OCP}	Overcurrent protection threshold Isc (short circuit current limit)	-	3	6	-	A
V_{UVP}	Undervoltage protection threshold	-	-	7	-	V
t_{pw_min}	Output minimum pulse width	No load	70	-	150	ns

Table 7. Threshold switching voltage variation with voltage on pin VL

Voltage on pin VL, V_L	V_{LOW} max	V_{HIGH} min	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5.0	0.85	1.85	V

Table 8. Logic truth table

Pin TRISTATE	Inputs as per *Figure 4*		Transistors as per *Figure 4*				Output mode
	INxA	INxB	Q1	Q2	Q3	Q4	
0	x	x	Off	Off	Off	Off	Hi Z
1	0	0	Off	Off	On	On	Dump
1	0	1	Off	On	On	Off	Negative
1	1	0	On	Off	Off	On	Positive
1	1	1	On	On	Off	Off	Not used

4 Test circuits

Figure 3. Test circuit

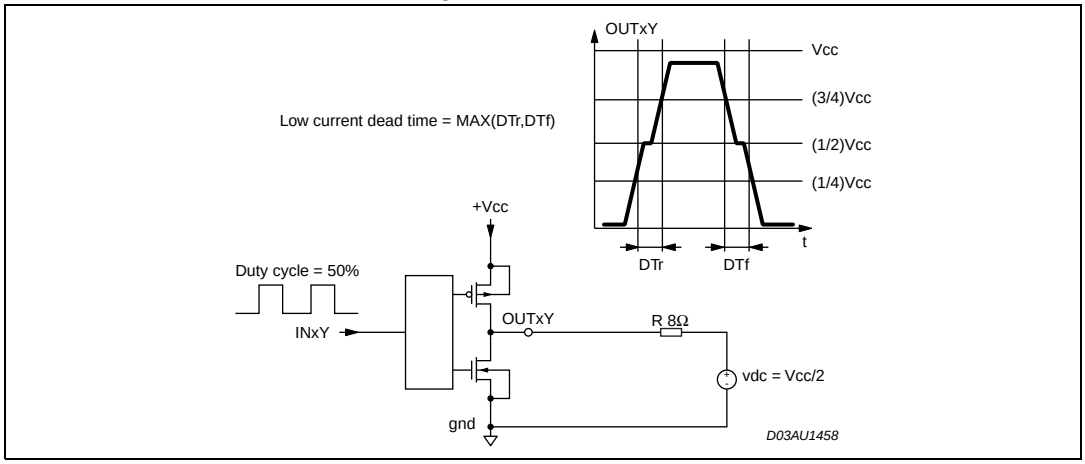
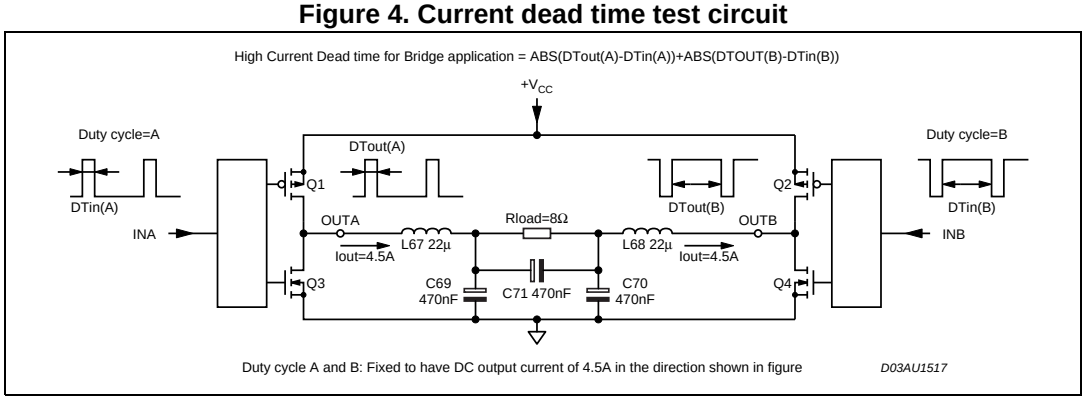


Figure 4. Current dead time test circuit



5 Application information

The STA515W is a dual channel H-bridge that can deliver 20 W per channel into 8 Ω with 10% THD at V_{CC} = 18 V with high efficiency.

The STA515W converts both DDX and binary-logic-controlled PWM signals into audio power at the load. It includes a logic interface, integrated bridge drivers, high efficiency MOSFET outputs and thermal and short-circuit protection circuitry.

In DDX mode, two logic-level signals per channel are used to control the high-speed MOSFET switches which drive the speaker load in a bridge configuration, according to the damped ternary modulation operation.

In binary mode, both full-bridge and half-bridge modes are supported.

The STA515W includes overcurrent and thermal protection as well as an undervoltage lockout with automatic recovery. A thermal warning status is also provided.

Figure 5. Block diagram for DDX or binary modes

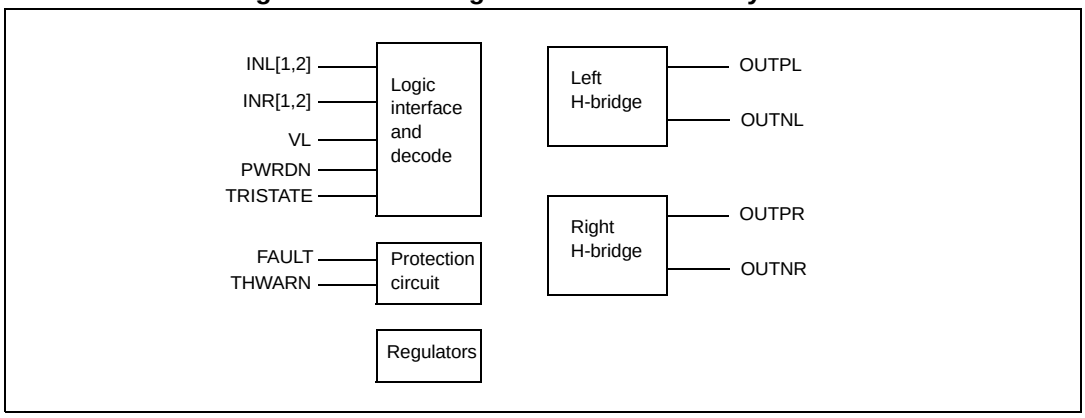
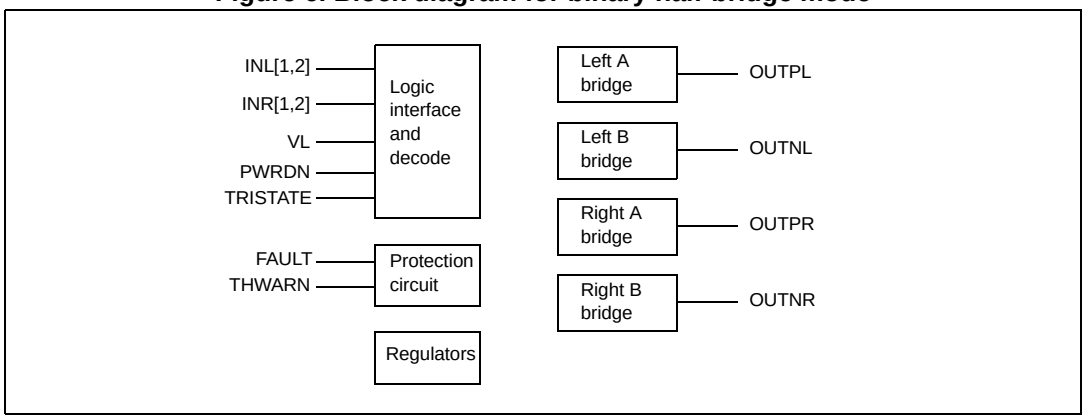


Figure 6. Block diagram for binary half-bridge mode



Logic interface and decode

The STA515W power outputs are controlled using one or two logic-level timing signals. In order to provide a proper logic interface, pin VL must operate at the same voltage as the DDX control logic supply.

Protection circuits

The STA515W includes protection circuitry for overcurrent and thermal overload conditions. A thermal warning pin (THWARN) is activated low (open-drain MOSFET) when the IC temperature exceeds 130 °C, which is in advance of the thermal shutdown protection. When a fault condition is detected an internal fault signal acts to immediately disable the output power MOSFETs, placing both H-bridges in the high-impedance state. At the same time an open-drain MOSFET connected to pin FAULT is switched on.

There are two possible modes subsequent to activating a fault:

- Shutdown mode:
  with pins FAULT (with pull-up resistor) and TRISTATE independent, an activated fault disables the device, signalling low at pin FAULT.
  The device may subsequently be reset to normal operation by toggling pin TRISTATE from high to low and back to high using an external logic signal.
- Automatic recovery mode:
  This is shown in the applications circuit in *Figure 7* and *Figure 7 on page 11*.
  Pins FAULT and TRISTATE are shorted together and connected to a time constant circuit comprising R59 and C58.
  An activated fault forces a reset on pin TRISTATE causing normal operation to resume following a delay determined by the time constant of the circuit.
  If the fault condition is still present, the circuit operation continues, repeating until the fault condition is removed.
  An increase in the time constant of the circuit produces a longer recovery interval.

Care must be taken in the overall system design so as not to exceed the protection thresholds under normal operation.

Power outputs

The STA515W power and output pins are duplicated to provide a low-impedance path for the device bridged outputs. All duplicated power, ground and output pins must be connected for proper operation.

Pins PWRDN or TRISTATE should be used to set all MOSFETS to the high-impedance state during power-up and until the logic power supply, VL, has settled.

Parallel-output and high-current operation

When using DDX mode, the STA515W outputs can be connected in parallel to increase the output current capability. In this configuration the device can provide 40 W into 8 Ω.

This mode of operation is enabled with pin CONFIG connected to VDD. The inputs must be combined to give INLA = INLB and INRA = INRB, then the corresponding outputs can be shorted together to give OUTLA = OUTLB and OUTRA = OUTRB.

Output filter

A passive 2nd-order filter is used on the STA515W power outputs to reconstruct an analog audio signal. The system performance can be significantly affected by the output filter design and choice of passive components.

Filter designs for 4-Ω and 8-Ω loads are shown in the applications circuits of *Figure 1 on page 2* for the half-bridge mode, and *Figure 7* and *Figure 8 on page 11* for the full bridge.

Applications circuits

Figure 7 below shows a typical full-bridge circuit for supplying 20 W + 20 W into 8 Ω speakers with 10% THD at V_{CC} = 18 V.

Figure 7. Typical stereo full-bridge configuration for 20 + 20 W

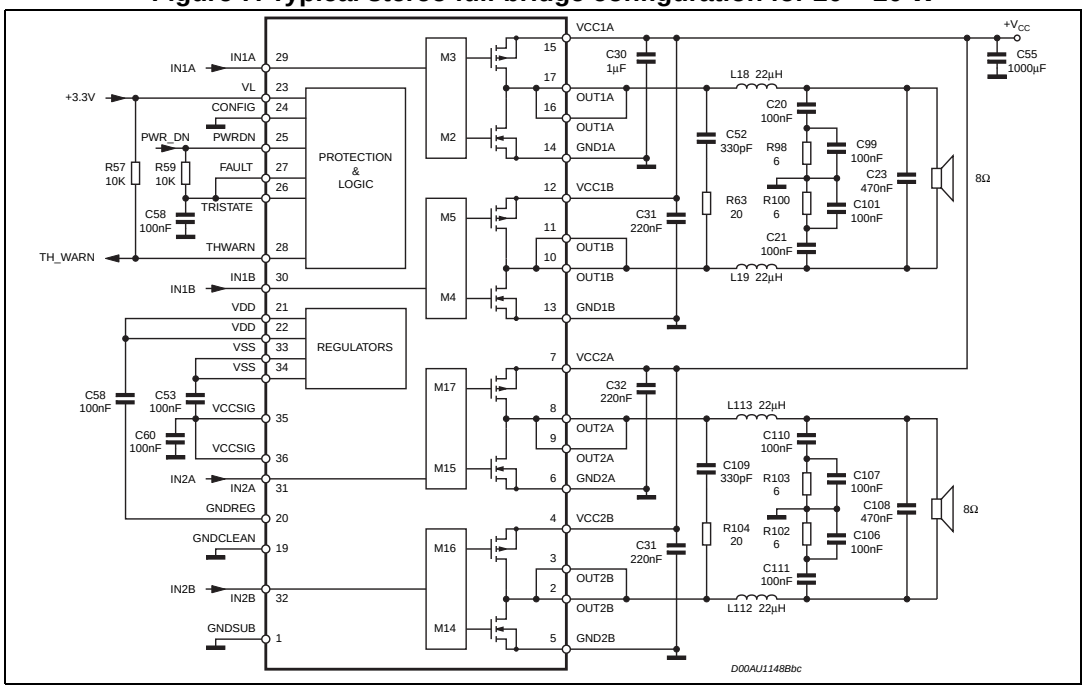
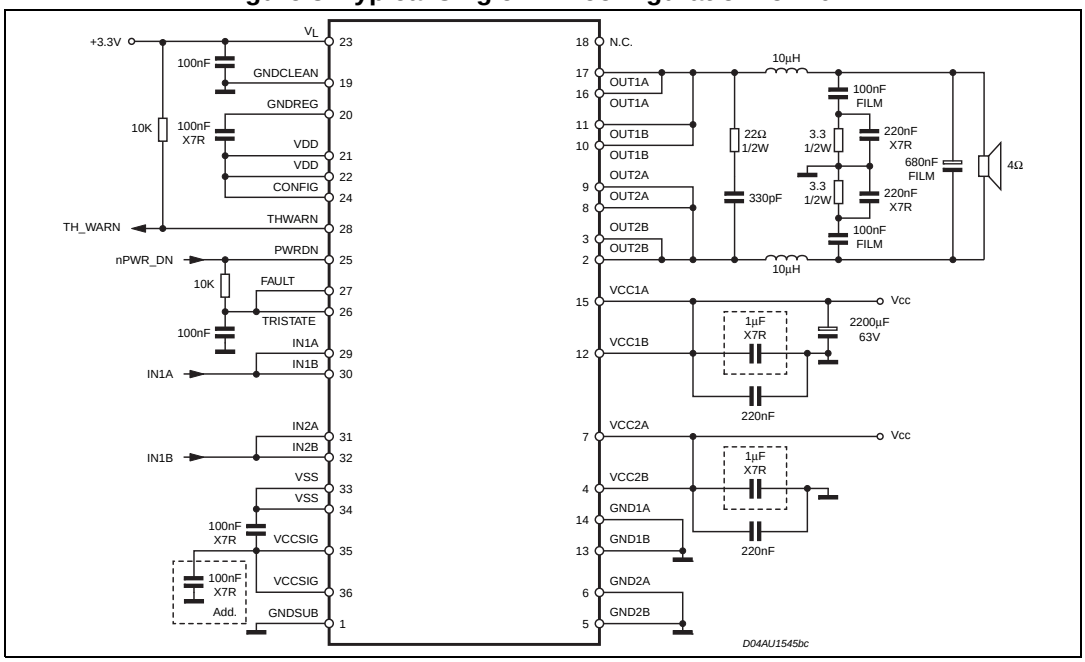


Figure 8 below shows a single-BTL configuration capable of supplying 40 W into a 4 Ω load at 10% THD with V_{CC} = 19 V. This result was obtained with peak power for <1 s using the STA308+STA515W+STA50X demo board. A PWM modulator as driver is required.

Figure 8. Typical single-BTL configuration for 40 W



6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

The STA515W comes in a 36-pin PowerSSO package with exposed pad down (EPD).

Figure 9 below shows the package outline and *Table 9* gives the dimensions.

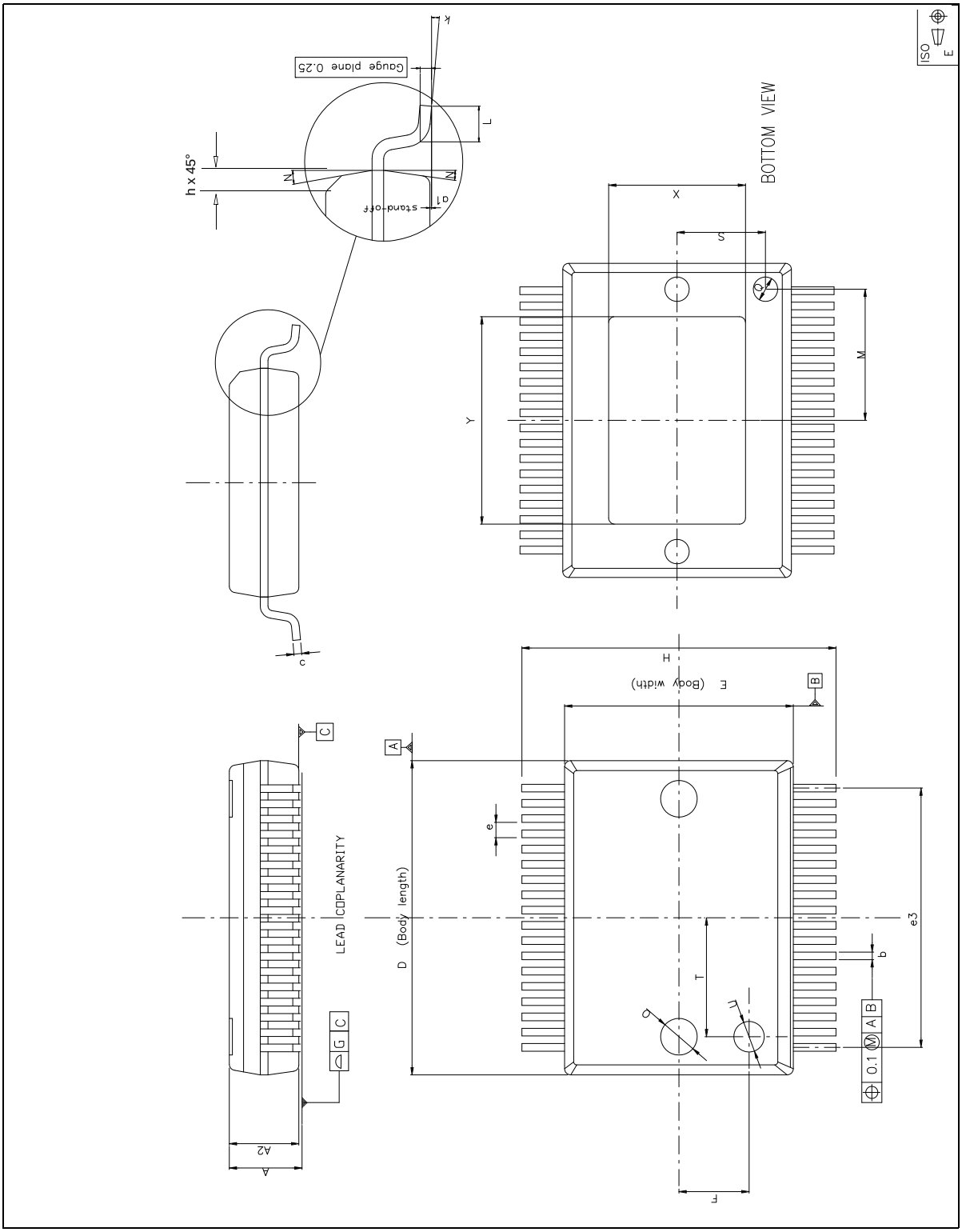


Figure 9. PowerSSO36 EPD outline drawing

Table 9. PowerSSO36 EPD dimensions

Symbol	Dimensions in mm			Dimensions in inches		
	Min	Typ	Max	Min	Typ	Max
A	2.15	-	2.47	0.085	-	0.097
A2	2.15	-	2.40	0.085	-	0.094
a1	0.00	-	0.10	0.000	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.60	-	1.00	0.024	-	0.039
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	6.50	-	7.10	0.256	-	0.280

7 Revision history

Table 10. Document revision history

Date	Revision	Changes
Nov-2004	1	Initial release.
27-Apr-2010	2	Added order code STA515W13TR Modified *Figure 1 on page 2* Reconstructed pin list in *Table 2 on page 3* with information from former table 3 Functional pin status Updated Vlow and Vhigh spec in *Table 6 on page 5* Modified *Figure 3* and *Figure 4 on page 8* Updated applications circuits in *Figure 7* and *Figure 8 on page 11*
24-Feb-2014	3	Updated order code *Table 1 on page 1*

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