AST1S31HF

Up to 4 V, 3 A step-down 2.3 MHz switching regulator for automotive applications

Datasheet - production data

Features

- AECQ100 qualified
- 3 A DC output current
- 2.8 V to 4 V input voltage
- Output voltage adjustable from 0.8 V
- 2.3 MHz switching frequency
- Internal soft-start and enable
- Integrated 70 mΩ and 55 mΩ power MOSFETs
- All ceramic capacitor
- Power Good (POR)
- Cycle-by-cycle current limiting
- Current foldback short-circuit protection
- VFDFPN 3 x 3 - 8L package

Applications

- Designed for automotive systems
- Battery powered applications
- Car body applications

Description

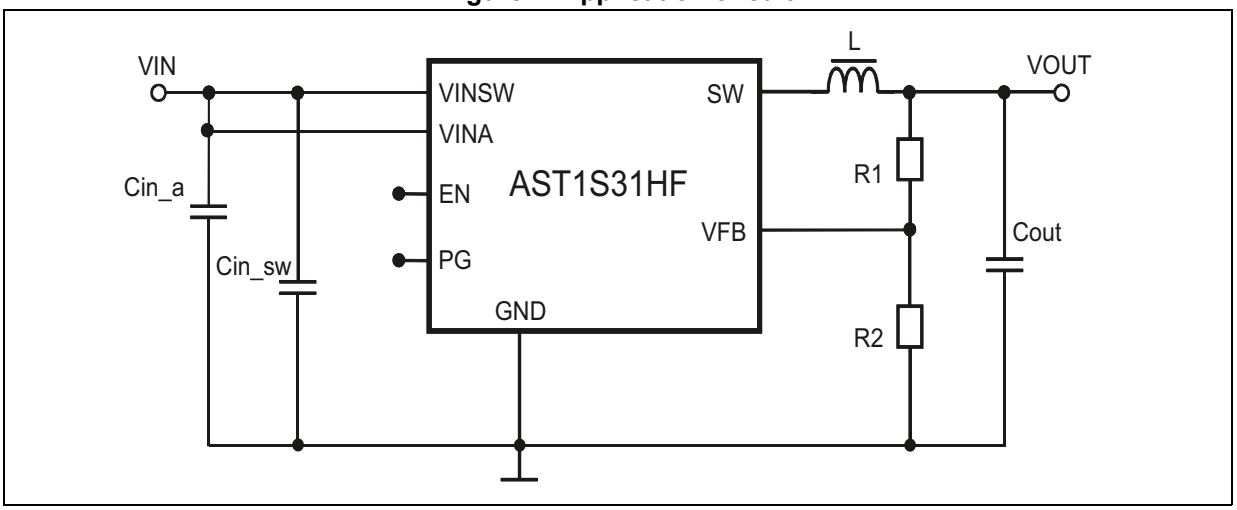
The AST1S31HF is an internally compensated 2.3 MHz fixed frequency PWM synchronous step-down regulator. The AST1S31HF operates from 2.8 V to 4 V input, while it regulates an output voltage as low as 0.8 V and up to V_{IN}.

The AST1S31HF device integrates a 70 mΩ high-side switch and a 55 mΩ synchronous rectifier allowing very high efficiency with very low output voltages.

The peak current mode control with internal compensation deliver a very compact solution with a minimum component count.

The AST1S31HF is available in a 3 mm x 3 mm, 8-lead VFDFPN package.

Figure 1. Application circuit



Contents

1 **Pin settings 4**
1.1 Pin connection 4
1.2 Pin description 4

2 **Maximum ratings 5**
2.1 Thermal data 5
2.2 ESD performance 5

3 **Electrical characteristics 6**

4 **Datasheet parameters over the temperature range 7**

5 **Functional description 8**
5.1 Output voltage adjustment 9
5.2 Soft-start 10
5.3 Error amplifier and control loop stability 10
5.4 Overcurrent protection 15
5.5 Enable function 17
5.6 Light-load operation 17
5.7 Hysteretic thermal shutdown 17

6 **Application information 18**
6.1 Input capacitor selection 18
6.2 Inductor selection 19
6.3 Output capacitor selection 20
6.4 Thermal dissipation 21
6.5 Layout consideration 22

7 **Demonstration board 24**

8 **Typical characteristics 26**

9 **Package information 29**

9.1 VFDFPN8 (3 x 3 x 1.0 mm) package information 30

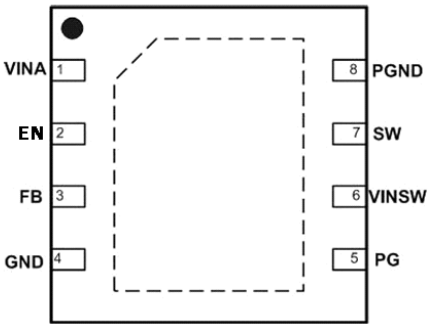
10 Order codes 31

11 Revision history 32

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

No.	Type	Description
1	VINA	Unregulated DC input voltage
2	EN	Enable input. With EN higher than 1.5 V the device in ON and with EN lower than 0.5 V the device is OFF.
3	FB	Feedback input. Connecting the output voltage directly to this pin the output voltage is regulated at 0.8 V. To have higher regulated voltages an external resistor divider is required from Vout to the FB pin.
4	AGND	Ground
5	PG	Open drain Power Good (POR) pin. It is released (open drain) when the output voltage is higher than 0.92 * V_{OUT} with a delay of 170 µs. If the output voltage is below 0.92 * V_{OUT}, the POR pin goes to low impedance immediately. If not used, it can be left floating or to GND.
6	VINSW	Power input voltage
7	SW	Regulator output switching pin
8	PGND	Power ground
9	ePAD	Exposed pad connected to ground

2 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to 5	V
V_{EN}	Enable voltage	-0.3 to V_{IN}	
V_{SW}	Output switching voltage	-1 to V_{IN}	
V_{PG}	Power-on reset voltage (Power Good)	-0.3 to V_{IN}	
V_{FB}	Feedback voltage	-0.3 to 1.5	
P_{TOT}	Power dissipation at T_A < 60 °C	2.25	W
T_{OP}	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	-55 to 150	°C

2.1 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
R_{thJA}	Maximum thermal resistance junction ambient(1)	VFDFPN	50	°C/W

1. Package mounted on demonstration board.

2.2 ESD performance

Table 4. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	± 2	kV
		CDM corner pins	± 750	V
		CDM non-corner pins	± 500	

3 Electrical characteristics

T_J = -40 °C to 125 °C, V_{IN} = 4 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Values			Unit
			Min.	Typ.	Max.	
V_{IN}	Operating input voltage range		2.8		4	V
V_{INON}	Turn-on V_{CC} threshold		2.3	2.45	2.6	
V_{INOFF}	Turn-off V_{CC} threshold		1.85	2.0	2.15	
R_{DSON}-P	High-side switch on-resistance	I_{SW} = 300 mA, T_J = 25 °C		70	110	mΩ
		I_{SW} = 300 mA			140	
R_{DSON}-N	Low-side switch on- resistance	I_{SW} = 300 mA, T_J = 25 °C		55	90	mΩ
		I_{SW} = 300 mA			110	
I_{LIM}	Maximum limiting current		3.6		6.0	A
Oscillator						
F_{SW}	Switching frequency		1.75	2.3	2.5	MHz
Dynamic characteristics						
V_{FB}	Feedback voltage	I_{LOAD} = 0 A	0.79	0.8	0.81	V
DC characteristics						
I_Q	Quiescent current	Duty cycle = 0, no load V_{FB} = 1.2 V		630	1200	µA
I_{QST-BY}	Total standby quiescent current	OFF			1	µA
Enable						
V_{EN}	EN threshold voltage	Device ON level	1.5			V
		Device OFF level			0.5	
I_{EN}	EN current				0.1	µA
Power Good						
PG	PG threshold		92	94	96	$\%V_{FB}$
	PG output voltage low	Isink = 6 mA open drain			400	mV
	PG rise delay			170		µs
Soft-start						
T_{SS}	Soft-start duration			400		µs
Protection						
T_{SHDN}	Thermal shutdown	(1)		150		°C
	Hystereris	(1)		20		

1. Guaranteed by design.

4 Datasheet parameters over the temperature range

The 100% of the population in the production flow is tested at three different ambient temperatures (-40 °C, +25 °C, +125 °C) to guarantee the datasheet parameters inside the junction temperature range (-40 °C, +125 °C).

The device operation is guaranteed when the junction temperature is inside the (-40 °C, +125 °C) temperature range. The designer can estimate the silicon temperature increase respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the TSHDN (+150 °C typ.) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase because of self-heating.

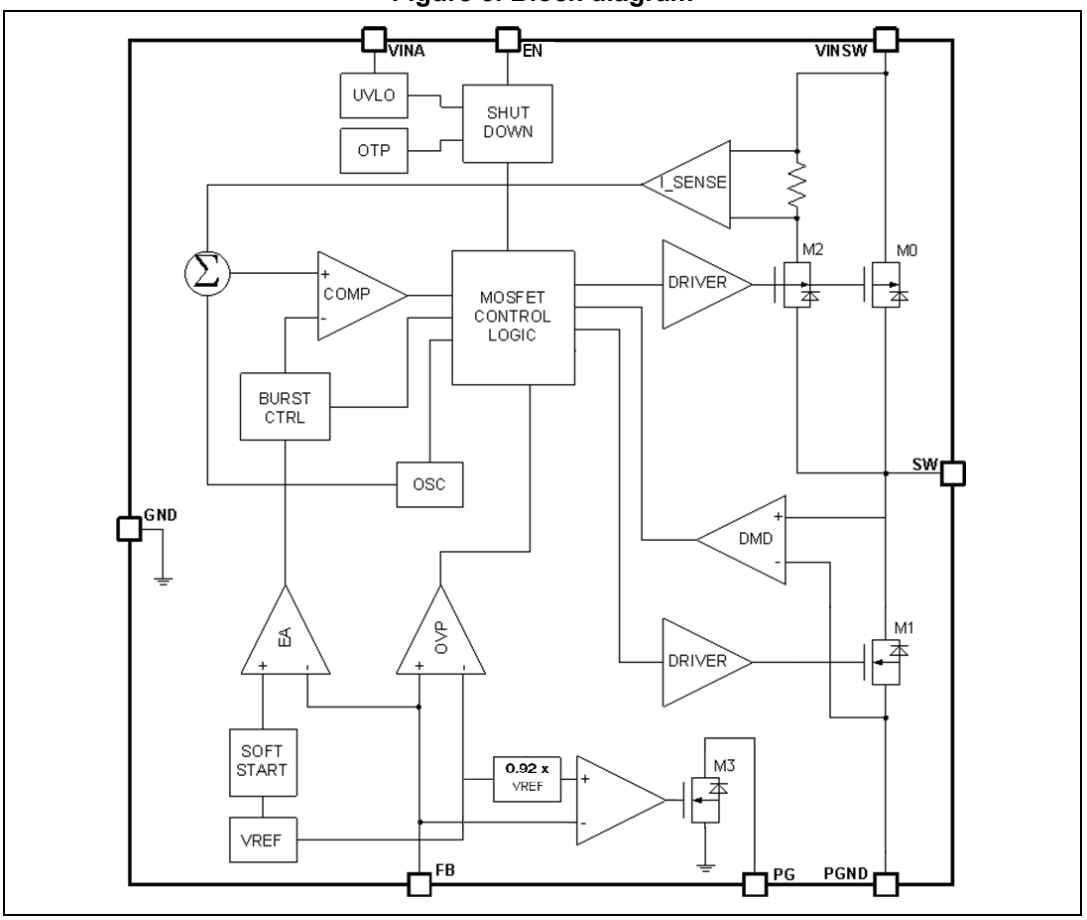
5 Functional description

The AST1S31HF device is based on a “peak current mode”, constant frequency control. The output voltage V_{OUT} is sensed by the feedback pin (FB) compared to an internal reference (0.8 V) providing an error signal that, compared to the output of the current sense amplifier, controls the ON and OFF time of the power switch.

The main internal blocks are shown in the block diagram in *Figure 3*. They are:

- A fully integrated oscillator that provides the internal clock and the ramp for the slope compensation avoiding sub-harmonic instability
- The soft-start circuitry to limit the inrush current during the start-up phase
- The transconductance error amplifier
- The pulse width modulator and the relative logic circuitry necessary to drive the internal power switches
- The drivers for embedded P-channel and N-channel power MOSFET switches
- The high-side current sensing block
- The low-side current sense to implement diode emulation
- The voltage monitor circuitry (UVLO) that checks the input and internal voltages
- The thermal shutdown block, to prevent the thermal runaway.

Figure 3. Block diagram



5.1 Output voltage adjustment

The error amplifier reference voltage is 0.8 V typical. The output voltage is adjusted according to the following formula (see *Figure 1 on page 1*):

Equation 1

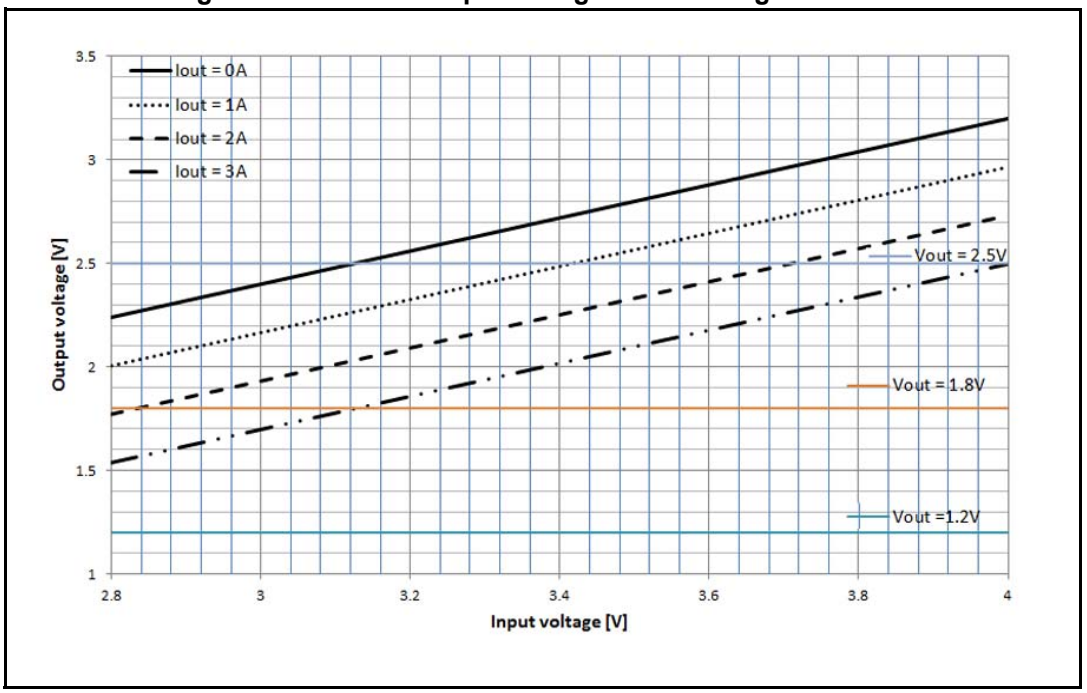
$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

The internal architecture of the device requires a minimum off time, cycle by cycle, for the output voltage regulation. The minimum off time is typically equal to 66 ns.

The control loop compensates for conversion losses with duty cycle control. Since the power losses are proportional to the delivered output power, the duty cycle increases with the load current request.

Figure 4 shows at different loading conditions the maximum regulated output voltage over the input voltage range.

Figure 4. Maximum output voltage over loading conditions



5.2 Soft-start

The soft-start is essential to assure the correct and safe start-up of the step-down converter. It avoids the inrush current surge and makes the output voltage rise monothonically.

The soft-start is managed ramping the reference of the error amplifier from 0 V to 0.8 V. The internal soft-start capacitor is charged with a resistor to 0.8 V, then the FB pin follows the reference so that the output voltage is regulated to rise to the set value monothonically.

5.3 Error amplifier and control loop stability

The error amplifier provides the error signal to be compared with the high-side switch current through the current sense circuitry. The non-inverting input is connected with the internal 0.8 V reference, whilst the inverting input is the FB pin. The compensation network is internal and connected between the E/A output and GND.

The error amplifier of the AST1S31HF is a transconductance operational amplifier, with high bandwidth and high output impedance.

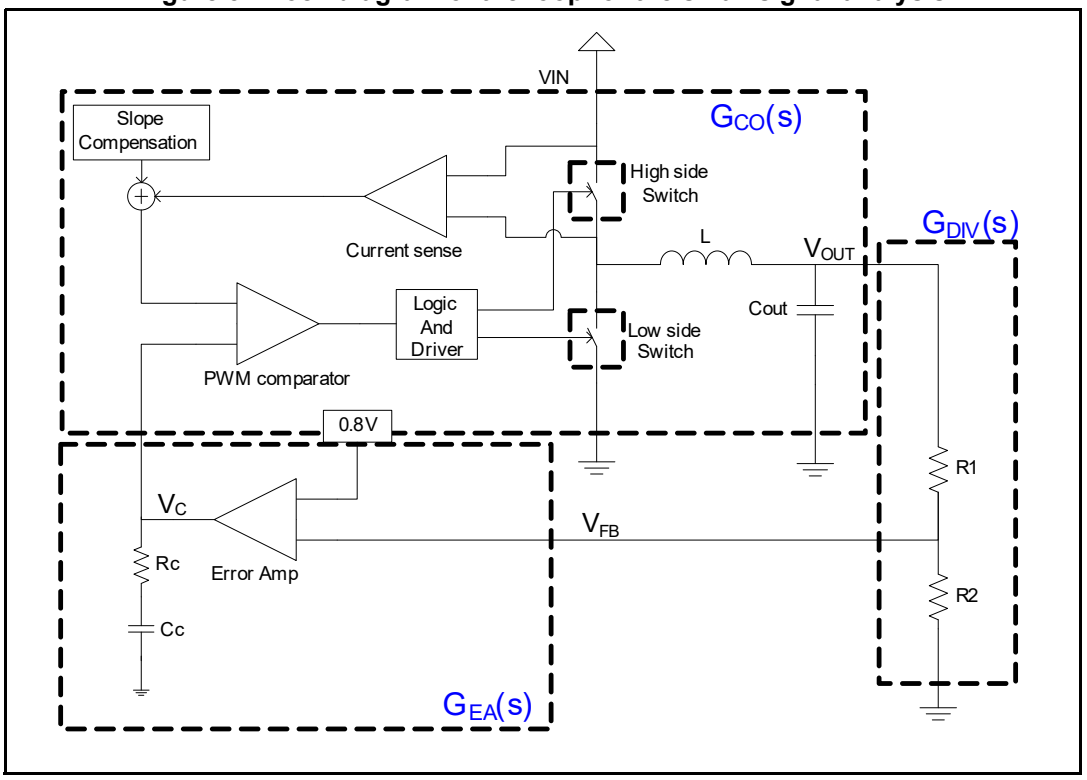
Table 6. Characteristics of the uncompensated error amplifier

Description	Value
DC gain	87 dB
gm	236 μA/V
Ro	98 MΩ

The AST1S31HF device embeds the compensation network that assures the stability of the loop in the whole operating range. In *Section 5.7 on page 17* all the tools needed to check the loop stability are shown.

In *Figure 5* is shown the simple small signal model for the peak current mode control loop.

Figure 5. Block diagram of the loop for the small signal analysis



Three main terms can be identified to obtain the loop transfer function:

1. From control (output of E/A) to output, $G_{CO}(s)$
2. From output (Vout) to the FB pin, $G_{DIV}(s)$
3. From the FB pin to control (output of E/A), $G_{EA}(s)$.

The transfer function from control to output $G_{CO}(s)$ results:

Equation 2

$$G_{CO}(s) = \frac{R_{LOAD}}{R_i} \cdot \frac{1}{1 + \frac{R_{out} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)} \cdot F_H(s)$$

where R_{LOAD} represents the load resistance, R_i the equivalent sensing resistor of the current sense circuitry (0.38 Ω), ω_p the single pole introduced by the LC filter and ω_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

Equation 3

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}}$$

Equation 4

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

Equation 5

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{pp} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i \end{cases}$$

S_n represents the ON time slope of the sensed inductor current, S_e the slope of the external ramp (V_{PP} peak-to-peak amplitude - 0.55 V) that implements the slope compensation to avoid sub-harmonic oscillations at the duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

Equation 6

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

Equation 7

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]}$$

and:

Equation 8

$$\omega_n = \pi \cdot f_{SW}$$

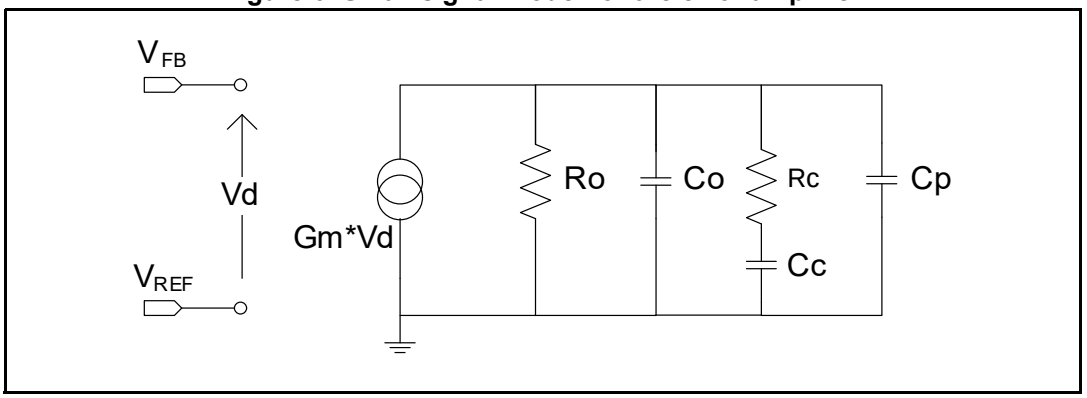
The resistor to adjust the output voltage gives the term from output voltage to the FB pin. $G_{DIV}(s)$ is:

Equation 9

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2}$$

The transfer function from FB to Vc (output of E/A) introduces the singularities (poles and zeroes) to stabilize the loop. In *Figure 6* the small signal model of the error amplifier with the internal compensation network is shown.

Figure 6. Small signal model for the error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability and can be neglected.

So $G_{EA}(s)$ results:

Equation 10

$$G_{EA}(s) = \frac{G_{EA0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

Where $G_{EA} = G_m \cdot R_o$.

The poles of this transfer function are (if $C_c >> C_0 + C_P$):

Equation 11

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

Equation 12

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

Equation 13

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is R_C = 80 kΩ, C_C = 55 pF while C_P and C_O can be considered as negligible. The error amplifier output resistance is 98 MΩ so the relevant singularities are:

Equation 14

$$f_Z = 36,2\ \text{kHz} \qquad f_{P\,LF} = 13,6\ \text{Hz}$$

So closing the loop the loop gain $G_{LOOP}(s)$ is:

Equation 15

$$G_{LOOP}(s) = G_{CO}(s) \cdot G_{DIV}(s) \cdot G_{EA}(s)$$

Example:

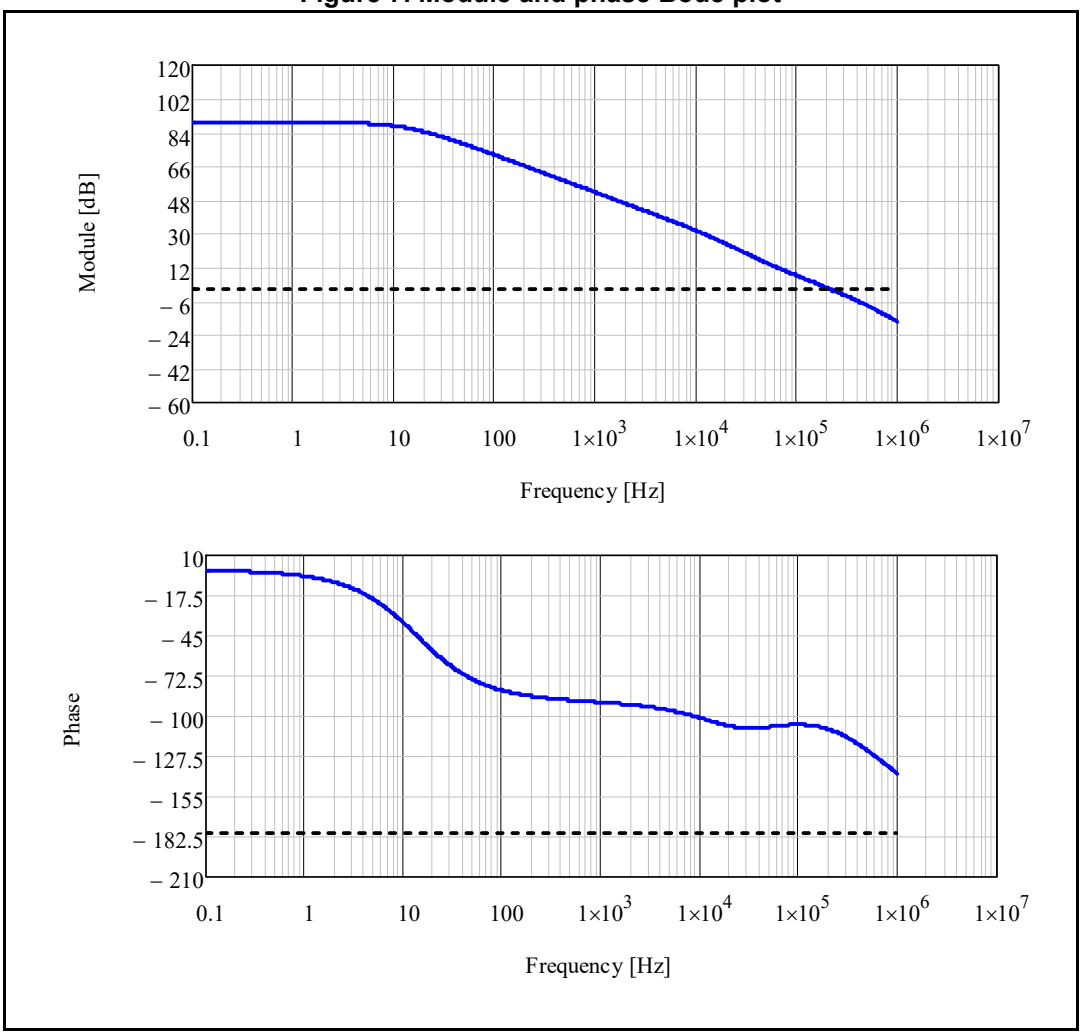
VIN = 3.3 V, VOUT = 1.2 V, Iomax = 3 A, L = 0.91 µH, Cout = 22 µF (MLCC),

R1 = 100 kΩ, R2 = 200 kΩ (see Section 6.2 on page 19 and Section 6.3 on page 20 for inductor and output capacitor selection guidelines).

The module and phase Bode plot are reported in Figure 7.

The bandwidth is 230 kHz and the phase margin is 70 degrees.

Figure 7. Module and phase Bode plot



5.4 Overcurrent protection

The AST1S31 device implements overcurrent protection sensing the current flowing through the high-side current switch.

If the current exceeds the overcurrent threshold the high-side is turned off, implementing cycle-by-cycle current limitation. Since the regulation loop is no more fixing the duty cycle, the output voltage is unregulated and the FB pin falls accordingly to the new duty cycle.

The mechanism to adjust the switching under the current foldback condition exploits the low-side current sense circuitry.

If FB is lower than 0.2 V, the high-side power MOSFET is turned off after the minimum conduction time (approximately 100 nsec typ.), then, after a proper deadtime that avoids the cross conduction, the low-side is turned on until the low-side current is lower than a valley threshold (1.5 A typ.). Once the low-side is turned off the high-side is immediately turned on.

In this way the frequency is adjusted to keep the inductor current ripple between peak current value that could be evaluated with the following equation:

Equation 16

$$I_{Peak} = I_{Valley} + \frac{V_{In} + V_{Out} - (DCR_L + R_{DS(on)HS}) \times I_{Valley}}{L} \times (T_{Onmin})$$

where DCR_L is the series resistance of the inductor and the measured value of the valley current threshold (1.5 A typ.), so properly limiting the output current in case of the overcurrent or short-circuit .

The overcurrent protection is always effective when VFB < 0.2 V thanks to the natural frequency reduction.

No frequency foldback is otherwise implemented when VFB > 0.2 V. In this case, when the current ripple during the on phase is bigger than the one during the off phase, there will be a peak current level higher than the current limit threshold.

The following equations show the inductor current ripple during the ON and OFF phases in case of overcurrent condition:

On phase:

Equation 17

$$\Delta I_{Ton} = \frac{V_{In} - V_{Out} - (DCR_L + R_{DS(on)HS}) \times I}{L} \times (T_{Onmin})$$

Where:

Equation 18

$$V_{Out} = V_{FB} \times \frac{V_{OUTSet}}{0.8}$$

It's also possible define the output voltage in function of input voltage, on phase time and switching frequency:

Equation 19

$$V_{OUTSet} = V_{IN} \times D_{MIN} = V_{IN} \times \frac{T_{OnMin}}{T_{SW}}$$

So the on phase the equation results:

Equation 20

$$\Delta I_{TON}(V_{FB}) = \frac{V_{IN} - V_{FB} \times \frac{V_{IN} \times T_{ONMin}}{0.8 \times T_{SW}} - (DCR_L + R_{DS(ON)HighSide}) \times I}{L} \times T_{ONMin}$$

Off phase:

Equation 21

$$\Delta I_{TOFF} = \frac{-(R_{DS(ON)LowSide} + DCR_L) \times I - V_{OUT}}{L} \times T_{SW}$$

It is possible to repeat the considerations realized to the on phase equation. So it's possible to write the off phase equation in the following manner:

Equation 22

$$\Delta I_{TOFF}(V_{FB}) = \frac{-(R_{DS(ON)LowSide} + DCR_L) \times I - V_{FB} \times \frac{V_{IN} \times T_{ONMin}}{0.8 \times T_{SW}}}{L} \times T_{SW}$$

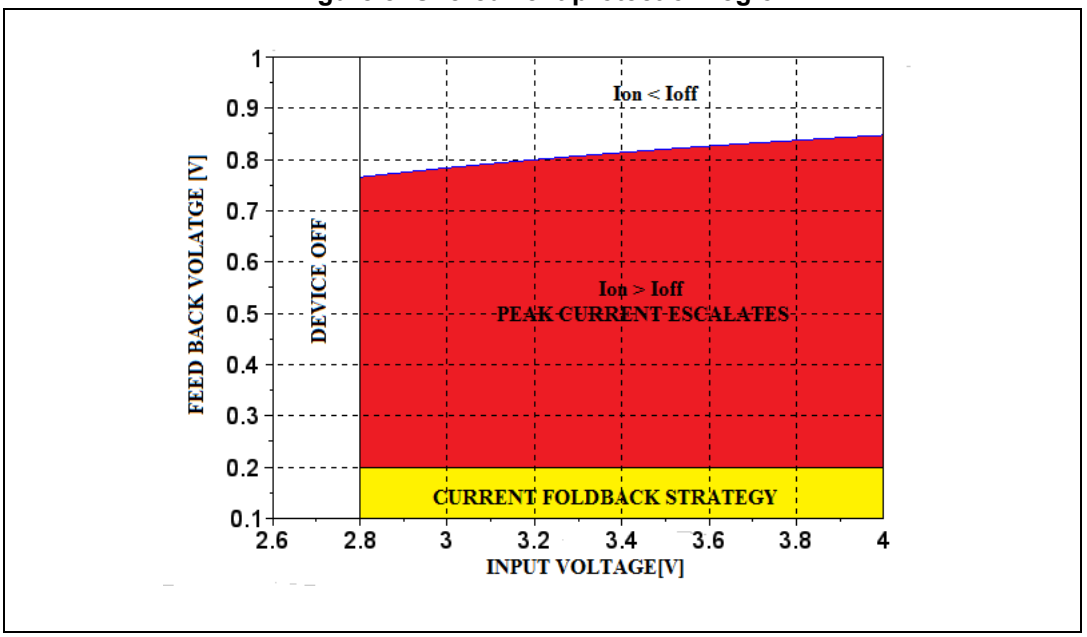
The peak current escalates over the peak current threshold (called "OCP1") if :

Equation 23

$$\Delta I_{TON}(V_{FB}) > \Delta I_{TOFF}(V_{FB})$$

In case the current escalates up to a further current threshold (called "OCP2"), slightly higher than OCP1, the converter stops the switching activity, the reference of the error amplifier is pulled down and then it restarts with a new soft-start procedure. If the overcurrent condition is still active, the current foldback with frequency reduction properly limit the output current.

Figure 8. Overcurrent protection region



5.5 Enable function

The enable feature allows to put the device into the standby mode. With the EN pin lower than 0.4 V, the device is disabled and the power consumption is reduced to less than 10 µA. With the EN pin higher than 1.2 V, the device is enabled. If the EN pin is left floating, an internal pull-down ensures that the voltage at the pin reaches the inhibit threshold and the device is disabled. The pin is also V_{IN} compatible.

5.6 Light-load operation

With the peak current mode control loop the output of the error amplifier is proportional to the load current. The AST1S31HF increases light-load efficiency, when the output of the error amplifier falls below a certain threshold, the high-side turn-on is prevented.

This mechanism reduces the switching frequency at the light-load in order to save the switching losses.

5.7 Hysteretic thermal shutdown

The thermal shutdown block generates a signal that turns off the power stage if the junction temperature goes above 150 °C. Once the junction temperature goes back to about 130 °C, the device restarts into the normal operation.

6 Application information

6.1 Input capacitor selection

The capacitor connected to the input must be capable to support the maximum input operating voltage and the maximum RMS input current required by the device. The input capacitor is a subject of a pulsed current, the RMS value of which is dissipated over its ESR, affecting the overall system efficiency.

So the input capacitor must have an RMS current rating higher than the maximum RMS input current and an ESR value compliant with the expected efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 24

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where I_O is the maximum DC output current, D is the duty cycle, and η is the efficiency. Considering $\eta = 1$, this function has a maximum at D = 0.5 and is equal to $I_O/2$.

The peak-to-peak voltage across the input capacitor can be calculated as:

Equation 25

$$V_{PP} = \frac{I_O}{C_{IN} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

where *ESR* is the equivalent series resistance of the capacitor.

Given the physical dimension, ceramic capacitors can well meet the requirements of the input filter sustaining a higher input RMS current than electrolytic / tantalum types. In this case the equation of C_{IN} as a function of the target peak-to-peak voltage ripple (V_{PP}) can be written as follows:

Equation 26

$$C_{IN} = \frac{I_O}{V_{PP} \cdot F_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

neglecting the small ESR of ceramic capacitors.

Considering $\eta = 1$, this function has its maximum in D = 0.5, therefore, given the maximum peak-to-peak input voltage (V_{PP_MAX}), the minimum input capacitor (C_{IN_MIN}) value is:

Equation 27

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot F_{SW}}$$

Typically, C_{IN} is dimensioned to keep the maximum peak-to-peak voltage ripple in the order of 1% of V_{INMAX}.

The placement of the input capacitor is very important to avoid noise injection and voltage spikes on the input voltage pin. So the C_{IN} must be placed as close as possible to the VIN_SW pin. In *Table 7* some multilayer ceramic capacitors suitable for this device are given.

Table 7. Input MLCC capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)
Murata	GCM	47	6.3
TDK	CGA6	47	6.3
TAIYO YUDEN	LMK325	47	10

A ceramic bypass capacitor, as close as possible to the VINA pin so that additional parasitic ESR and ESL are minimized, is suggested in order to prevent instability on the output voltage due to noise. The value of the bypass capacitor can go from 330 nF to 1 µF.

6.2 Inductor selection

The inductance value fixes the current ripple flowing through the output capacitor. So the minimum inductance value to have the expected current ripple must be selected. The rule to fix the current ripple value is to have a ripple at 20% - 40% of the output current.

In the continuous current mode (CCM), the inductance value can be calculated by *Equation 28*:

Equation 28

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

where T_{ON} is the conduction time of the high-side switch and T_{OFF} is the conduction time of the low-side switch [in CCM, $F_{SW} = 1 / (T_{ON} + T_{OFF})$]. The maximum current ripple, given the V_{OUT}, is obtained at maximum T_{OFF}, that is, at a minimum duty cycle (see previous section to calculate minimum duty). So by fixing ΔI_L = 20% to 30% of the maximum output current, the minimum inductance value can be calculated:

Equation 29

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SWMIN}}$$

where F_{SWMIN} is the minimum switching frequency, according to *Table 5 on page 6*. The slope compensation, to prevent the sub-harmonic instability in the peak current control loop, is internally managed and so fixed. This implies a further lower limit for the inductor value. To assure sub-harmonic stability:

Equation 30

$$L > V_{out} / (2 \cdot V_{pp} \cdot f_{sw})$$

where V_{PP} is the peak-to-peak value of the slope compensation ramp. The inductor value selected based on *Equation 29* must satisfy *Equation 30*.

The peak current through the inductor is given by *Equation 31*:

Equation 31

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (which must be lower than the current limit of the device) increases. The higher the inductor value, the higher the average output current that can be delivered, without reaching the current limit.

In *Table 8* some inductor part numbers are listed.

Table 8. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
COILTRONICS	DRA73	0.6 to 2.2	5.5 to 7.9
COILCRAFT	XAL40XX	0.6 to 2.2	5.4 to 8.35

6.3 Output capacitor selection

The current in the output capacitor has a triangular waveform which generates a voltage ripple across it. This ripple is due to the capacitive component (charge or discharge of the output capacitor) and the resistive component (due to the voltage drop across its ESR). So the output capacitor must be selected in order to have a voltage ripple compliant with the application requirements.

The amount of the voltage ripple can be calculated starting from the current ripple obtained by the inductor selection.

Equation 32

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

For a ceramic (MLCC) capacitor, the capacitive component of the ripple dominates the resistive one. While for an electrolytic capacitor the opposite is true.

As the compensation network is internal, the output capacitor should be selected in order to have a proper phase margin and then a stable control loop.

The equations of *Section 5.3 on page 10* help to check loop stability given the application conditions, the value of the inductor and of the output capacitor.

In *Table 9* some capacitor series are listed.

Table 9. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GCM	22 to 470	10	5
TDK	CGA6	22 to 470	16	10

6.4 Thermal dissipation

The thermal design is important to prevent the thermal shutdown of the device if junction temperature goes above 150 °C. The three different sources of losses within the device are:

a) Conduction losses due to the on-resistance of the high-side switch (R_{HS}) and low-side switch (R_{LS}); these are equal to:

Equation 33

$$P_{COND} = R_{HS} \cdot I_{OUT}^2 \cdot D + R_{LS} \cdot I_{OUT}^2 \cdot (1 - D)$$

where *D* is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between V_{OUT} and V_{IN}, but it is actually slightly higher to compensate the losses of the regulator.

b) Switching losses due to the high-side power MOSFET turn-on and turn-off; these can be calculated as:

Equation 34

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot Fsw = V_{IN} \cdot I_{OUT} \cdot T_{SW} \cdot F_{SW}$$

where T_{RISE} and T_{FALL} are the overlap times of the voltage across the high-side power switch (V_{DS}) and the current flowing into it during the turn-on and turn-off phases, as shown in *Figure 9*. T_{SW} is the equivalent switching time. For this device the typical value for the equivalent switching time is 20 ns.

c) Quiescent current losses, calculated as:

Equation 35

$$P_Q = V_{IN} \cdot I_Q$$

where I_Q is the quiescent current (I_Q = 1.2 mA maximum).

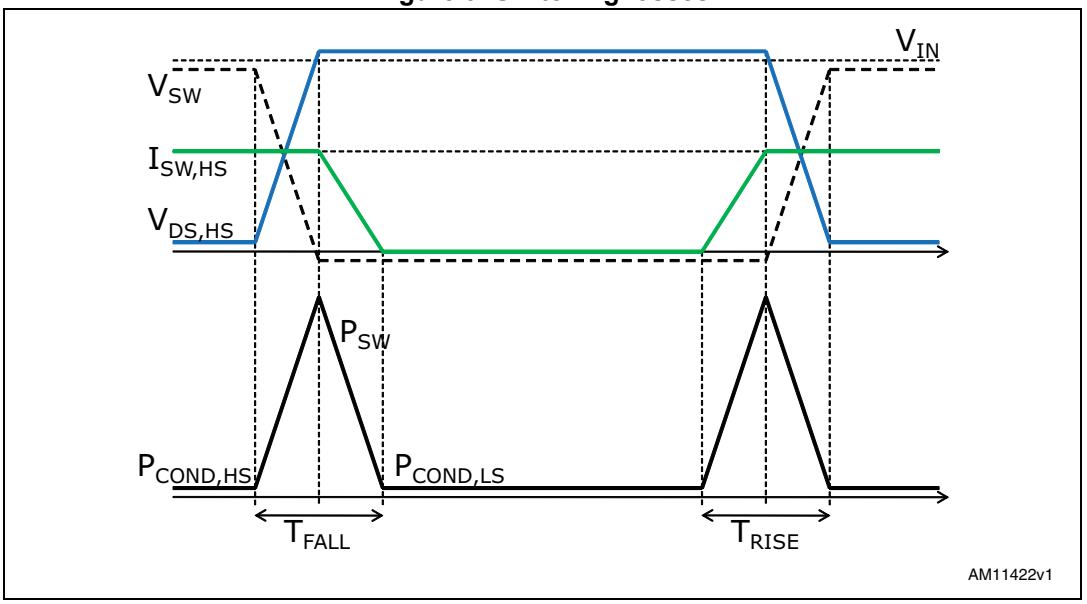
The junction temperature T_J can be calculated as:

Equation 36

$$T_J = T_A + Rth_{JA} \cdot P_{TOT}$$

where T_A is the ambient temperature and P_{TOT} is the sum of the power losses just seen. Rth_{JA} is the equivalent thermal resistance junction to ambient of the device; it can be calculated as the parallel of many paths of heat conduction from the junction to the ambient. For this device the path through the exposed pad is the one conducting the largest amount of heat. The Rth_{JA} measured on the demonstration board (see *Figure 12 on page 25*) is about 50 °C/W.

Figure 9. Switching losses



6.5 Layout consideration

The PC board layout of the switching DC-DC regulator is very important to minimize the noise injected in high impedance nodes, to reduce interference generated by the high switching current loops and to optimize the reliability of the device.

In order to avoid EMC problems, the high switching current loops must be as short as possible. In the buck converter there are two high switching current loops: during the on-time, the pulsed current flows through the input capacitor, the high-side power switch, the inductor and the output capacitor; during the off-time through the low-side power switch, the inductor and the output capacitor.

The input capacitor connected to VINSW must be placed as close as possible to the device, to avoid spikes on VINSW due to the stray inductance and the pulsed input current.

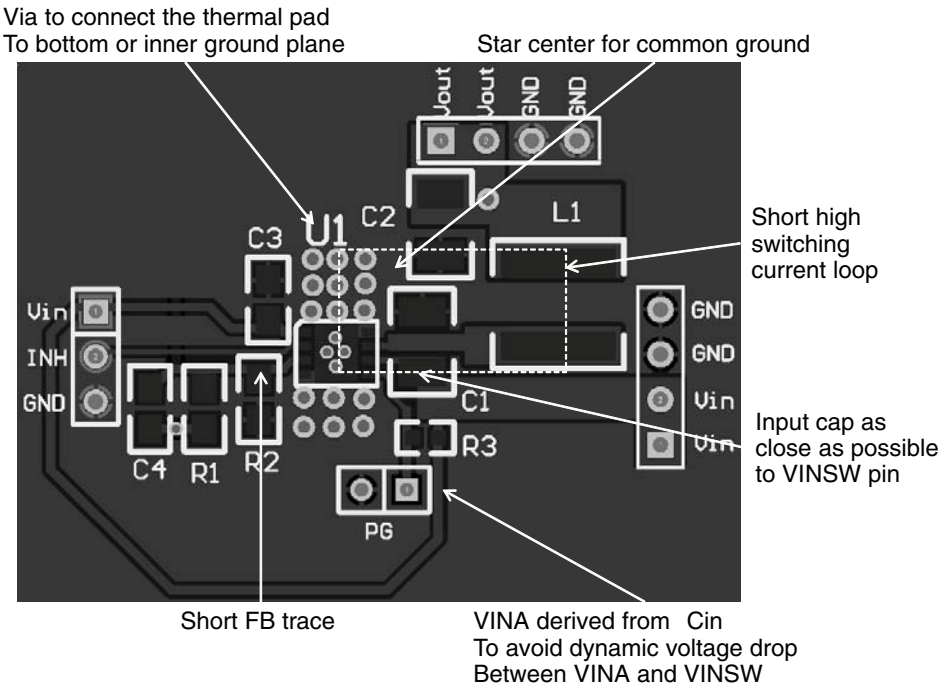
In order to prevent the dynamic unbalance between VINSW and VINA, the trace connecting the VINA pin to the input must be derived from VINSW.

The feedback pin (FB) connection to the external resistor divider is a high impedance node, so the interference can be minimized by routing the feedback node with a very short trace and as far as possible from the high current paths.

A single point connection from signal ground to power ground is suggested.

Thanks to the exposed pad of the device, the ground plane helps to reduce the thermal resistance junction to ambient; so a large ground plane, soldered to the exposed pad, enhances the thermal performance of the converter allowing high power conversion.

Figure 10. PCB layout example



7 Demonstration board

Figure 11. Demonstration board schematic

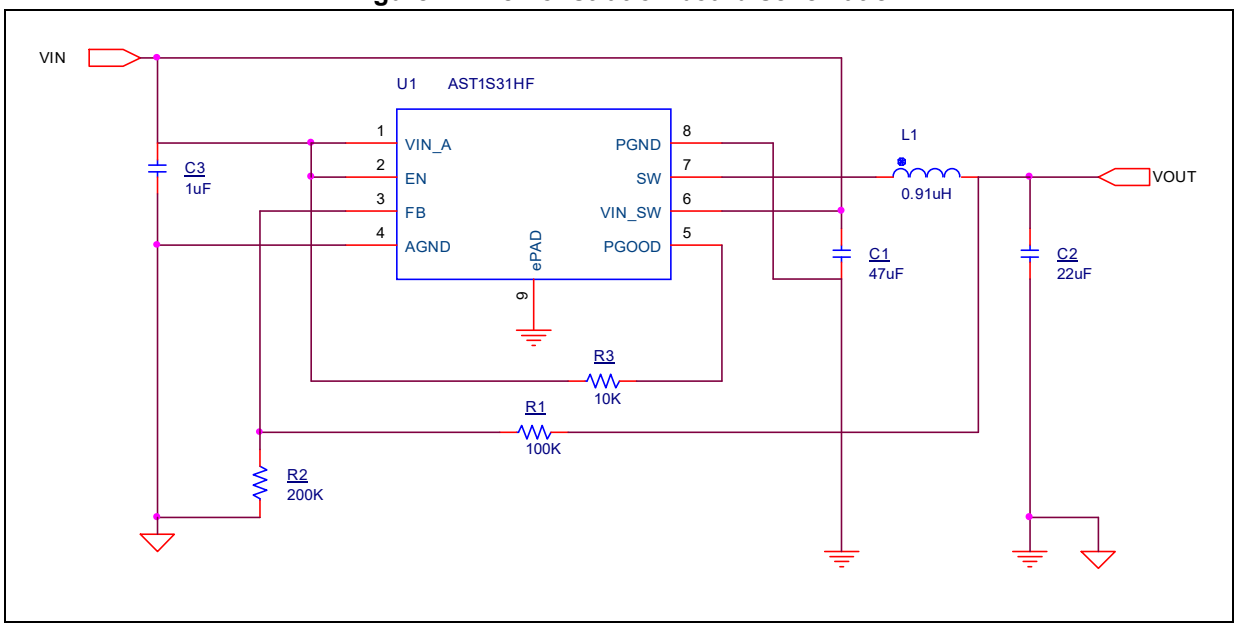
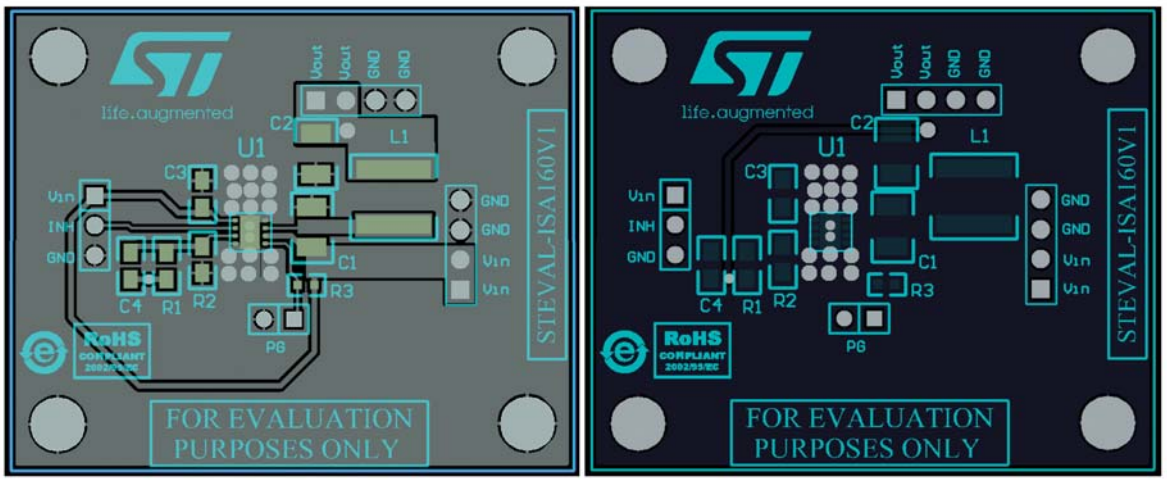


Table 10. Component list

Reference	Part number	Description	Manufacturer
U1	AST1S31HF		STM
L1	DRA73 1R0 R	0.91 µH, Isat = 8.22 A	Coiltronics
C1	GCM32ER70J476ME16	47 µF 6.3 V X7R	MURATA
C2	GCM32ER71A226KE12	22 µF 10 V X7R	MURATA
C3		1 µF 25 V X7R	
C4		NC	
R1		100 kΩ 1%	
R2		200 kΩ 1%	
R3		10 kΩ 1%	

Figure 12. Demonstration board PCB top and bottom, DFN package



8 Typical characteristics

Figure 13. Efficiency curves: V_{IN} = 4.0 V

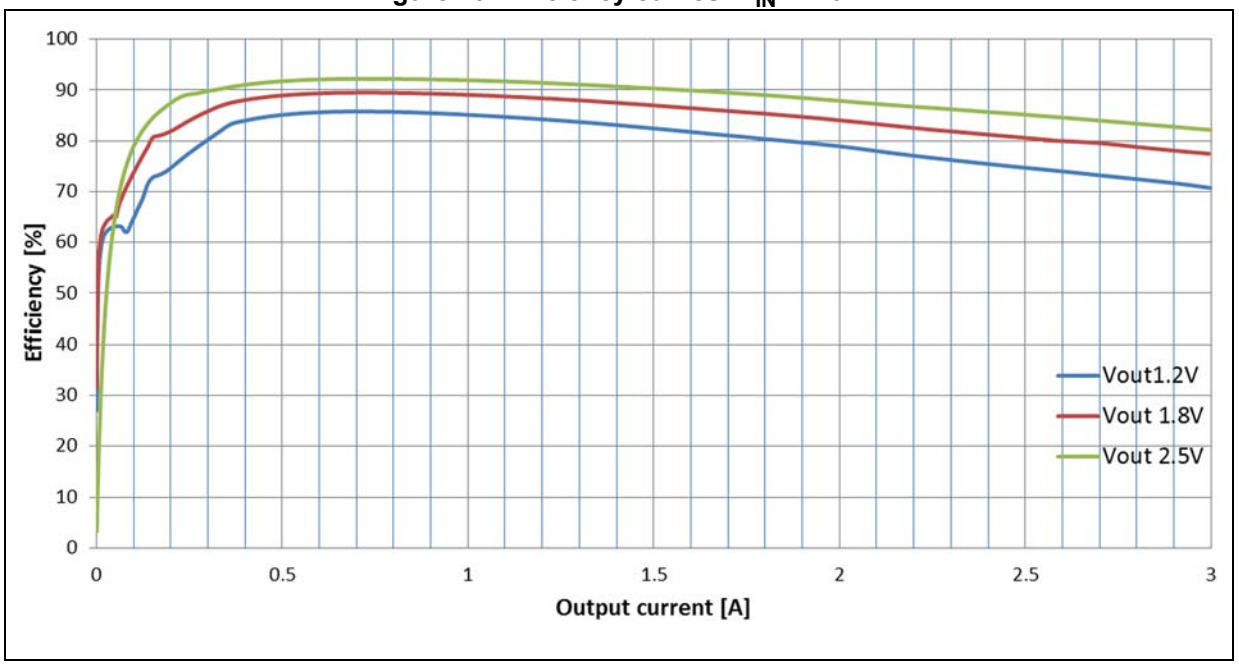


Figure 14. Efficiency curves: V_{IN} = 4.0 V (log scale)

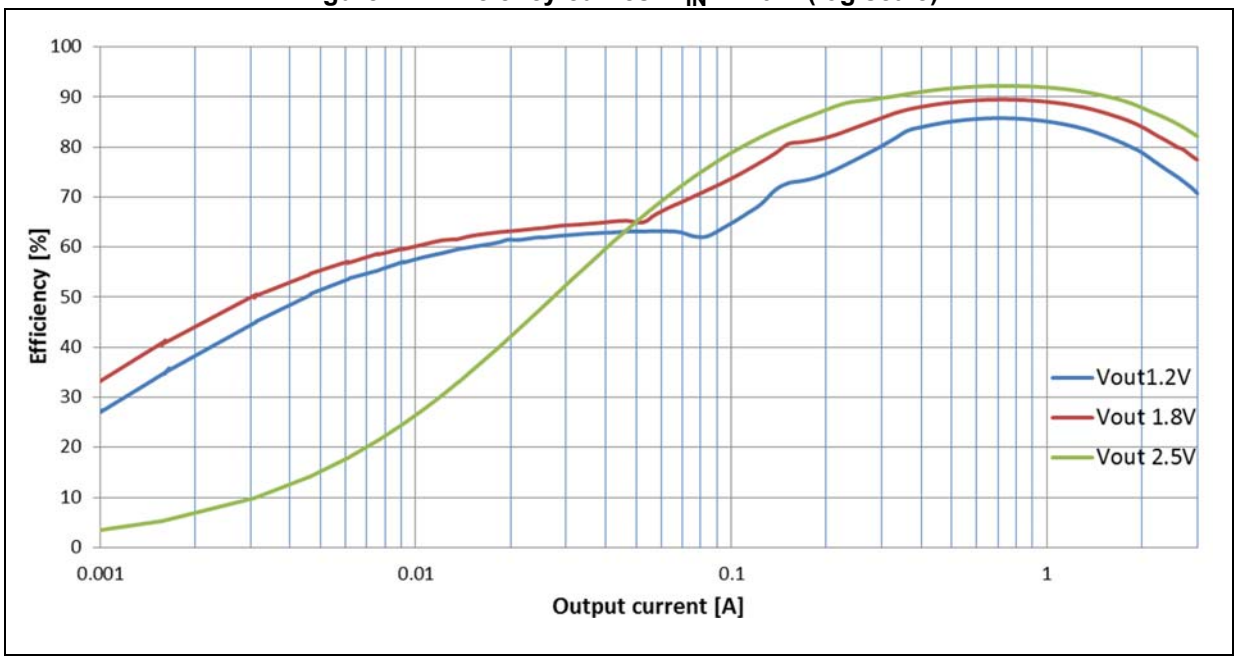


Figure 15. Load regulation (V_{IN} = 4 V)

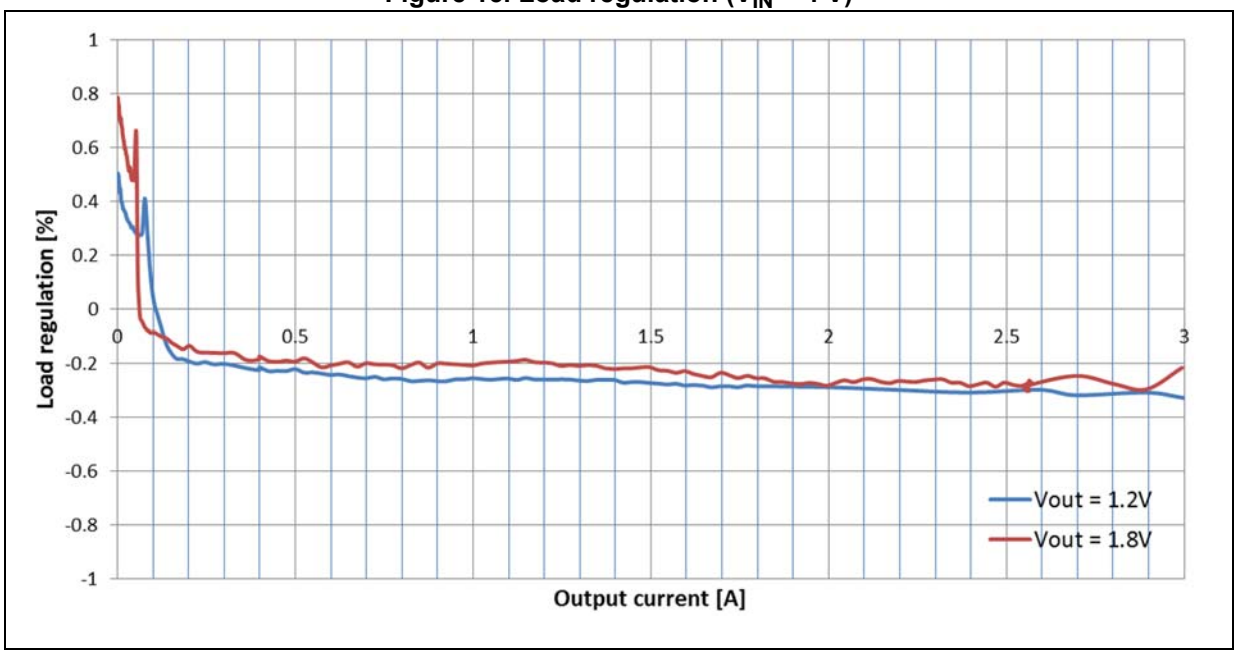


Figure 16. Efficiency curves: V_{IN} = 3.3 V

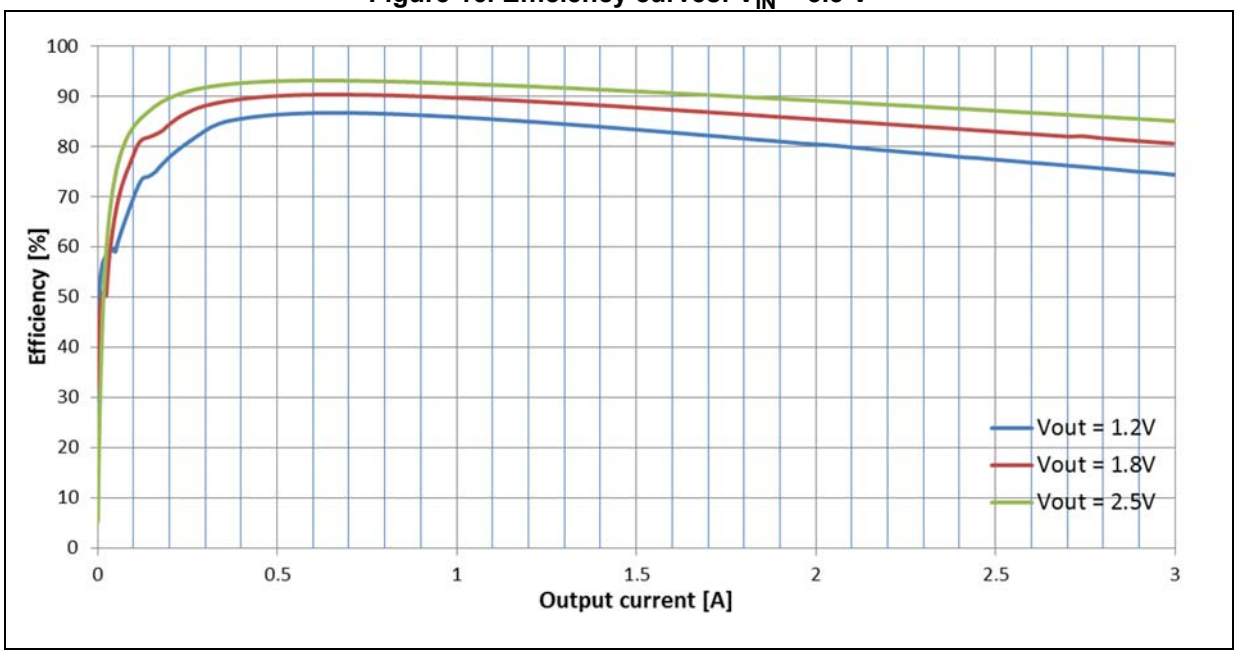


Figure 17. Efficiency curves: V_{IN} = 3.3 V (log scale)

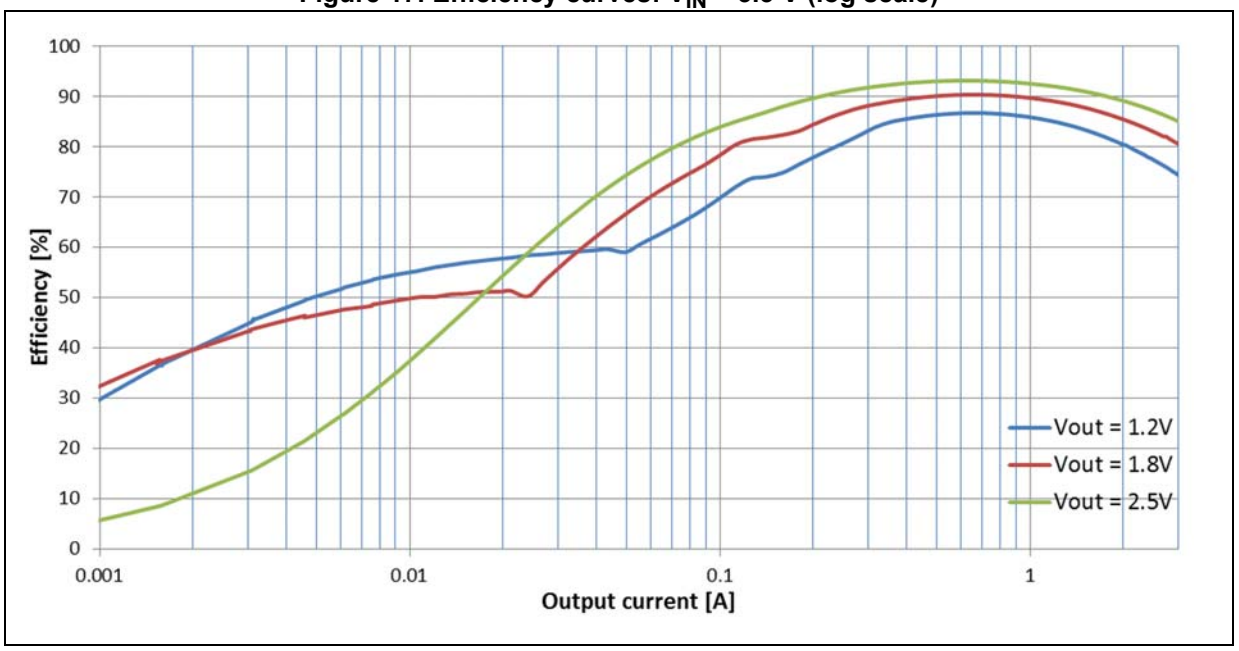
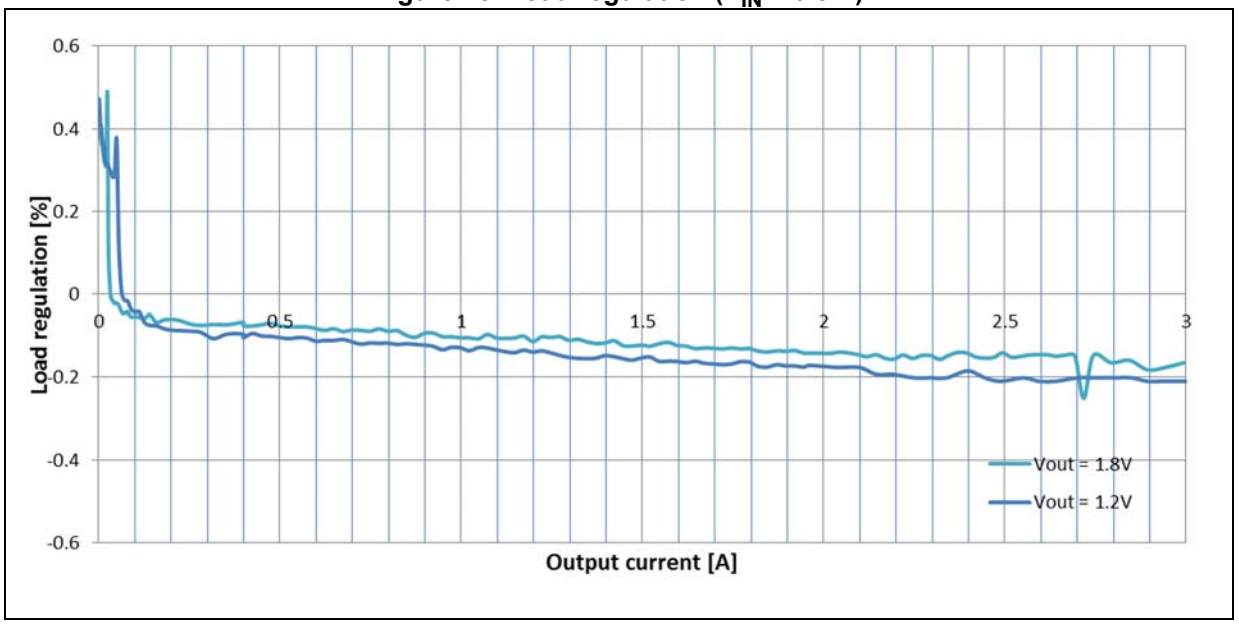


Figure 18. Load regulation (V_{IN} = 3.3 V)



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

9.1 VFDFPN8 (3 x 3 x 1.0 mm) package information

Figure 19. VFDFPN8 (3 x 3 x 1.0 mm) package outline

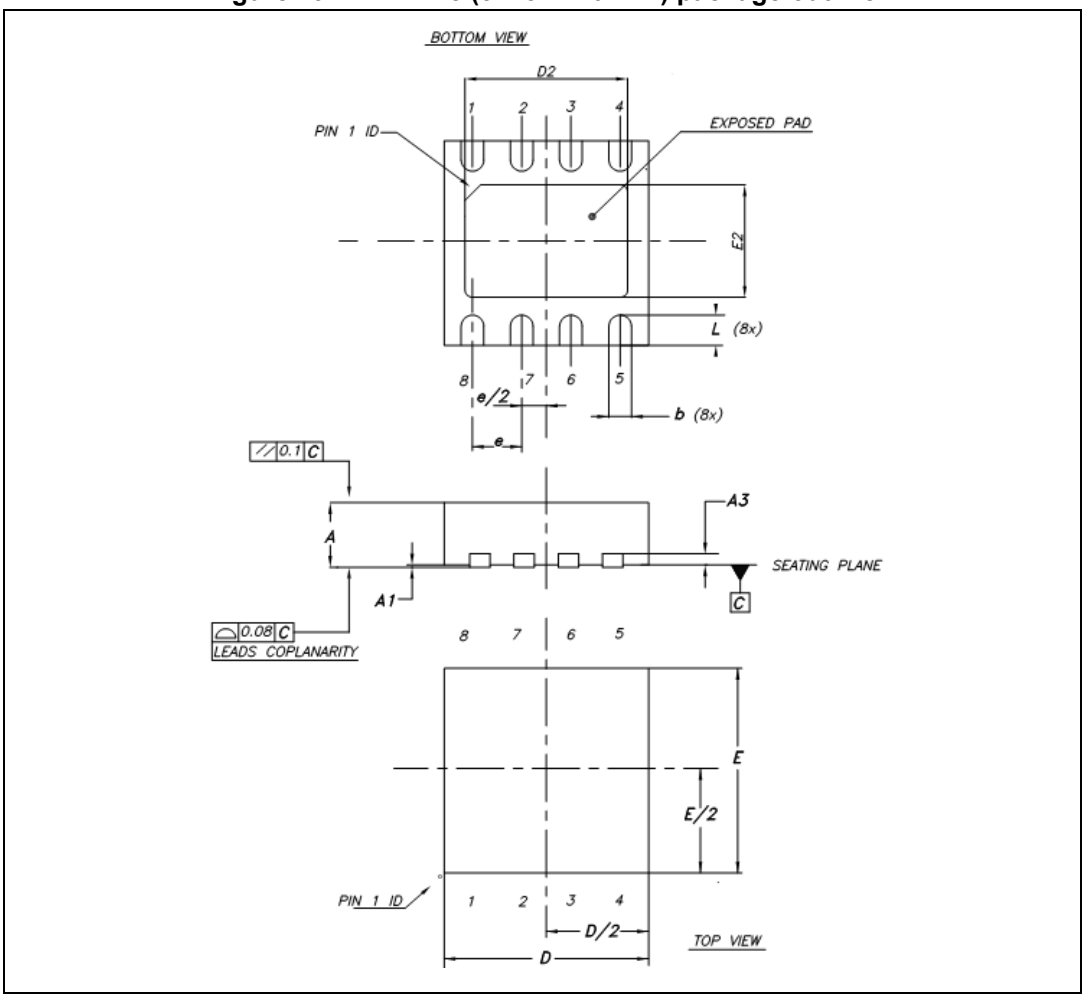


Table 11. VFDFPN8 (3 x 3 x 1.0 mm) package mechanical data

Symbol	Dimensions (mm)			Dimensions (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1	0.0		0.05	0.0		0.0020
b	0.25	0.30	0.35	0.0098	0.0118	0.0138
D		3.00			0.1181	
D2	2.234	2.384	2.484	0.0878	0.0937	0.0976
E		3.00			0.1181	
E2	1.496	1.646	1.746	0.0589	0.0648	0.0687
e		0.65			0.0256	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197

10 Order codes

Table 12. Ordering information

Order code	Package
AST1S31HF	VFDFPN 3 x 3 8L

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Sep-2014	1	Initial release.
03-Mar-2016	2	Updated value in Table 3 on page 6 and Section 7.4 on page 22 (replaced 60 °C/W by 50 °C/W). Updated Section 6.1 on page 10 (added text and Figure 4). Added Section 9 on page 27. Minor modifications throughout document
03-Aug-2018	3	Updated Figure 1: Application circuit on the cover page.
31-Aug-2020	4	Added *Section 2.2: ESD performance*.

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