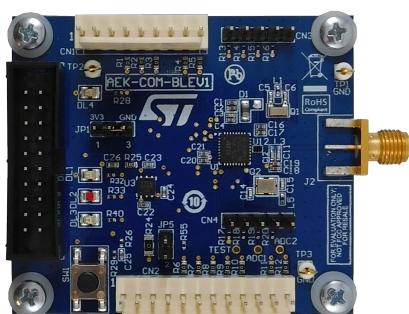


Bluetooth communication board based on BlueNRG-1



Features

- Based on the [BlueNRG-1](#) Bluetooth low energy system on chip
- Associated [STSW-BLUENRG-DK](#) ([BlueNRG-1](#) development kit software package) including firmware and documentation
- Up to +8 dBm available output power (at antenna connector)
- Excellent receiver sensitivity (-88 dBm)
- Very low power consumption: 7.7 mA RX and 8.2 mA TX at +0 dBm
- Bluetooth® low energy compliant: supports master, slave and simultaneous master-and-slave roles
- New integrated balun [BALF-NRG-02D3](#) which integrates a matching network and harmonics filter
- 3 user LEDs
- JTAG debug connector
- Pre-programmed as network processor
- Board size: 60 x 40 mm.
- Part of the [AutoDevKit™](#) initiative
- RoHS and WEEE compliant

Description

The [AEK-COM-BLEV1](#) evaluation board is based on the [BlueNRG-1](#) low power Bluetooth® smart system on chip, compliant with the Bluetooth® specification.

The evaluation board can be connected to a microcontroller via a 12-pin or alternative 9-pin male connector for SPI, serial interface or I²C communication.

The [BlueNRG-1](#) device is supplied with the network processor software loaded and ready to process Bluetooth commands. The software image (DTM_UART.hex) is available in the BlueNRG design kit.

The [STSW-AEKBLE](#) firmware provides a straightforward demonstration of the [AEK-COM-BLEV1](#) board functionality used in conjunction with the [AEK-MCU-C4MLIT1](#) evaluation board with microcontroller.

Product summary	
Bluetooth communication board based on the BlueNRG-1	AEK-COM-BLEV1
Firmware for AEK-COM-BLEV1 testing	STSW-AEKBLE
Bluetooth® low energy system-on-chip	BlueNRG-1
Setup for BlueNRG kits	STSW-BLUENRG-DK
50 Ω, conjugate match balun to BlueNRG transceiver, with integrated harmonic filter	BALF-NRG-02D3
Applications	Factory Automation Bluetooth Low Energy Mobility Services

1 Loading firmware onto the BlueNRG-1 chip

Follow the procedure below to restore the factor firmware on the [BlueNRG-1](#) device.

1.1 Hardware and software requirements

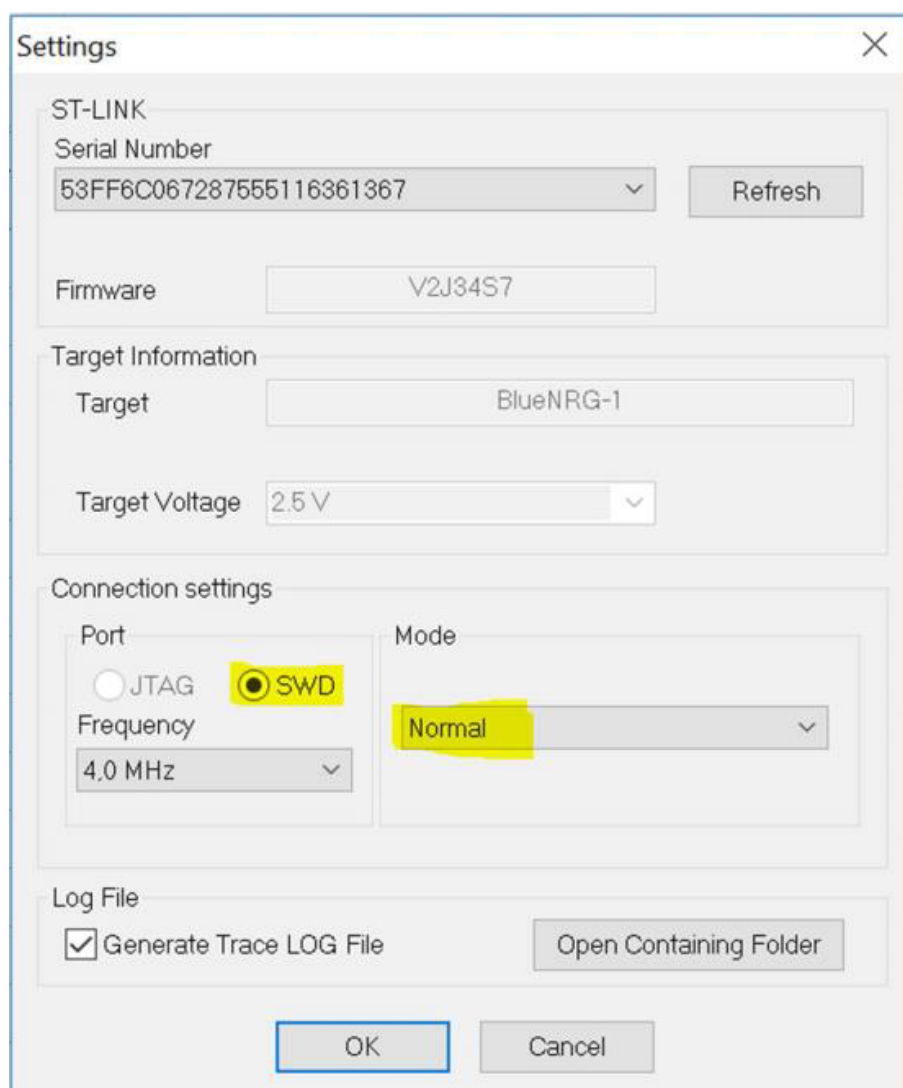
- [ST-LINK/V2](#) programmer/debugger, which is connected through the evaluation board JTAG port
- [STSW-LINK007](#) - ST-LINK/V2 firmware upgrade
- [STSW-LINK009](#) - ST-LINK/V2 Windows driver
- [STSW-BNRG1STLINK](#) - ST-LINK utility required to burn the code in the [BlueNRG-1](#)
- [STSW-BLUENRG-DK](#) - design kit containing the Flash image for the [BlueNRG-1](#). After installing the design kit, go to the installation directory ([\[Firmware \]>\[BLE_Examples\]>\[DTM\]>\[BlueNRG-1\]](#)) to find the "DTM_UART.hex" file

1.2 Firmware burning procedure

- Step 1.** Connect the [ST-LINK/V2](#) to the PC via USB and to the [AEK-COM-BLEV1](#) evaluation board JTAG port
- Step 2.** Run the BlueNRG-1 ST-LINK Utility

- Step 3.** From the top menu, select **[Target]>[Settings]** and ensure the following parameters are set:
- Frequency: 4.0 MHz
 - Mode: Normal
 - Port: SWD

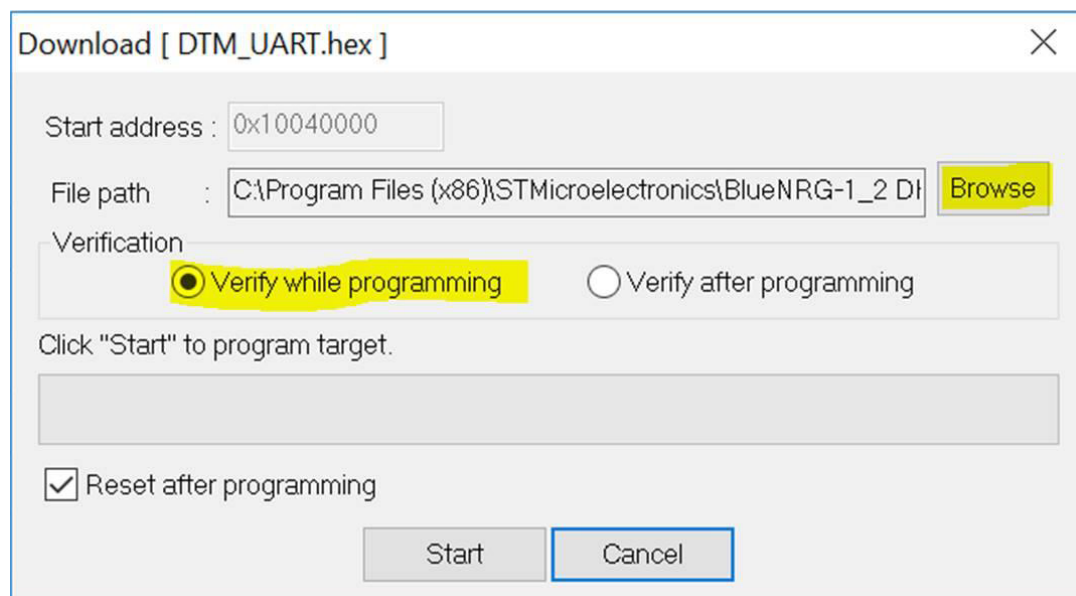
Figure 1. BlueNRG-1 ST-LINK Utility settings



- Step 4.** Press **[OK]** to confirm
- Step 5.** From the main menu, select **[Target]>[Connect]** to connect the programmer
The **ST-LINK/V2** LED starts blinking
- Step 6.** From main menu, select **[Target]>[Program Verify]**

Step 7. Press **[Browse]** and select DTM_UART.hex from the disk to download it

Figure 2. DTM_UART.hex file downloading



Download [DTM_UART.hex]

Start address : 0x10040000

File path : C:\Program Files (x86)\STMicroelectronics\BlueNRG-1_2 DI **Browse**

Verification

☒ Verify while programming ☐ Verify after programming

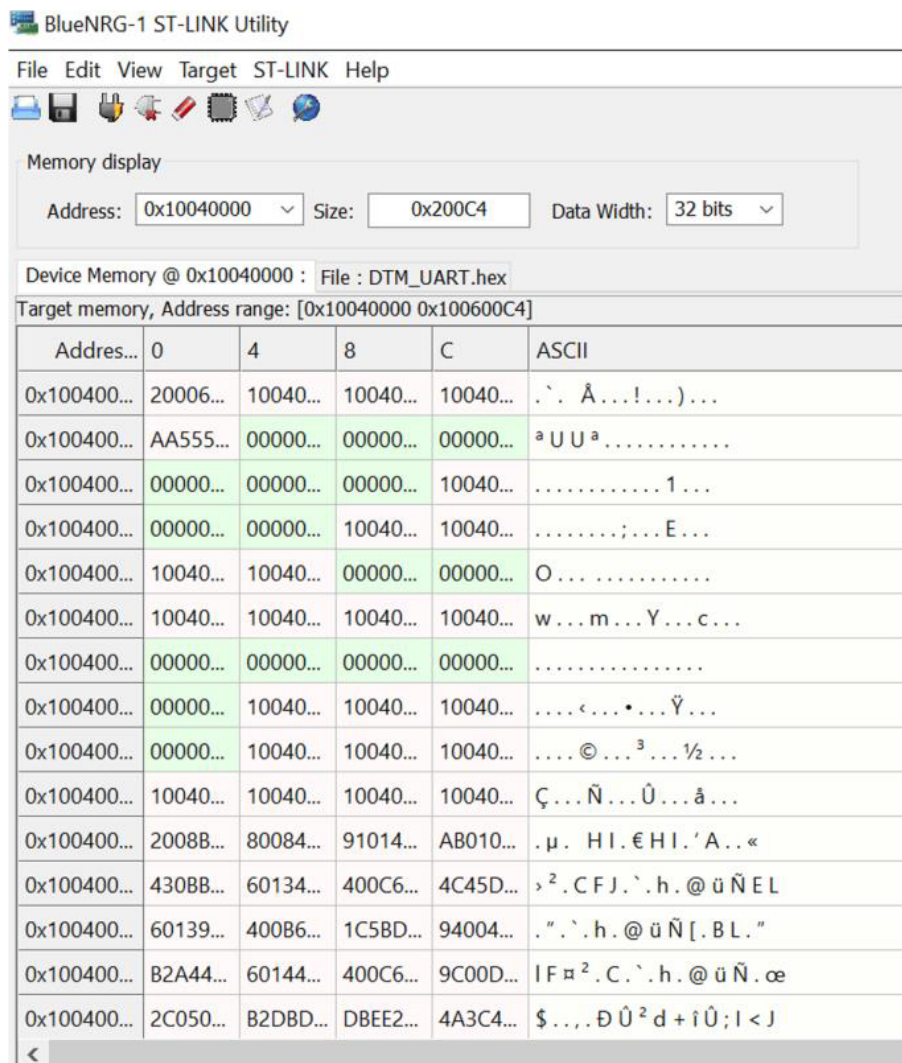
Click "Start" to program target.

☒ Reset after programming

Start Cancel

Step 8. Press **[Start]** to Flash the image onto the **BlueNRG-1** memory

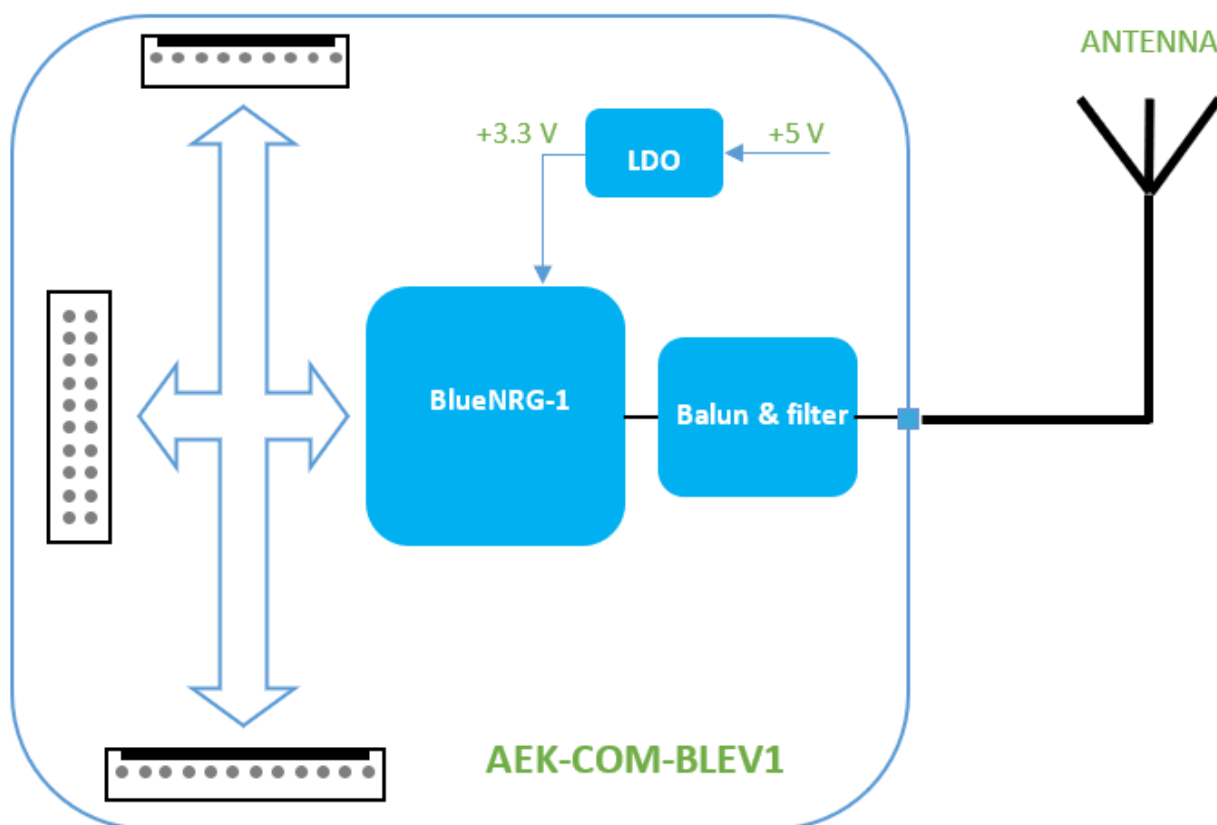
Figure 3. BlueNRG-1 ST LINK Utility device memory



Step 9. From the main menu, select **[>[Target]>[Disconnect]** to disconnect the programmer

2 Block diagram

Figure 4. AEK-COM-BLEV1 block diagram



3

Schematic diagrams

Figure 5. AEK-COM-BLEV1 schematic diagram (1 of 4)

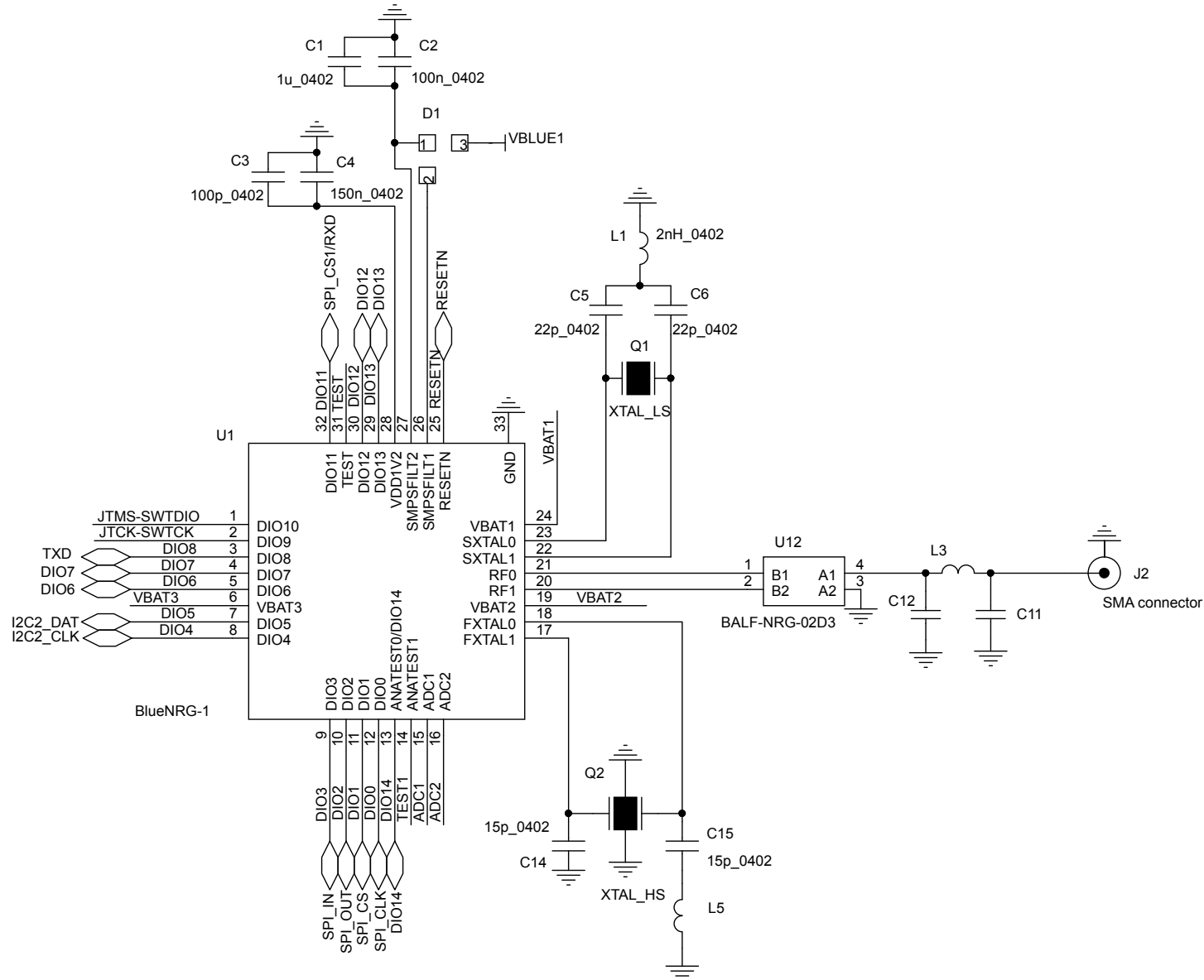


Figure 6. AEK-COM-BLEV1 schematic diagram (2 of 4)

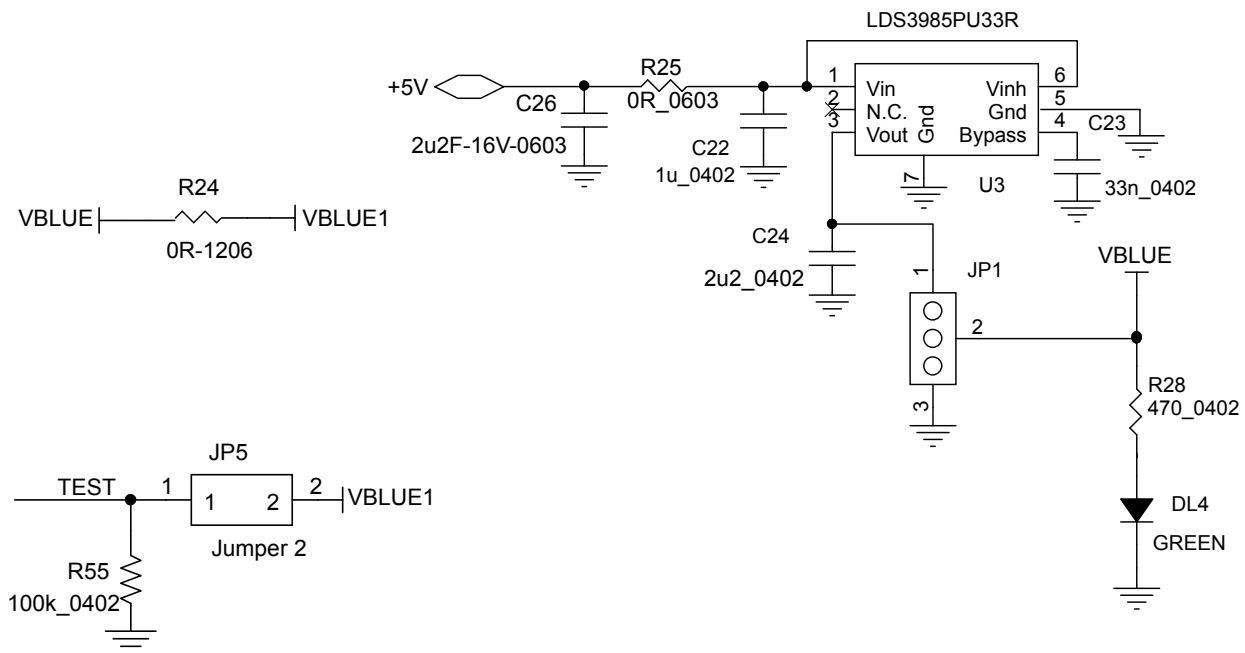
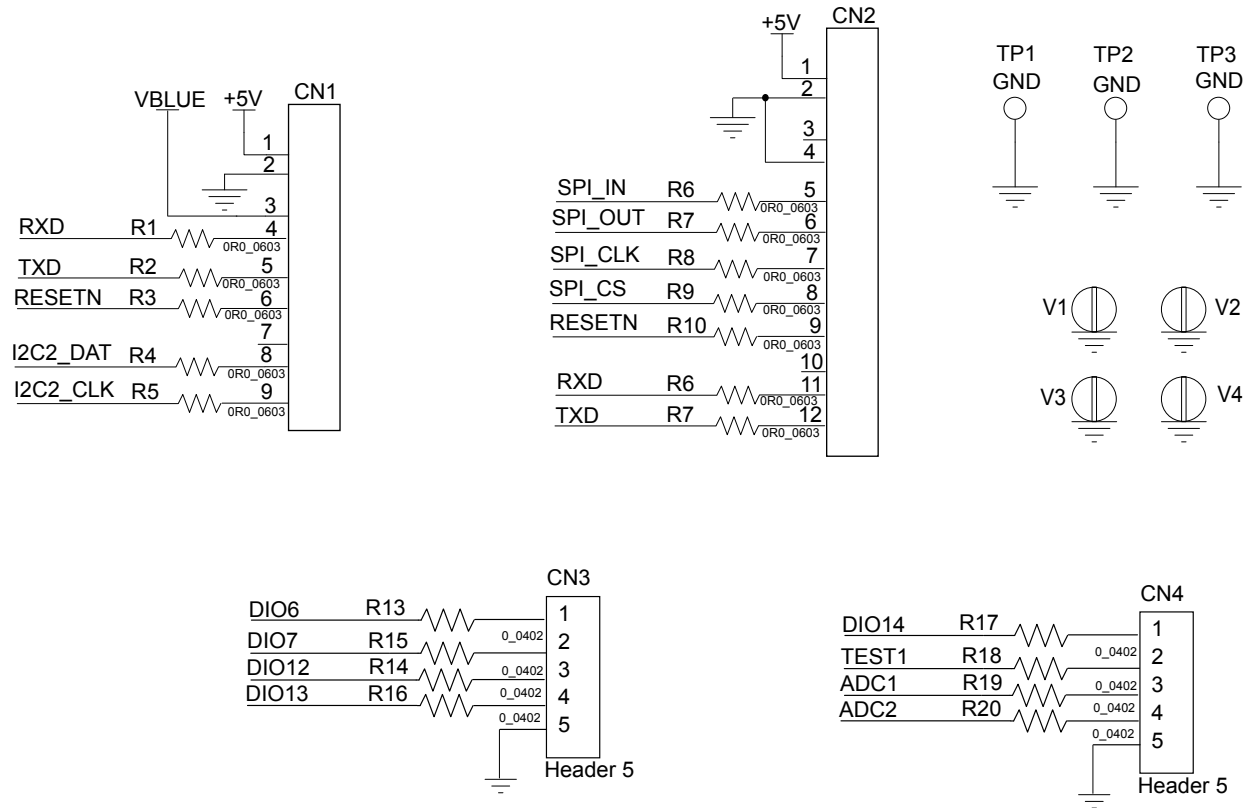


Figure 7. AEK-COM-BLEV1 schematic diagram (3 of 4)



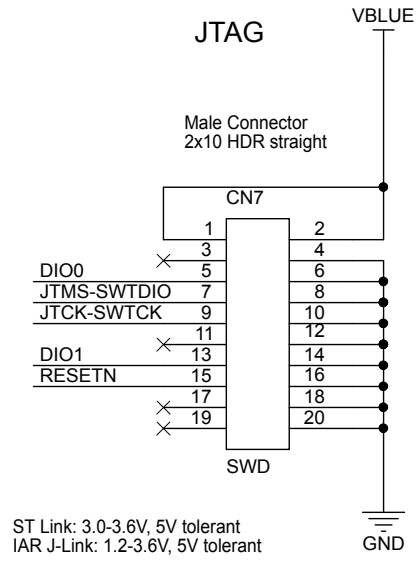
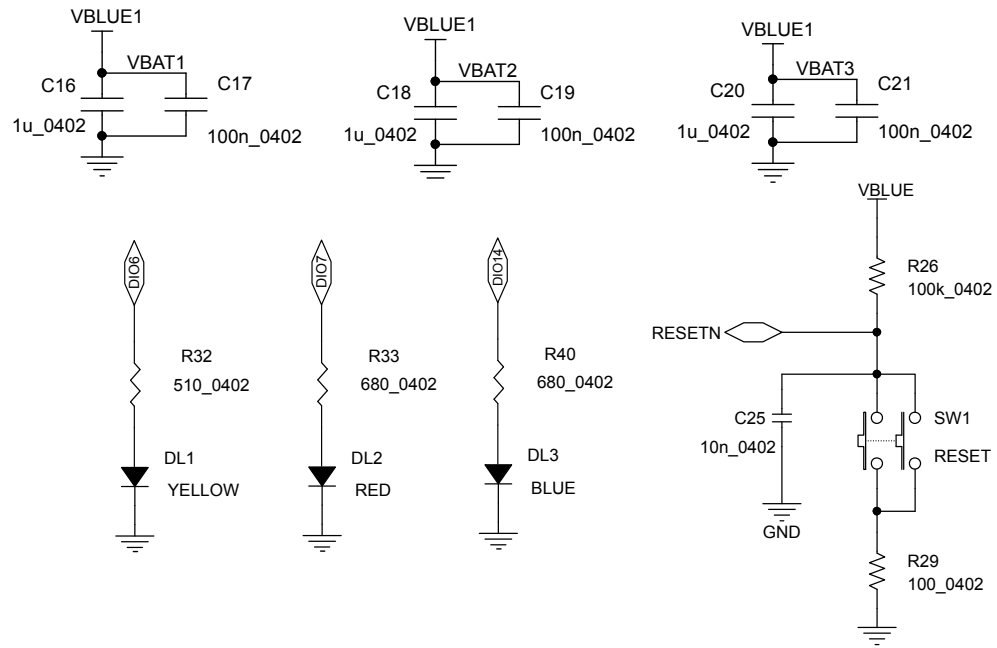


Figure 8. AEK-COM-BLEV1 schematic diagram (4 of 4)



Revision history

Table 1. Document revision history

Date	Version	Changes
19-Feb-2020	1	Initial release.

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