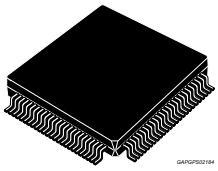
L9390

Twelve channel valve driver

Datasheet - production data



TQFP100
(Exposed pad down)

Features

- Four low side switched output drivers with 0.1 Ω $R_{ds,ON}$ at 25°C
- Possibly configurable as PWM controlled adding external freewheeling diodes
- Two low side PWM controlled output drivers with 0.1 Ω $R_{ds,ON}$ at 25 °C and integrated active freewheeling diodes
- Six low side current controlled output drivers with 0.16 Ω $R_{ds,ON}$ at 25 °C and integrated active freewheeling diodes
- Current accuracy:
  - 10% (I_{load} < 800 mA)
  - 6% (I_{load} > 80 0mA)
- All outputs with integrated 35 V zener clamp
- Five pin SPI port (four standard pins plus additional SPI enable input pin)
- Six serial high speed inputs for output control
- High level diagnostic, including silent valve driver test
- Direct disable of outputs with an external pin
- Programmable jitter frequency of PWM and current controlled outputs
- TQFP100 exposed pad package

Description

The L9390 is a twelve output low side valve driver designed for use in an ABS/ESP vehicle system. All outputs are PWM configurable, while six out of twelve are current regulated. Each of the twelve outputs is open drain configured and has a built-in 35 V clamp. Eight of the twelve have integrated active freewheeling diodes for active rectification of the PWM controlled load.

In order to minimize electromagnetic emissions during load actuation, the possibility to control output slopes is provided.

Two separate communication interfaces are present: the SPI port is primarily designated to provide diagnostics and secondary control. The serial High End Timer interface (HET) provides the primary output control functions from on/off switching to current level control commands.

Diagnostic includes over current protection, under current detection, open load detection, loss of ground detection, loss of freewheeling diode, and over temperature detection, output integrity check, SVDT, leakage current test, PWM integrity and functionality check, valve resistance sense check, loss of freewheeling diode detection and more.

Power supply monitoring is also included.

Table 1. Device summary

Part number	Package	Packing
L9390	TQFP100 14x14x1.0mm (exposed pad down)	Tray

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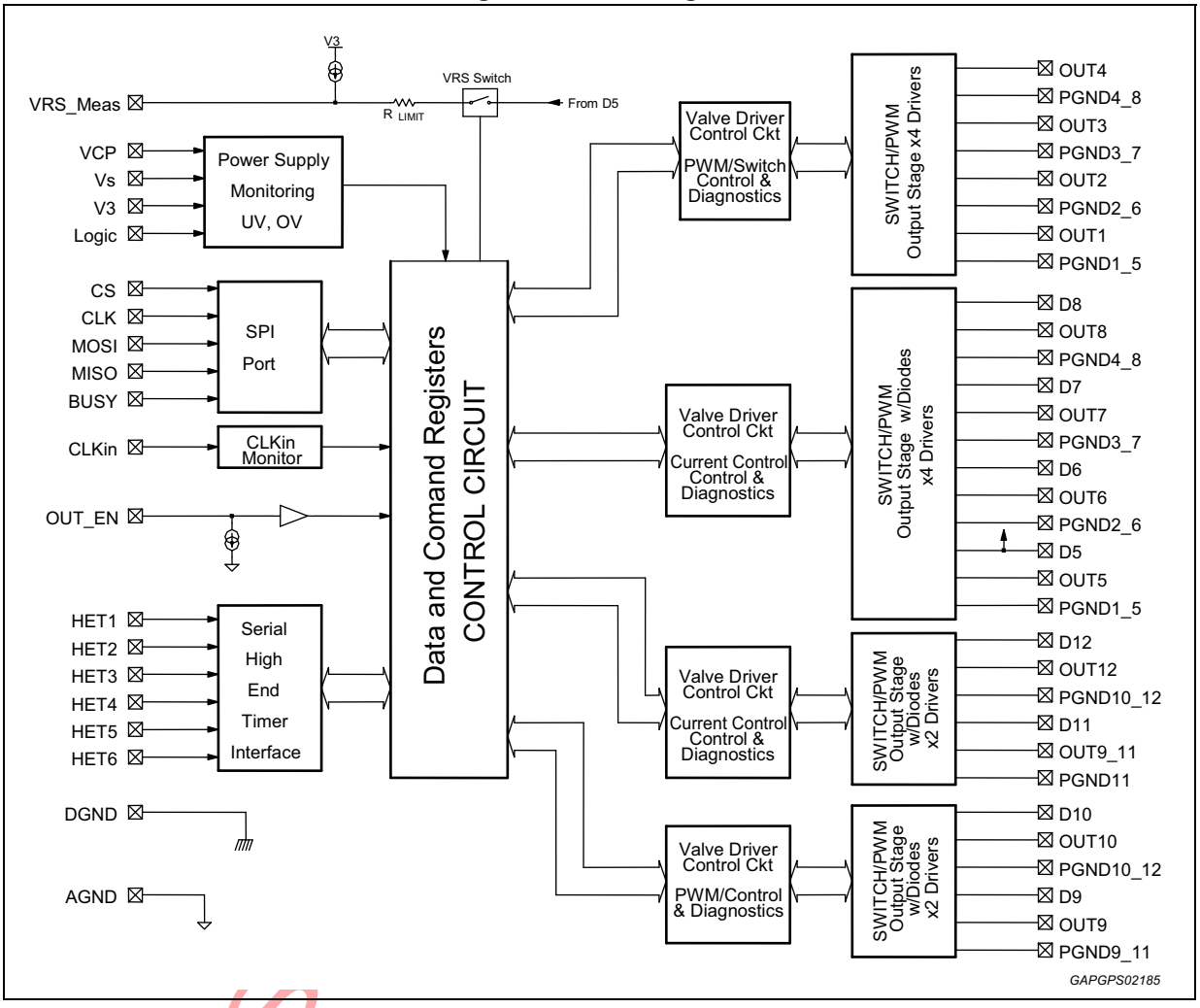
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection diagram (top view)

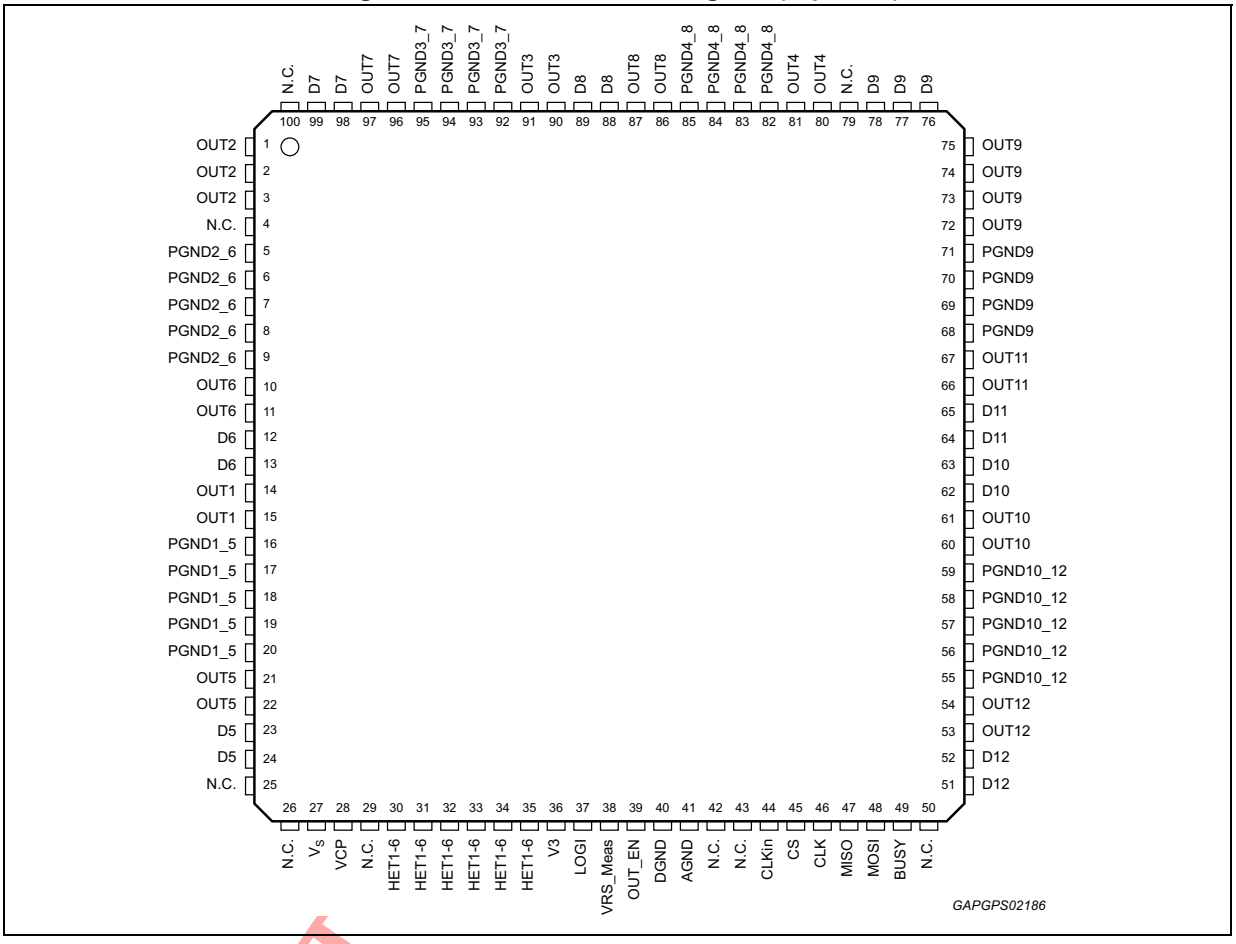


Table 2. Pins description

Pin #	Name	Description
1-3	OUT2	Valve low side driver output, switched or PWMmed
4	N.C.	Not connected
5-9	PGND2_6	Dedicated output power ground
10-11	OUT6	Valve low side driver output, PWMmed or current regulated
12-13	D6	Freewheeling diode cathode
14-15	OUT1	Valve low side driver output, switched or PWMmed
16-20	PGND1_5	Dedicated output power ground
21-22	OUT5	Valve low side driver output, PWMmed or current regulated
23-24	D5	Freewheeling diode cathode
25-26	N.C.	Not connected
27	Vs	Battery level supply input voltage
28	VCP	Charge pump voltage input

Table 2. Pins description (continued)

Pin #	Name	Description
29	N.C.	Not connected
30-35	HET1-6	Serial high end timer inputs
36	V3	3.3V supply input
37	LOGI	Logic supply input, must be tied to V3
38	VRS_Meas	Switch connection to pin D5 for the purpose of diagnosing specific load resistances.
39	OUT_EN	Enables/ disables all outputs asynchronous to any other commands
40	DGND	Circuit ground
41	AGND	Signal ground
42-43	N.C.	Not connected
44	CLKin	Clock input for IC
45	CS	SPI chip select input
46	CLK	SPI clock input
47	MISO	SPI master in slave out
48	MOSI	SPI master out slave in
49	BUSY	SPI enable input
50	N.C.	Not connected
51-52	D12	Freewheeling diode cathode
53-54	OUT12	Valve low side driver output, current regulated
55-59	PGND10_12	Dedicated output power ground
60-61	OUT10	Valve low side driver output, current regulated
62-63	D10	Freewheeling diode cathode
64-65	D11	Freewheeling diode cathode
66-67	OUT11	Valve Low Side Driver output, PWMmed
68-71	PGND9	Dedicated output power ground
72-75	OUT9	Valve low side driver output, PWMmed
76-78	D9	Freewheeling diode cathode
79	N.C.	Not connected
80-81	OUT4	Valve low side driver output, switched or PWMmed
82-85	PGND4_8	Dedicated output power ground
86-87	OUT8	Valve low side driver output, PWMmed or current regulated
88-89	D8	Freewheeling diode cathode
90-91	OUT3	Valve low side driver output, switched or PWMmed
92-95	PGND3_7	Dedicated output power ground
96-97	OUT7	Valve low side driver output, PWMmed or current regulated
98-99	D7	Freewheeling diode cathode
100	N.C.	Not connected

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Pin/parameter name	Parameter	Min.	Max.	Unit
V_S	Supply voltage (continuous)	-0.3	+20	V
	Supply voltage (t < 5 min)	-	+27	V
V_S, VCP	Supply voltage τ < 400 ms		+35	V
V3, VLOGIC	Maximum voltage		+3.6	V
CS, CLK, MOSI, MISO, EN, CLKin, HETx		-0.3	+3.6	V
OUT_EN		-0.3	+3.6	V
VRS_Meas		-0.3	+3.6	V
OUTx, Dx		-0.3	+35	V
T_j	Junction temperature	-40	(1)	°C
	Junction temperature (1h over life-time)		+190(2)	°C
T_{stg}	Storage temperature	-65	+150	°C

1. Internally limited
2. Allowed only during switch-off

Warning: The absolute maximum ratings are the values at which if exceeded the device may become damaged.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min.	Max.	Unit
T_j	Junction temperature	-40	+150	°C
T_{amb}	Ambient temperature	-40	+105	°C
$R_{th(j\text{-}amb)}$	Thermal resistance junction to ambient(1)		20	°C/W
$R_{th(j\text{-}case)}$	Thermal resistance junction to case		2	°C/W
$E_{OUT(MAX)}$	Maximum OUTx clamping energy, single pulse		50	mJ

1. On a multilayer FR4 board with thermal vias and 2 Ounce copper covering >10mm^2

3.3 Electrical characteristics

(-40 °C < T_J < 150 °C, 7 V < V_S < 19 V unless otherwise specified.)

Table 5. V_S supply voltage

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{SOPER}	Operating supply voltage	-	7.0	-	19	V
$I_{Q(Vs)}$	Supply current on-state	$V_{S(LVI)} < V_S < V_{S(OVS)}$	-	-	5	mA
$V_{S(LVI)}$	Supply voltage inhibit threshold (1)	Falling edge	3.0	3.4	3.8	V
$V_{S(LVI)}$	Supply voltage inhibit threshold	Rising edge	6.6	-	7.0	V
$V_{S(LVI)HYST}$	Inhibit threshold hysteresis	-	-	0.2	-	-

1. See the functional description for a detailed description of this function.

Table 6. V3 3.3V supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V3_{OPER}$	Operating voltage	-	3.0	-	3.6	V
$I_{Q(V3)}$	Supply current in on-state	3.0 V < V3 < 3.6 V	-	-	40	mA
$V3_{LVI}$	Supply low voltage inhibit	L9390 enters RESET mode after $t_{LVI(V3)}$, set 3V_Fail bit	2.5	2.75	2.95	V
$t_{LVI(V3)}$	Low voltage inhibit filter time	After delay device enters RESET mode, set V3_Fail bit	4	-	20	µs

Table 7. VCP operating

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VCP_{OPER}	Operating voltage	-	V_S+6	-	35	V
VCP_{CLAMP}	Clamping voltage	Built in zener protection	35	-	-	V
$I_{Q(VCP)}$	Supply current in on-state	V_S+6 < VCP < 35 V	-	-	300	µA
VCP_{LVI}	Supply low voltage inhibit	-	V_S+3	-	V_S+6	V

Table 8. Band gap

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ΔV_{BG}	Band gap voltage monitor	Voltage measured outside of this value will cause a RESET and setting of the V3_Fail bit	-7	-	+7	%
$t_{VBG(error)}$	Band gap fault filter time	After delay device enters RESET mode	100	-	200	µs

Table 9. Output driver

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DS(on)OUT1-4}$	Static drain to source on resistance outputs 1-4	I_{OUT} = 1 A T_J = 25 °C T_J = 175 °C	-	0.076	 0.2	Ω
$R_{DS(on)OUT5-8}$	Static drain to source on resistance outputs 5-8	I_{OUT} = 1 A T_J = 25 °C T_J = 175 °C	-	0.12	 0.32	Ω
$R_{DS(on)OUT9-10}$	Static drain to source on resistance, outputs 9-11	I_{OUT} = 1 A T_J = 25 °C T_J = 175 °C	-	0.064	 0.18	Ω
$R_{DS(on)OUT11-12}$	Static drain to source on resistance, outputs 11-12	I_{OUT} = 1 A T_J = 25 °C T_J = 175 °C	-	0.12	 0.32	Ω
Tj_{OTS}	Over temperature shutdown(1)	OUTx disabled after t_{OT}	190	205	220	°C
Tj_{OTSH}	Over temperature shutdown hysteresis	-	-	20	-	°C
V_{CLAMP}	Output clamping voltage	I_{OUT} = 100 mA	35	-	-	V
$I_{OUT(PD)}$	Output pull-down current	OUTx = off, EN_set = 1	9	10	11	µA
$I_{OUT(LEAK)}$	Output leakage current	V_{OUT} < 30 V, EN_set = 0 if T < 140 °C if 140 °C < T < 175 °C	-	-	4 19	µA
E_{CLAMP}	Output clamping energy		-	-	30	mJ

1. See the functional description for a detailed description of this function.

Table 10. Active freewheeling diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{DS(on)Diode1}$	Static drain to source on resistance diodes D5-D8, D11, D12	I_{OUT} = 1.5 A, Vs = 13 V T_J = 25 °C T_J = 175 °C	-	0.220	 0.475	Ω
$R_{DS(on)Diode2}$	Static drain to source on resistance diodes D9, D10	I_{OUT} = 1.5 A, Vs = 13 V T_J = 25 °C T_J = 175 °C	-	0.20	 0.40	Ω
R_{SENSE}	Sense resistor for current regulated outputs(OUT5-OUT8, OUT11, OUT12)	Calculated: (VD @ 1.5A - VD @ 0.25A) / 1.55A VD = Voltage across Diode when conducting (V_{OUTx} - V_{Dx})	-	0.25	0.40	Ω
$t_{D(on)}$	Additional on-time of freewheeling diode (transistor)	After deactivation of output	-	20	-	ms

Table 10. Active freewheeling diode (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DON}	Freewheeling diode (transistor) switch-on threshold	Above this voltage the transistor is turned on (V_{OUTx}-V_{Dx})	-150	0	+150	mV
V_{DOFF}	Freewheeling diode (transistor) switch-off threshold	Below this voltage the transistor is turned off (V_{OUTx}-V_{Dx})	-	0	1	V

Figure 3. Output timing

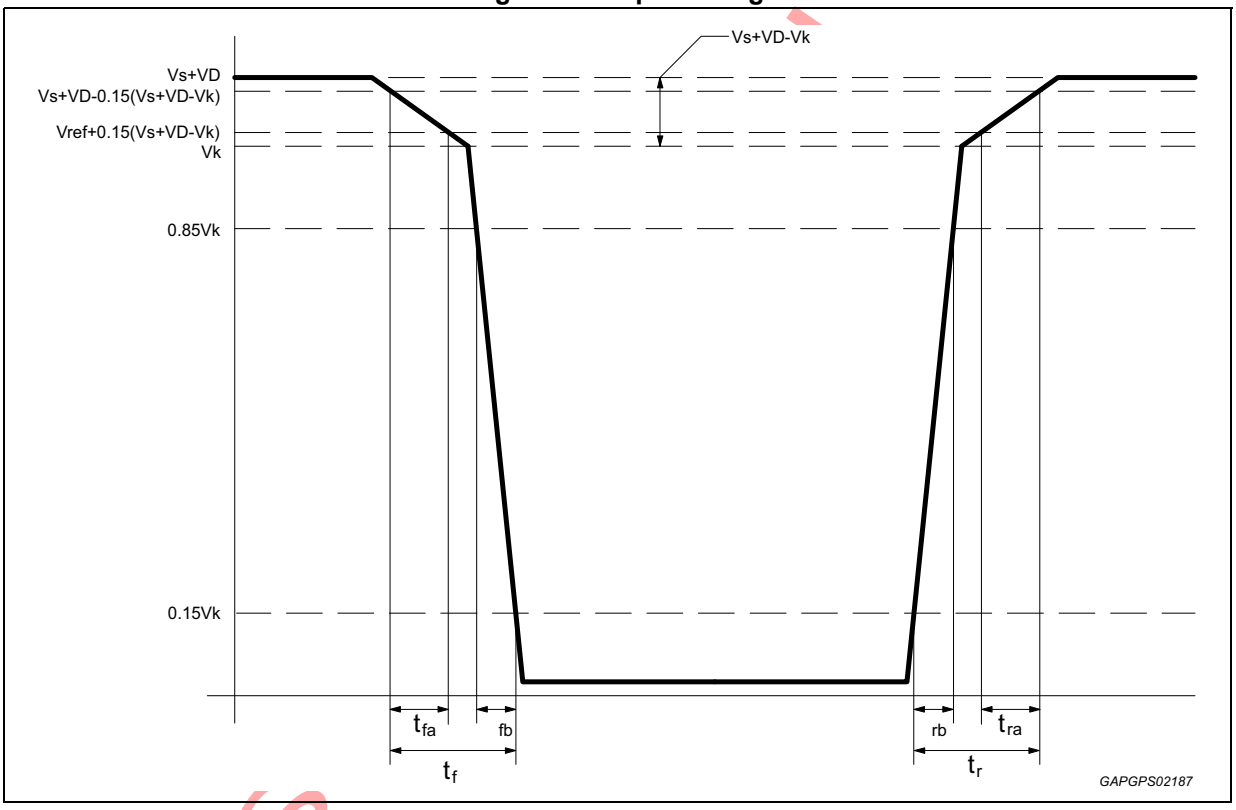


Table 11. PWM output timing characteristics with edge shaping (SHAPE_EN=1)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_K	Slope a to slope b knee voltage	0.5 A < I_{OUT} < 0.5 A, 8 V < V_S < 20 V	V_S-2		V_S-1	V
t_{fa}	Slope a falling slew rate	0.5 A < I_{OUT} < 1.5 A	3.5	5	6.5	V/µs
t_{fb}	Slope b falling slew rate		14	20	26	V/µs
t_{ra}	Slope a rising slew rate		3.5	5	6.5	V/µs
t_{rb}	Slope b rising slew rate		14	20	26	V/µs
t_f	Fall time		0.5	1.5	5	µs
t_r	Rise time		0.5	1.5	5	µs

Table 12. PWM output timing characteristics without edge shaping (SHAPE_EN=0)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_r	Output rise time	0.5 A < I_{OUT} < 1.5 A	7	10	13	V/µs
t_f	Output fall time	0.5 A < I_{OUT} < 1.5 A, 8 V < V_S< 20 V	7	10	13	V/µs

Table 13. PWM output timing characteristics without edge shaping

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_f	Fall time	0.5 A < I_{OUT} < 1.5 A	0.5	1.5	5	µs
t_r	Rise time		0.5	1.5	5	µs

Table 14. Input buffer parameters, CLK, CS, MOSI

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low voltage	-	-0.3	-	1.0	V
V_{IH}	Input high voltage	-	2.0	-	V3+0.3	V
$V_{I(HYST)}$	Input threshold hysteresis	-	0.2	0.5	1.0	V
I_{P-U}	Internal pull-up current source	-0.3<V_{IN}<2.0V	-35	-	-65	µA
f_{IN}	Input signal frequency range	-	DC	-	11	MHz

Table 15. Input buffer parameters, MISO, EN

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	I_{OUT} < 25 µA, CL < 60pF	0	-	0.4	V
V_{OH}	Output high voltage		V3-0.4	-	V3	V
$R_{(ON)}$	Pull-up/down switch resistance	-25 µA < I_{OUT} < 25 µA, CS = low	20	50	100	Ω
$R_{(OFF)}$	Off-state switch resistance	CS = high, outputs tri-stated	50	120	300	kΩ
$I_{EN(P-U)}$	Internal enable (EN) pull-up current	-0.3 V < V_{EN} < 2.0 V	-35	-50	-65	µA
f_{IN}	Signal frequency range	I_{OUT} <25µA, CL<60pF	DC	-	11	MHz
$\Delta V_{OUT}/\Delta t$	Output slew rate	CL<60pF	-	150	-	V/µs

Table 16. SPI timing parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CLK}	CLK frequency	-	DC	-	10	MHz
$t_{CLK(high)}$	CLK high time	-	37	-	-	ns
$t_{CLK(low)}$	CLK low time	-	37	-	-	ns
t_{CS-CLK}	CS to CLK delay	3*V_{CLK}-13ns	17	-	-	ns

Table 16. SPI timing parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{CLK-CS}	CLK to CS delay	~1/2CLK = 50 ns + VCLK - 13 ns	45	-	-	ns
$t_{MOSI(set)}$	MOSI to CLK delay	-	27	-	-	ns
$t_{MOSI(hold)}$	CLK to MOSI delay	-	45	-	-	ns
t_{rise}	CLK, MOSI rise time	C_{LOAD} = 60 pF	-	-	13	ns
t_{fall}	CLK, MOSI fall time		-	-	13	ns
$t_{MISO(delay)}$	CLK to MISO delay	~ $t_{CLK(high)}$ + t_f -6ns, 9ns reserve t_{Fall}, t_{Rise} – symmetry	-	-	35	ns
$t_{MISO(active)}$	CS to MISO active delay	C_{LOAD} = 60 pF	-	-	15	ns
$t_{MISO(tri-state)}$	CS to MISO tristate delay		-	-	15	ns
$t_{MISO(rise)}$	MISO rise time		-	-	13	ns
$t_{MISO(fall)}$	MISO fall time		-	-	13	ns
$t_{CS(high)}$	CS high time	$3V_{CLK}$ -Δtr, f, -6 ns	20	-	-	ns
$t_{CS(low)}$	CS low time	34*t_{CLK}	3.4	-	-	µs
$t_{EN(on)}$	CS to EN delay	Falling edge of CS, C_{LOAD} = 60 pF $C_{LOAD(MIN)}$= 15 pF	-	-	100	ns
$t_{EN(high)}$	EN high time	-	-	-	2	µs
$t_{EN(off)}$	CS to EN delay	Rising edge of CS, $3V_{CLK}$-$\Delta t_{Rise/Fall}$, -6 ns	-	-	15	ns

Figure 4. SPI timing diagram

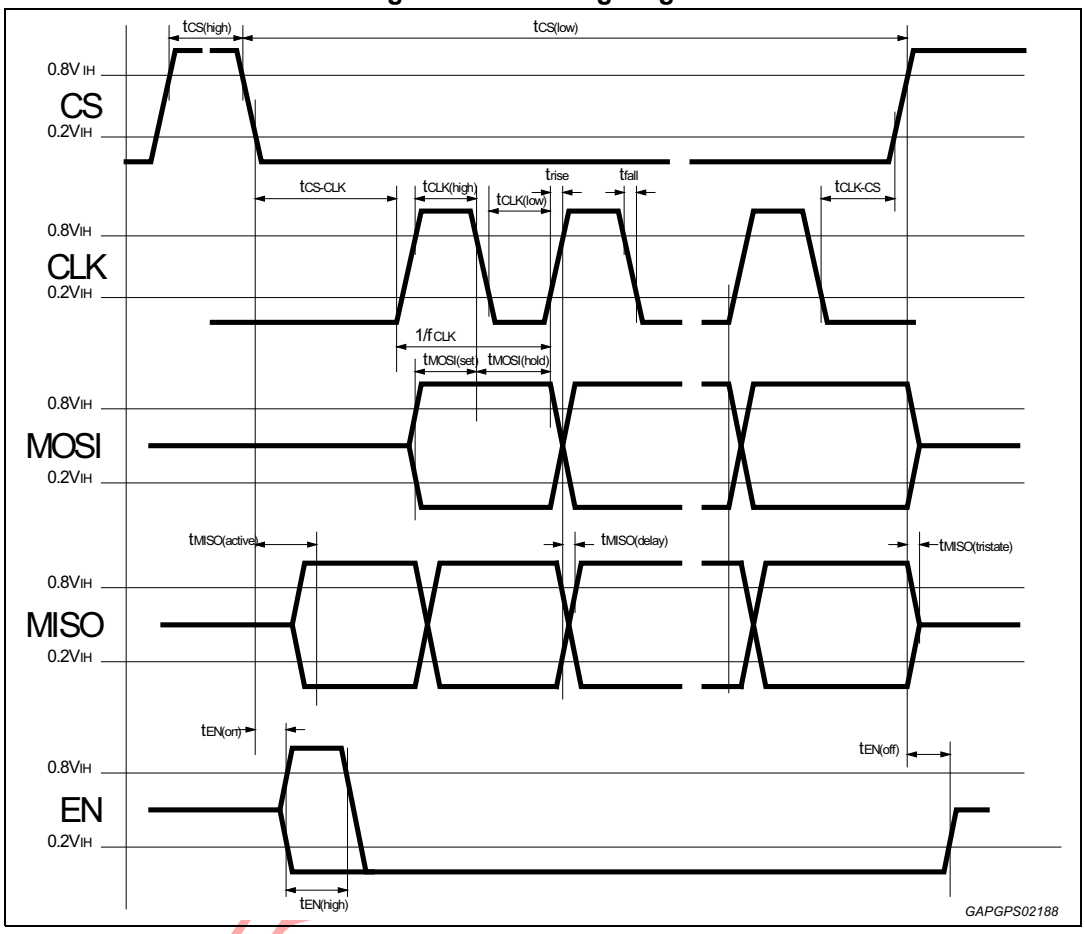


Table 17. CLKin threshold parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{CLKin(low)}$	Input low threshold	-	1.0	-	-	V
$V_{CLKin(high)}$	Input high threshold	-	-	-	2.0	V
$V_{CLKin(Hyst)}$	Input threshold hysteresis	-	0.2	0.5	1.0	V
I_{CLKin}	CLKin input current (pin to GND)	0.5 V < V_{CLKin} < V3	35	50	65	µA
f_{CLKin}	Input frequency range	-	DC	-	5	MHz

Table 18. CLKin timing parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\Delta\%f_{CLKin}$	Signal frequency accuracy requirements	Not including jitter, tested @ 4MHz	-2	-	+2	%
$\%DC_{CLKin}$	Signal duty cycle	t_{High} x f_{CLKin} x 100%	40	50	60	%
f_{Jitter}	CLKin jitter frequency	-	100	4	-	kHz
Δf_{Jitter}	CLKin jitter amplitude	-	-	40	-	kHz

Table 18. CLKin timing parameters (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$\Delta f_{(low)}$	Compares f_{OSC} and f_{CLKin}	Set CLKin_Fail = 1 if below this threshold	0.1	-	0.4	x f_{CLKin}
$\Delta f_{(high)}$	Compares f_{OSC} and f_{CLKin}	Set CLKin_Fail = 1 if above this threshold	2.5	-	10	x f_{CLKin}
$t_{CLKin(fail)}$	Failure detection filtering time	Incorrect frequency must be detected for this length of time to post a failure on CLKin_Fail	3	10	20	µs

4 Application information

The L9390 is a 12 channel open drain / low side valve driver for an ABS / Vehicle Stability system. All of the outputs can be PWMmed while some will require an external diode to do so. 6 of the outputs can drive a load using current regulation.

4.1 Supply monitoring

4.1.1 Low voltage inhibit (Vs(LVI))

The Vs supply has a low voltage warning function with hysteresis. When Vs drops below Vs(LVI) a bit is set in the SPI diagnostic register

4.2 General output functionality

Each of the 12 outputs are open drain configured. Each output has a built in 35V clamp and 8 of the 12 have integrated active freewheeling diodes for active rectification of the PWMmed loads. At loss of Dx, the output can be switched off and clamped regardless of the presence of a freewheeling diode.

The DMOS outputs have the option of having controlled switch on/off slopes to minimize EMC during actuation or PWM. This feature can be enabled or disabled via SPI.

All of the outputs can be asynchronously turned off either via the SPI "ALL_OFF" command or via the "OUT_EN" input pin. There are two (2) ALL_OFF SPI register bits that must be specifically configured to disable the outputs.

Table 19. Outputs disable registry map

BIT 0	BIT 1	ALL_OFF status
0	0	Not allowed
1	1	Not allowed
1	0	All outputs disabled immediately
0	1	Normal Operation

The outputs can be switched on directly using the SPI as well. When the OUT_ON_EN bit is set the OUT_ONx bits are OR'ed with the appropriate HET input commands to drive the specified output (s) on.

Table 20. SPI outputs disable

ALL_OFF	OUT_ONx	OUT_ON _EN	OUTx Commanded status1	OUTx state
10	X	X	X	All Outputs Off
01	0	X	X	No Change
01	X	0	X	No Change
01	1	1	X	OUTx ON

Four possible states On / PWM / Current regulated / Off

Thermal protection is performed in on-state driver pairs. The pairs are set up to be configured with other driver types to minimize both drivers in the pair from being on at the same time. Refer to the over temperature detection portion in the Diagnostics section.

Table 21. Diagnostic output

Output pairs	
1	5
2	6
3	7
4	8
9	11
10	12

The power grounds are also paired in like manner to optimize the current flow through the ground leads and reduce ground offset.

4.2.1 Edge shaping

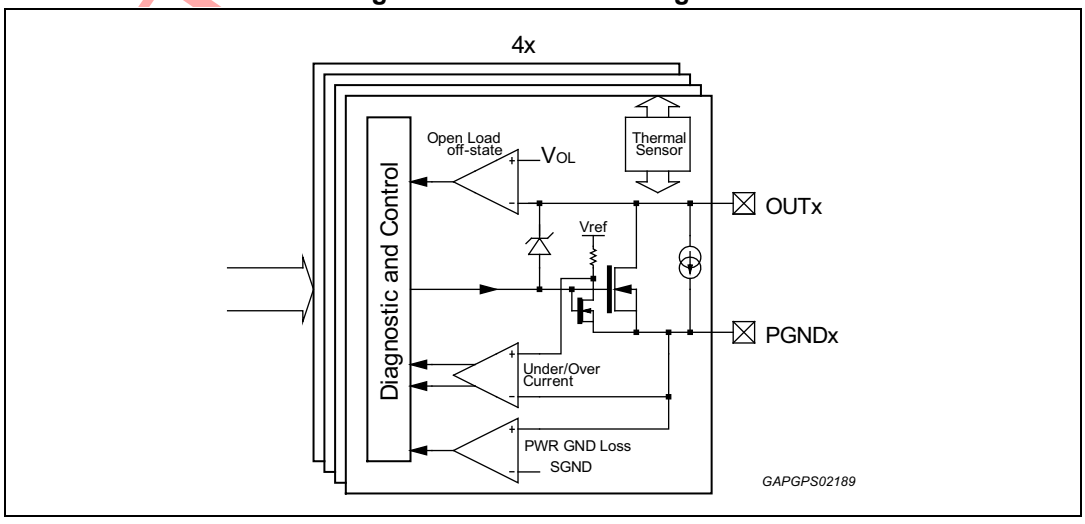
When the SHAPE_En bit is set the output rising and falling edges are controlled in a manner to minimize the EMI that can be generated by continuous PWMming of a load. The edges have a dual slope to both minimize the EMI as well as minimize the power dissipated during switching. Refer to *Figure 3* for a graphic of the edge shaping.

When the SHAPE_EN bit is not set the slope is fixed to 20 V/s.

4.2.2 Out1-out4

These outputs are configured as switching drivers. There is not internal active diode for PWMming. However these outputs can be PWMmed if an external diode is present. The PWM duty cycle and frequency is accomplished through the serial HET input commands.

Figure 5. Out1-4 block diagram

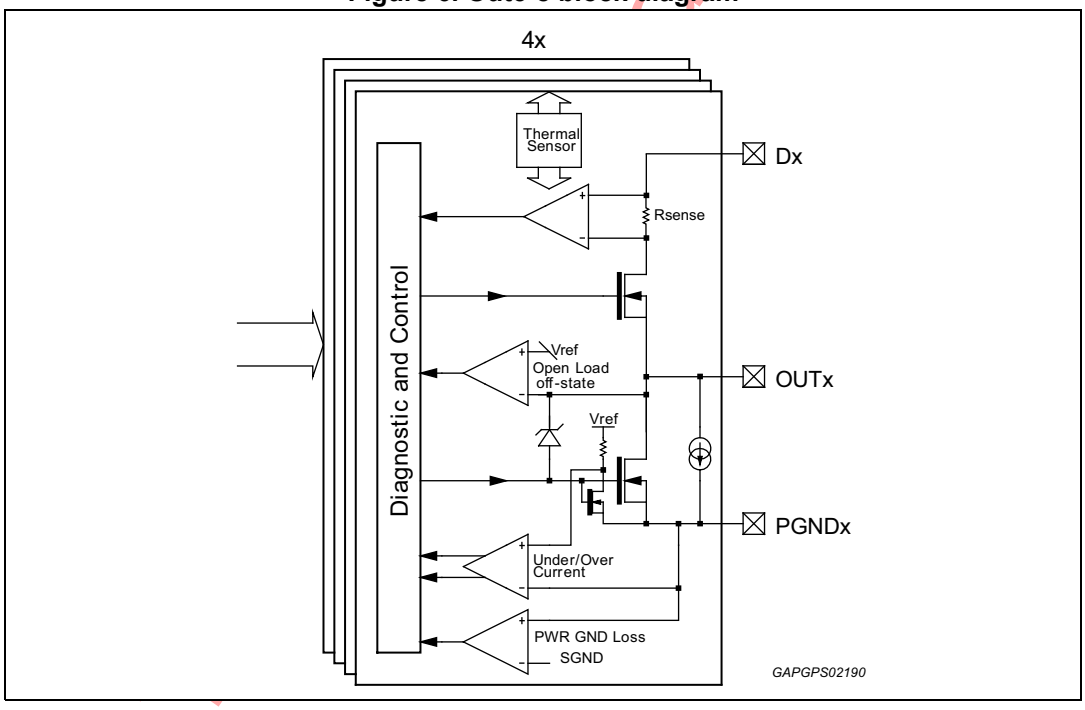


These outputs have over current protection, under current detection, open load (off state), voltage clamp, loss of ground detection, loss of freewheeling diode (when one is used in the circuit), and shared thermal shutdown.

4.2.3 Out5-out8

Outputs 5 through 8 are Current Controlled outputs. They include a freewheeling MOSFET for synchronous rectification. These outputs will regulate to a commanded current within $I_{OUT(tol)}$ %. The frequency and current levels are commanded via the serial HET interface. They can be selected as current controlled outputs, PWMmed outputs, or switched outputs via the SPI.

Figure 6. Out5-8 block diagram

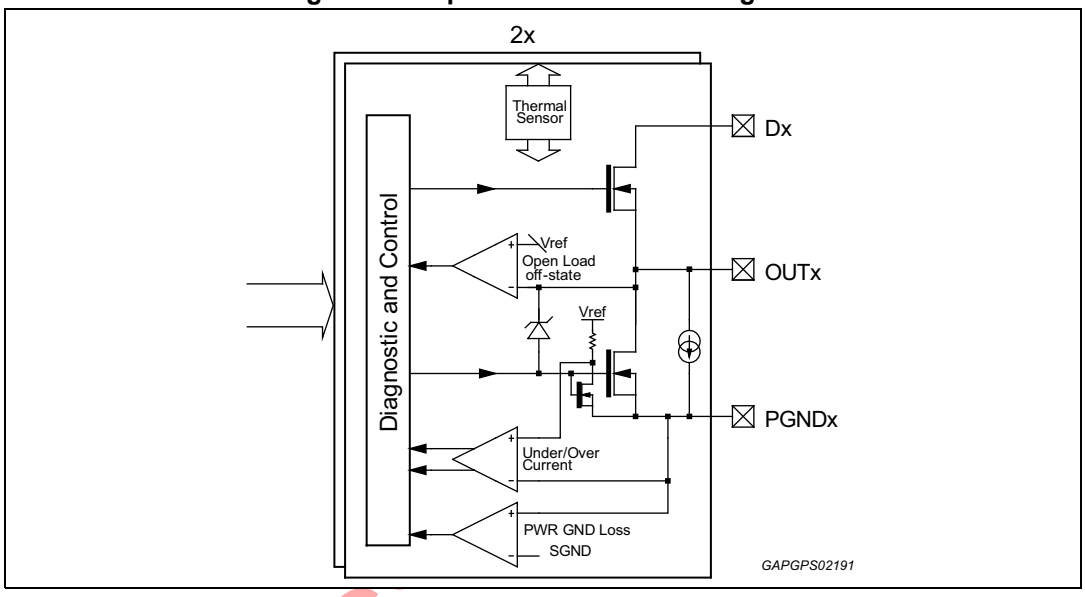


These outputs have over current protection, under current detection, current not achieved detection, open load (off state), voltage clamp, loss of ground protection, loss of freewheeling diode and shared thermal shutdown.

4.2.4 Out9-out10

Outputs 9 and 10 are PWM controlled outputs. They include a freewheeling MOSFET for synchronous rectification. The PWM frequency and duty cycle is commanded through the serial HET interface. They can be selected as PWMmed outputs, or switched outputs via the SPI.

Figure 7. Outputs 9 and 10 block diagram

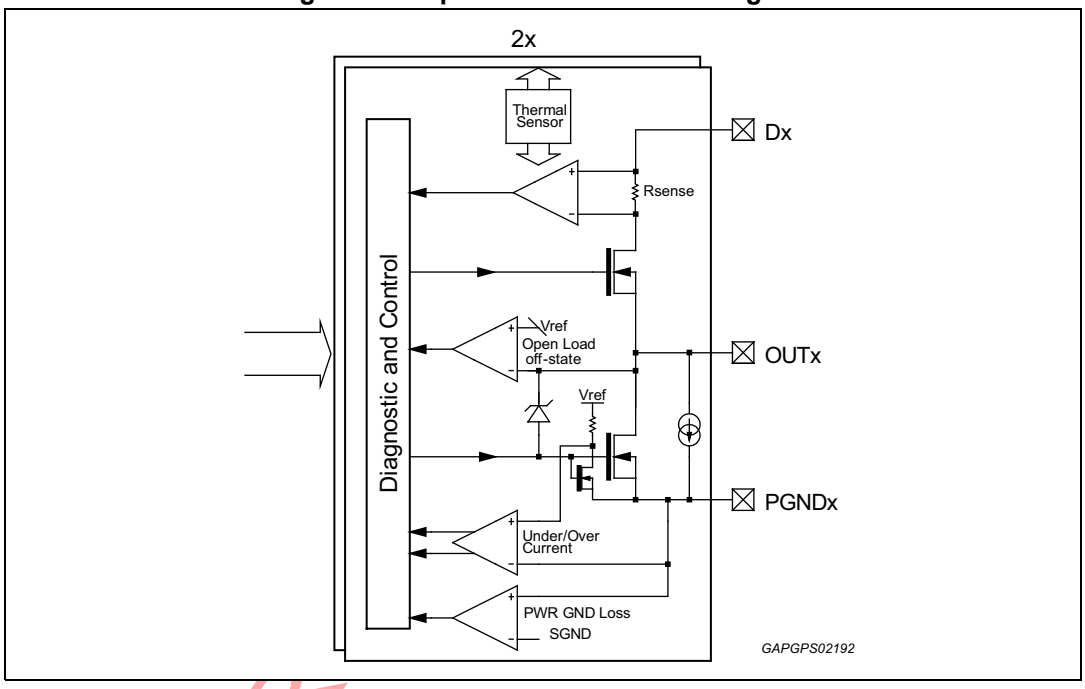


These outputs have over current protection, under current detection, open load (off state), voltage clamp, loss of ground protection, loss of freewheeling diode, and shared thermal shutdown.

4.2.5 Out11-out12

Outputs 11 through 12 are current controlled outputs. They include a freewheeling MOSFET for synchronous rectification. These outputs will regulate to a commanded current within IOUT(tol) %. The current level is commanded via the serial HET interface. They can be used as current controlled outputs, PWMmed outputs, or switched outputs.

Figure 8. Outputs 11 and 12 block diagram



These outputs have over current protection, under current detection, current not achieved detection, open load (off state), voltage clamp, loss of ground protection, loss of freewheeling diode and shared thermal shutdown.

5 Serial communications

There are two separate conduits of communication into and out of the L9390. These are the 5 pin SPI port and the 6 serial HET inputs. The SPI port is primarily designated to provide diagnostics and secondary control. The serial HET inputs provide the primary output control functions from on/off switching to current level control commands.

5.1 SPI data bus

The SPI bus addresses several registers within the L9390. Each of the registers are 24 bits wide. The address, data and parity bits add up to a total of 31 for the SPI transmission.

5.2 SPI safety features

Parity

To ensure proper communication every SPI frame has a parity bit (odd). If a parity error is detected then the data is discarded and the PAR_Fail Bit is set.

Clock monitor

The number of clock pulses for each frame is counted. If this number is incorrect then the data is discarded and the PAR_Fail bit is set.

Master to Slave address correlation

To verify a proper transmission a subsequent Slave frame contains the same address information as the initial Master frame.

Unused addresses

The SPI addresses 00H and FFH are not used.

SPI read error

Reading a non-existing address will cause a SPI read failure and set the RAd_Fail bit.

SPI write error

Writing to a non-existent or non-writable address will cause a SPI write error and will set the WAd_Fail bit. Writing to an address that has both writable and only readable bit will not cause a failure. This also applies to addresses that have both writable and un-used bits.

Writing a bit combination that is not allowed will also cause a WAd_Fail bit to be set. If this is attempted the bit values will not be changed.

5.3 SPI commands / registers

Acknowledgement / wake-up

The initial SPI Slave-to-Master transmission after a RESET contains all 1's except for bit 31. If a Master-to-Salve transmission contains an error (incorrect parity, etc) all 31 bits in the subsequent Slave-to-Master transmission will be all 1's.

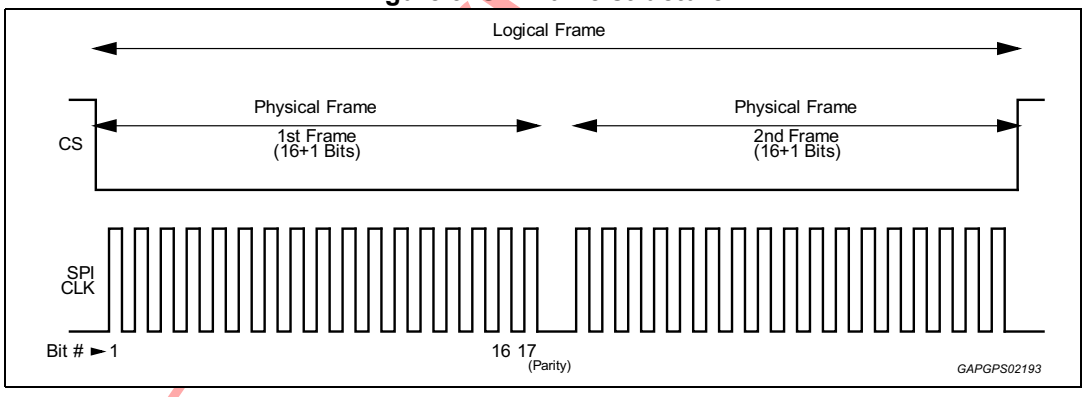
Table 22. Acknowledgement / wake-up

Bit	31	30-24	23-0
Initial Slave-to-Master Tx after RESET	0	1	1
Master-to-Slave Rx Error detected	1	1	1

SPI command / register description

The SPI command word consists of parity (1 bit), address (7 bits), and Command/Data (24 bits) sections. The following descriptions are done by SPI address. The SPI addresses used are 20H through 35H.

Figure 9. SPI frame structure



5.3.1 Revision ID, Device ID, SPI status

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
20H	R	Revision identification								Device identification								EN_Set	TEST_En	SGND_L	AV_Config	Par_Fail	WAd_Fail	RAd_Fail	Takt_Fail
Normal operation		0	0	0	1	0	0	0	1	0	1	1	0	1	0	0	0	X	0	0	X	0	0	0	0

Table 23. Revision ID, Device ID, SPI status characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	After POR	After RESET address
23 -16	Revision ID	“11HEX”	Read	“11HEX”	no	“11HEX”	“11HEX”
15 -8	Device ID	“60HEX”	Read	“60HEX”	no	“60HEX”	“60HEX”
7	EN_set	“0” = OUT_EN < V_{IL} “1” = OUT_EN > V_{IH}	Read	One or more low signal detected since last SPI polling	Set to “1” if input = “high”	X	X
6	Test_eN	“1” = ASIC testmode active	Read	“1” if ASIC testmode activated one or more times since last SPI polling	Reset bit	0	0
5	SGND_L	“1” = SGND_L is lost “0” = normal operation	Read	One or more failures detected since last SPI polling	set to “0”	0	0
4	AV_config	“0” = configuration 1 “1” = configuration 2	Read	current	no	x	x
3	Par_Fail	"1" = SPI / parity failure detected	Read	One or more SPI messages failed since last SPI polling	Reset bit	0	0
2	WAd_Fail	"1" = Write address failure detected	Read	One or more SPI messages failed since last SPI polling	Reset bit	0	0
1	RAd_Fail	"1" = Read address failure detected	Read	One or more SPI messages failed since last SPI polling	Reset bit	0	0
0 LSB	CLK_Fail	"1" = CLK failure detected	Read	One or more SPI messages failed since last SPI polling	Reset bit	0	0

5.3.2 Direct driving of outputs, edge shaping, feedback configuration

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
21H	R/W	OUT_ON12	OUT_ON11	OUT_ON10	OUT_ON9	OUT_ON8	OUT_ON7	OUT_ON6	OUT_ON5	OUT_ON4	OUT_ON3	OUT_ON2	OUT_ON1	CUR_PWM		VRS_Meas		LDT_En	SHAPE_En	ALL_OFF		Not Used	OUT_ON_EN	SVDT	
Normal operation		X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	1	1	0	1	X	X	X	X

Table 24. Direct driving of outputs, edge shaping, feedback configuration characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default (After POR)	After RESET address
23-12	OUT_ONx	Output enable OUT1...OUT12	Read/ write	Present value	Set to new value	0	0
11-10	CUR_PWM (For OUT5-OUT8, OUT11, OUT12)	Current regulation or PWM control Switch: “01” = Current regulation (default) “10” = PWM actuated valve driver	Read/ write	Present value	Set to new value	01	01
9-8	VRS_Meas	$V_{RSsense}$ switch: “x1” = on “x0” = off	Read/ write	Present value	Set to new value	00	00
7	LDT_en	Leakage detection test switch “1”= off (normal operation), “0”= on (Leakage test)	Read/ write	Present value	Set to new value	1	1
6	SHAPE_En	Edge Shaping Switch “1”= On (normal operation) “x0” = off (no edge shaping)	Read/ write	Present value	Set to new value	1	1
5-4	ALL_OFF	Output Disable Switch “01” = normal operation “10” = All outputs switched off	Read/ write	Present value	Set to new value	01	01
3	Not used					0	0
2	OUT_ON_EN	SPI Driven outputs enable switch “1” = OUT_ONx commands enabled “0” = Disables SPI driving capability	Read/ write	Present value	Set to new value	0	0
1-0 LSB	SVDT	Enables Silent Valve Driver Test: “10” = Enabled “01” = Disabled	Read/ write	Present value	Set to new value	01	01

5.3.3 Input diagnostic feedback

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
22H	R	HET_Fail6	HET_Fail5	HET_Fail4	HET_Fail3	HET_Fail2	HET_Fail1	Not Used	Osc_Fail	VCP_Fail	CLKin_Fail	Vs_Fail	V3_Fail	LD_Fail12	LD_Fail11	LD_Fail10	LD_Fail9	LD_Fail8	LD_Fail7	LD_Fail6	LD_Fail5	LD_Fail4	LD_Fail3	LD_Fail2	LD_Fail1
Normal Operation		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25. Input diagnostic feedback characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default (After POR)	After RESET address
23 - 18	HET_Fail(x) (HET6 – HET1)	“1” = Inx Tx failure “0” = normal operation	Read	One or more failures detected since last SPI polling	set to “0”	0	0
17	Not used					0	0
16	Osc_Fail	“1” = Oscillator failure detected	Read	One or more failures detected since last SPI polling	set to “0”	0	0
15	VCP_Fail	"1" =VCP<VCP_{LVI}	Read	Present	no	0	0
14	CLKin_Fail	“1” = CLKIn failure detected	Read	One or more failures detected since last SPI polling	set to “0”	0	0
13	Vs_Fail	“1” = Vs < $Vs_{(LVI)}$ “0” = normal operation	Read	One or more failures detected since last SPI polling	set to “0”	0	0
12	V3_Fail	“1” = V3 < $V3_{(LVI)}$	Read	One or more failures detected since last SPI polling	set to “0”	1	0
11-0 LSB	LD_Fail(x)	“1” = I_{OUTx}>I_{DET} “0” = I_{OUTx}<I_{DET}	Read	One or more failures detected since last SPI polling	set to “0”	0	0

5.3.4 Output feedback, one address per output

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
23H-2EH	R	SVDT_OUTx	PWM_MUXx	Edge_OUTx						LOW_OUTx										PWM_CKx		Not Used	OC_OUTx	UC_OUTx	OL_OUTx
Normal operation		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

There are 12 registers represented, from 23H to 2EH.
There is one register for each output.
OUT1 is referenced to 23H… OUT12 is referenced to 2EH

Table 26. Output feedback, one address per output characteristics

Bit #	Function	Level	R R/W W	Status at SPI Polling	Function after SPI polling	Default (After POR)	After RESET address
23	SVDT_OUTx 1-12 1 referenced to 23H ... 12 referenced to 2EH	“1” = SVDT failure detected	Read	One or more failures detected since last SPI polling	set to “0”	0	0
22	PWM_MUXx	“0” = PWM-Check at OUTx “1” = PWM-Check performed at GATEx	Read	Present	No	0	0
21-16	Edge_OUTx	Number of positive edges in one HET sequence (6 bits)	Read	Present	set to “0”	0	0
15-6	LOW_OUTx	Number of low time counts in one HET sequence	Read	Present	set to “0”	0	0
5-4	PWM_CKx	“00” = Busy/Inactive: “01” = Sequence 1 “10” = Sequence 2 “11” = Sequence 3	Read	Present	no	0	0
3	Not used				0	0	0
2	OC_OUTx	“1” = $I_{OUTx} > I_{OCx}$ Over current detection	Read	One or more failures detected since last SPI polling	set to “0”	0	0
1	UC_OUTx	“1” = $I_{OUTx} < I_{UC}$ Under current detection	Read	One or more failures detected since last SPI polling	set to “0”	0	0
0 LSB	OL_OUTx	“1” = $V_{OUTx} < V_{OL}$ Off state open load detection	Read	One or more failures detected since last SPI polling	set to “0”	0	0

5.3.5 Current regulation commands, two outputs per address

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2FH	R	Not Used	Not Used	CNA_Fail6	CREG_OUT6										CNA_Fail5	CREG_OUT5									
30H	R	Not Used	Not Used	CNA_Fail8	CREG_OUT8										CNA_Fail7	CREG_OUT7									
31H	R	Not Used	Not Used	CNA_Fail12	CREG_OUT12										CNA_Fail11	CREG_OUT11									
Normal Operation		0	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X

Table 27. Current regulation commands, two outputs per address characteristics

Bit #	Function	Level	R R/W W	Status at SPI Polling	Function after SPI polling	Default(After POR)	After RESET address
23-22	Not Used				0	0	0
21	CNA_Fail(x) OUT6, OUT8, OUT12	Current for Out6, 8, &12 is not achievable	Read	Present	no	0	0
20-11	CREG_OUT(x) OUT6, OUT8, OUT12	Current PWM values for Out6,8,&12	Read	Present	no	0	0
10	CNA_Fail(x) OUT5, OUT7, OUT11	Current for Out5, 7, &11 is not achievable	Read	Present	no	0	0
9-0 LSB	CREG_OUT(x) OUT5, OUT7, OUT11	Current PWM values for Out5. 7. &11	Read	Present	no	0	0

5.3.6 Diagnostics - feedback, Dx lost, over temperature, power ground lost

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
32H	R	OT1012	OT911	OT48	OT37	OT26	OT15	PGL1012	PGL911	PGL48	PGL37	PGL26	PGL15	D1_Loss	D2_Loss	D3_Loss	D4_Loss	D5_Loss	D6_Loss	D7_Loss	D8_Loss	D9_Loss	D10_Loss	D11_Loss	D12_Loss
Normal Operation		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28. Diagnostics - feedback, Dx lost, over temperature, power ground lost characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default (after POR)	After RESET address
23-18	OTxy ([channelx][channely])	"1" = T_{Jxy}>T_{OT} Over temperature detection	Read	One or more failures detected since last SPI polling	set to "0"	0	0
17-12	PGNDLxy ([channelx][channely])	"1" = V_{PGNDxy}>V_{SGND}+V_{PGS}	Read			0	0
11-0 LSB	Dx_loss	"1" = V_{OUT} > 35 V @ turn-off, Free-wheeling diode channel lost all outputs	Read			0	0

5.3.7 Gate monitoring feedback

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
33H	R	out1_off	out2_off	out3_off	out4_off	out5_off	out6_off	out7_off	out8_off	out9_off	out10_off	out11_off	out12_off	gate1_on	gate2_on	gate3_on	gate4_on	gate5_on	gate6_on	gate7_on	gate8_on	gate9_on	gate	gate	gate
Normal operation		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 29. Gate monitoring feedback characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default (After POR)	After RESET address
23-12	OUTx_Off	Gate monitor 1 (Off state monitoring)	Read	One or more events detected since last SPI polling	set to "0"	0	0
11-0 LSB	GATEx_On	Gate monitor 2 (On state monitoring)				0	0

5.3.8 Current regulation P/I parameters

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
34H	R/W	KI_OUT12		KP_OUT12		KI_OUT11		KP_OUT11		KI_OUT8		KP_OUT8		KI_OUT7		KP_OUT7		KI_OUT6		KP_OUT6		KI_OUT5		KP_OUT5	
Normal Operation		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 30. Current regulation P/I parameters characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default after POR)	After RESET address
23-22 19-18 15-14 11-10 7-6 3-2	KI_OUT12 KI_OUT11 KI_OUT8 KI_OUT7 KI_OUT6 KI_OUT5	Programming of Ki coefficient OUTx: “00” Ki=700 “01” Ki=1000 “10” Ki=1200 “11” Ki=1600	Write/ read	Present	Set to new value	00	00
21-20 17-16 13-12 9-8 5-4 1-0LSB	KP_OUT12 KP_OUT11 KP_OUT8 KP_OUT7 KP_OUT6 KP_OUT5	Programming of Kp coefficient OUTx: “00” Kp=1.5 “01” Kp=2.0 “10” Kp=3.0 “11” Kp=4.0	Write/ read	Present	Set to new value	00	00

5.3.9 Built in self test functionality

Address	R, R/W, W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
35H	R/W	Not used	Not used	Not used	Not used	Not used	Start/busy	R = BIST2R W = BIST2C								Not used	Start/busy	R = BIST1R W = BIST1C							
Normal Operation		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 31. Built in self test functionality characteristics

Bit #	Function	Level	R R/W W	Status at SPI polling	Function after SPI polling	Default (After POR)	After RESET address
23- 19	Not used				0	0	0
18	Start/busy2	“0” = BIST2 Busy	W/R	Present	Set to new value	0	0
17-10	BIST2C (8 bits)	Program initial CRC command value for BIST2	W	Present	Set to new value	0	0
17-10	BIST2R (8 bits)	BIST2 Answer	R	Present	Set to new value	0	0
9	Not Used				0	0	0
8	Start/busy1	“1” = BIST1 Busy	W/R	Present	Set to new value	0	0
7-0 LSB	BIST1C (8 bits)	Program initial CRC command value for BIST1	W	Present	Set to new value	0	0
7-0 LSB	BIST1R (8 bits)	BIST1 answer	R	Present	Set to new value	0	0

5.3.10 Serial HET bus configuration

Data bits	D61	D60	D59	…		D49	D48	D47	…		D37	D36	D35	…	D31	D30	…	D26	D25	D24	D23	D22
Normal operation	0	1	Duty x D59: MSB				1	Duty y D47: MSB			1	Freq x D35: MSB				Freq y D35: MSB			0	1	AV x on	AV y on
Data bits	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Normal operation	PWM-Check		Details: see *Table 32*						1	0	0	0	0	0	0	0	0	0	0	0	0	1

Table 32. Serial HET input bit description

Bit	HET1	HET2	HET3	HET4	HET5	HET6
0	Data transfer					
12-1	“000HEX”: Synchronization					
13	“1”: Separator					
14	Enable OUT2(1)	Enable OUT4(1)	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”
15	Enable OUT1(1)	Enable OUT3(1)	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”
16	Enable OUT6	Enable OUT8	Enable OUT10	Enable OUT12	Enable OUT2	Enable OUT4
17	Enable OUT5	Enable OUT7	Enable OUT9	Enable OUT11	Enable OUT1	Enable OUT3
18	“1” = PWM-Check to GATEx (OUT5, OUT6, OUT1, OUT2)(1)	“1”= PWM-Check to GATEx (OUT7, OUT8, OUT3, OUT4)(1)	“1”: PWM-Check to GATEx (OUT9, OUT10)	“1”: PWM-Check to GATEx (OUT11, OUT12)	“1”: PWM-Check to GATEx (OUT1, OUT2)	“1”: PWM-Check to GATEx (OUT3, OUT4)
19	Leakage test enable (OUT5, OUT6, OUT1, OUT2)(1)	Leakage test enable (OUT7, OUT8, OUT3, OUT4)(1)	Leakage test enable (OUT9, OUT10)	Leakage test enable (OUT11, OUT12)	Leakage test enable (OUT1, OUT2)	Leakage test enable (OUT3, OUT4)
21-20	PWM_Check Enable bits (OUT5, OUT6, OUT1, OUT2)	PWM_Check Enable bits (OUT7, OUT8, OUT3, OUT4)	PWM_Check Enable bits (OUT9, OUT10)	PWM_Check Enable bits (OUT11, OUT12)	PWM_Check Enable bits (OUT1, OUT2)	PWM_Check Enable bits (OUT3, OUT4)
22	OUT2 Switch on(1)	OUT4 Switch on(1)	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”
23	OUT1 Switch on(1)	OUT3 Switch on(1)	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”	Not used Fixed to “0”
25-24	“01”: Separator and Resync.					
30-26	Frequency for OUT6	Frequency for OUT8	Frequency for OUT10	Frequency for OUT12	Frequency for OUT2	Frequency for OUT4
35-31	Frequency for OUT5	Frequency for OUT7	Frequency for OUT9	Frequency for OUT11	Frequency for OUT1	Frequency for OUT3
36	“1”: Separator					
47-37	Current or duty for OUT6 (10bit used)	Current or duty for OUT8 (10bit used)	Duty for OUT10 (10bit used)	Current or duty for OUT12 (10bit used)	Duty for OUT2 (10bit used)	Duty for OUT4 (10bit used)
48	“1”: Separator					
59-49	Current or duty for OUT5 (10bit used)	Current or duty for OUT7 (10bit used)	Duty for OUT9 (10bit used)	Current or Duty for OUT11 (10bit used)	Duty for OUT1 (10bit used)	Duty for OUT3 (10bit used)

1. When HET5 is low (100% or grounded) then OUT1-OUT4 are controlled as a switch using the "Enable OUTx" bits (14-15) and the "OUTx Switch on" bits (22-23) OF HET1 and HET2. Otherwise HET5 and HET6 commands OUT1-OUT4 as a PWM driver and an external diode is required.

6 Diagnostics

The diagnostics are designed to check and double check circuits internal and external to they device. Load integrity as well as internal circuit integrity are verified with specific testing capabilities within the device.

6.1 Conditions that cause a reset

Reset conditions override any other states/conditions in the L9390. The fault conditions that cause a logical reset with the L9390 are, Undervoltage on the 3V3 pin, OUT_EN pin active low, and CLKin failure. Unless otherwise specified a RESET condition will include:

- All outputs disabled
- All digital information reset or set to 0
  - All set points
  - All duty cycle durations
  - All counters
  - All status registers (default value is 0)
- All inputs, outputs and data buffers are set to the default values
- The INx input module is held in the reset condition

6.1.1 Under voltage

An under voltage condition detected on the V3 (3.3V supply) will cause a RESET.

Table 33. Under-voltage characteristics

Parameter	Condition	Min	Typ	Max	Units
$V3_{UV}$	L9390 in RESET	2.5	2.75	2.95	Volts
t_{UV}	Filtering time	4	-	20	µs
$V3_{UV(BG)}$	3.3V_fail bit set in SPI register	-4	-	+4	%
$t_{UV(BG)}$	Filtering time	100	-	400	µs

6.1.2 OUT_EN = 0 ("EN_set" Bit = 0)

At EN_set = 0 the L9390 will enter a RESET state. In addition to the normal reset conditions all pull down current sinks at each OUTPUT are disabled.

The EN_set bit shows the level of the OUT_EN Pin. If the value of the OUT_EN was low for the last time since the last accessing to this register the status EN_set bit is low. This bit is cleared by accessing this address.

6.1.3 CLKin-failure ("CLKin_fail" Bit = "1")

At CLKin_fail = "1" the L9390 will react by entering the normal RESET mode plus the following:

- All inputs, outputs and data buffers are set to the default values
- The HETx Module will be held in the reset condition.
- The status register is not influenced during a CLKin-failure

6.2 Fault monitoring

Fault monitoring provides status of the outputs. In some cases the outputs are shut off to protect them. In other cases the output states are not altered by the fault detected.

6.2.1 Open load detection (off-state)

Off-State open load is detected by monitoring the load voltage on the output. When active, an internal pull down current source at each output will bring the output voltage below VOL when a load is not present.

This feature is available at all outputs. The status of the open load is stored for each channel in the SPI status register in the OL_OUTx Bit. The bit is set ("1") when an open load condition is detected after a filter time and cleared once the register is read. It can be set again by actuating and then disabling the offending output or by executing the SVDT test.

The open load condition does not prevent the affected output from being actuated nor does it affect the overall operation of the L9390.

Table 34. Open load characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{OL}, Open Load Threshold	Output Off,	0.3	0.33	0.36	xV_S
t_{OL}	Filtering time	10	20	40	µs

Open load is detected when the output voltage is below this threshold.

6.2.2 Under current detection

An under current condition is detected when the current through a driver in an on-state is below the threshold (I_{UC}) for longer than the filtering time (t_{UC}). Undercurrent detection is available on all outputs

Once an undercurrent condition is detected, the undercurrent detection bit, UC_OUTx, for each channel is set ("1"). This bit only reflects the present status of the output and is not latched. However, this bit can be latched at the end of the SVDT test.

During an SVDT, the under current status is latched at the falling edge of the gate signal. The under current detection bit is reset by accessing the address.

The under current condition does not disable the affected output nor does it affect the overall operation of the L9390.

Table 35. Under current characteristics

Parameter	Condition	Min	Typ	Max	Units
I_{UC}, under current threshold	Output On All outputs	50	10	140	mA
t_{UC}	Filtering time	10	20	40	µs

Under current is detected when the output current is below this threshold.

6.2.3 Over current detection

An over current condition is detected when the current through an enabled output is above the over current threshold (I_{OCx}) for longer than the filtering time (t_{OC}). Over current detection is available on all outputs.

Once an over current condition is detected the offending output is disabled, the over current detection bit (OC_OUTx) is latched ("1"), and all setpoint and control variables for that output are reset to "0".

Accessing the offending output register address will reset the OC_OUTx bit and allow the output to be re-enabled.

Table 36. Over current characteristics

Parameter	Condition	Min	Typ	Max	Units
I_{OC1}, over current threshold	Output On, OUT1-4, OUT9-10	6.9		10.1	A
I_{OC2}, over current threshold	Output On, OUT5-8, OUT11-12	3.2		4.8	A
t_{OC}	Filtering time, switch-off delay	10	20	40	µs

Over current is detected when the output current is above this threshold.

Over current detection is also a part of the SVDT test.

6.2.4 Over temperature detection

Over temperature is detected when the thermal sensor associated with the offending output senses a temperature above T_{OT} for t_{OT}. When an over temperature is detected, the output is disabled, the corresponding over temperature bit (OTxy) is set, and the all setpoint and control variables for that output are reset to "0". Over temperature detection is available for all outputs. The offending output is re-enabled once the register for that output is accessed via the SPI bus.

For thermal protection there is one thermal sensor for every two outputs. Each sensor has associated with it one SPI data bit, OTxy. The thermal sensor is enabled only when one or both of its associated outputs (x or y) are enabled.

The thermal sensors sense the following pairs of outputs:

Table 37. Sensor outputs

Sensor bit	Shared outputs	
OT15	1	5
OT26	2	6
OT37	3	7
OT48	4	8
OT911	9	11
OT1012	10	12

Table 38. Over temperature characteristics

Parameter	Condition	Min	Typ	Max	Units
T_{OT}, Over Temperature Threshold	Output On, all outputs	190	205	220	°C
ΔT_{OT}, Over Temperature Hysteresis	-	-	20	-	°C
t_{OT}	Filtering time, switch-off delay	10	20	40	µs

Over temperature is detected when the thermal sensor measures a temperature above this threshold

6.2.5 Loss of PGND

There are 6 different power ground pairs in the L9390. The output power grounds are paired (connected by metal) before exiting the device. The Power Grounds for each output pair (PGNDxy) are monitored for continuity with Signal Ground (SGND).

Table 39. Power ground outputs

Loss of PGND bit	Common grounds	
PGNDL15	1	5
PGNDL26	2	6
PGNDL37	3	7
PGNDL48	4	8
PGNDL911	9	11
PGNDL1012	10	12

When the voltage difference between one of these grounds and SGND is greater than VPGS for more than tPGS then the offending outputs are disabled, the PGNDLxy bit is set ("1"), and all set point and control variables are reset. An output can be re-enabled once the fault has been removed by accessing the SPI status register and reading the PGNDLxy Bit. As long as the fault is present the offending outputs will not be able to be actuated. The output is not required to be enabled for this fault to be detected.

Table 40. Loss of PGND characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{PGS}	Loss of PGND threshold	1.0		2.0	V
$V_{PGS(Hyst)}$	Hysteresis	0.2		0.5	V
t_{PGS}	Filtering time, switch-off delay	10	20	40	µs

Power ground is lost when the voltage between this pin and SGND exceeds this threshold. A Loss of power ground is also detected during SVDT testing.

6.2.6 Loss of freewheeling diode (Dx)

Loss of freewheeling diode (Dx-Loss) testing is available for all outputs. For this test to be valid for outputs OUT1-OUT4, an external freewheeling diode is required.

Loss of a freewheeling diode is detected by sensing a voltage greater that V_{FW} for at least t_{FW} after the offending output is disabled. Once a loss of freewheeling diode is detected the Dx_Loss bit is set. This bit can be reset by accessing the address of the offending output.

Table 41. Loss of freewheeling diode (Dx) characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{FW}	Loss of diode threshold		35		V
t_{FW}	Filtering time	1	2	5	µs

Loss of freewheeling diode is detected when the output voltage is above this threshold.

This function is also used in the SVDT test.

6.2.7 Output integrity check

The Output Integrity check is two tests that verify that the output MOSFET is indeed functioning. These tests are:

- Gate Threshold voltage detection (GATEx_On)
- Off state output current detection (OUTx_Off)

The output MOSFET Gate voltage is monitored to determine if it is above or below the threshold ($V_{GS(on)}$). The GATEx_On bit is set if the output is commanded on and the gate voltage is measured to be above $V_{GS(on)}$. Once set, this bit is not reset when the output is turned off and the gate voltage drops below the threshold.

The OUTx_Off bit is set if an output is disabled and the drain current is below $I_{OUTx(off)}$. This bit is not reset when an output is turned back on

Table 42. Output integrity check outputs

State	GATEx_On	OUTx_Off
On	1	0
Off	0	1
Actuated	1	1
Fault	0	0

The OUTx_Off and the GATEx_On bits are only reset by accessing the corresponding Output SPI address

Table 43. Output integrity check characteristics

Parameter	Condition	Min	Typ	Max	Units
$V_{GS(on)}$, Gate –source threshold	Output On, is detected when the gate voltage is above this threshold	2.5	-	-	V
$I_{OUTx(off)}$ Off-state output current threshold	Output Off, is detected when the current measured in the output is below this threshold	-	-	1	mA

6.2.8 PWM-Integrity monitor

The PWM-Integrity monitor performs two measurements. It counts the positive edges on an output between HET PWM commands and it counts the accumulated low time on the outputs between HET PWM commands.

The PWM-Integrity test is performed using either the open load comparator or the GATEx monitor comparator. This selection is programmable via the serial HET interface bit 18 and is reflected in the SPI status register (PWM_CKx). When HETx bit 18 is "1" the PWM-Integrity test is performed using the GATEx comparator for the corresponding outputs (see *Table 42* for more details). When the HETx bit 18 is "0" the PWM-Integrity test is performed using the open load comparator at the corresponding outputs.

A current PWM must be completed before the PWM-Integrity test will start or stop. The PWM-Integrity test starts or stops with falling edge of the busy flag of the actuation register.

Edge counting (Edge_OUTx)

Table 44. PWM-Integrity monitor characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{OL} threshold	Rising edges increment the Edge_OUTx counter – no filtering	0.3	0.33	0.36	xV_S
$V_{GS(on)}$ threshold	Looking for high to low transitions	2.5	-	-	V
Register size	# of bits for counting	-	6	-	bit
Max # of positive edges	@ 4 kHz over a 15 ms period = 60	-	-	63	counts

All output positive edges are counted since the last access to the corresponding HET register. All low to high transitions are measured using the (OFF state) open load voltage comparator. If the GATEx comparator is selected the falling edges are counted as the gate voltage is an inversion of the output voltage.

Additionally, the duration of the output in low, or "ON", state is accumulated and stored in a 10 bit register (LOW_OUTx). An output low time is defined as the duration at which the output voltage falls below the (off-state) open load voltage. If the GATEx comparator is

selected (HETx bit 18="0") then the output "low" is determined by the GATE voltage being above the GATEx threshold.

Both of these registers stop accumulating once the maximum count has been reached. There is no overflow. Both values are cleared by accessing the data in their corresponding output register.

On-time level monitoring

Table 45. On-time level monitoring characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Looking for “Low” on output	0.3	0.33	0.36	xV_S
$V_{GS(on)}$	Looking for “High”	2.5	-	-	V
f_T Time Base Frequency	Depending on CLKin Resolution to 20µs	-	50	-	kHz
Register size	# of bits fro counting	-	10	-	bit
Max low level duration	20 µs period counting 1024 steps	-	20	-	ms

6.2.9 PWM-check functionality

The PWM-Check test is controlled using the serial High End Timer (HET) protocol and read back through the SPI port. To identify the correct PWM Check test sequence, two bits are transferred through the serial HET interface (PWM_Check Enable bits) defining three sequences: "Sequence 1", "Sequence 2" and "Sequence 3". The two bits are necessary since actuation of these tests and reading the results are asynchronous (Serial HET vs. SPI).

The bit indices Sequence 1, 2, or 3 enables a correlation between the PWM-check test results and HETx valve driver actuation. The actual valid index is set by the serial HET protocol. The HET sequence commands are stored in the 2 bit read only SPI address PWM_CKx.

Table 46. PWM-check outputs

PWM_CKx bits	Function
00	Busy / Inactive
01	Sequence 1
10	Sequence 2
11	Sequence 3

As long as the PWM check test is active, according to the related serial HET protocol, a flag is set which does not allow reading back the register content of the related registers (Edge_OUTx, and LOW_OUTx) via SPI. After a "stop" command via HETx has been received and the current PWM is finished the PWM check test stops and the related registers can be read back via SPI.

By performing this test the entire chain of control from HETx to OUTx is verified.

6.2.10 Current regulator PWM-Feedback

For the current regulated outputs, the value of the current PWM duty cycle is stored in the SPI register CREG_OUTx. There is one 10 bit register for each of the current regulated outputs.

6.2.11 Current not achieved detection

This monitor detects when the current regulated outputs have not attained their requested value. This may occur when the supply voltage is insufficient to generate enough current in the Valve.

Table 47. Current not achieved detection characteristics

Parameter	Condition	Min	Typ	Max	Units
I_{SET} Current Not Reachable Threshold	Set by input command (current Set-Point)				A
t_{FW}	Filtering time	9.75	10	10.25	ms

The failure "Current not achieved" can be read back via the SPI port with the bit CNA_failx.

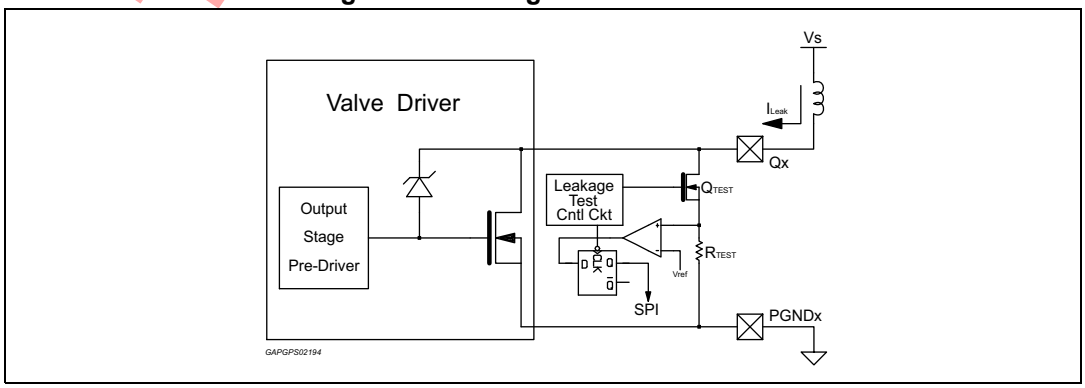
6.2.12 Leakage current test

The leakage current test measures the amount of residual current there is in the load (Valve) when the corresponding output is disabled. This test relies on the load, a valve, being inductive in nature. As a result, this test includes the potential leakage from components attached to the output as well as the output MOSFET internal to the L9390.

This test is available for all output drivers. Some delay after disabling the output must pass to ensure that there is no current still freewheeling in the load at the start of the test.

The leakage current test is performed only on disabled outputs. The test is actuated when the leakage test bit LDT_En in the SPI register and the HET Leakage test bit for that output are set to "1". The test is actuated at the completion of a serial HET frame.

Figure 10. Leakage detection circuit



Test concept

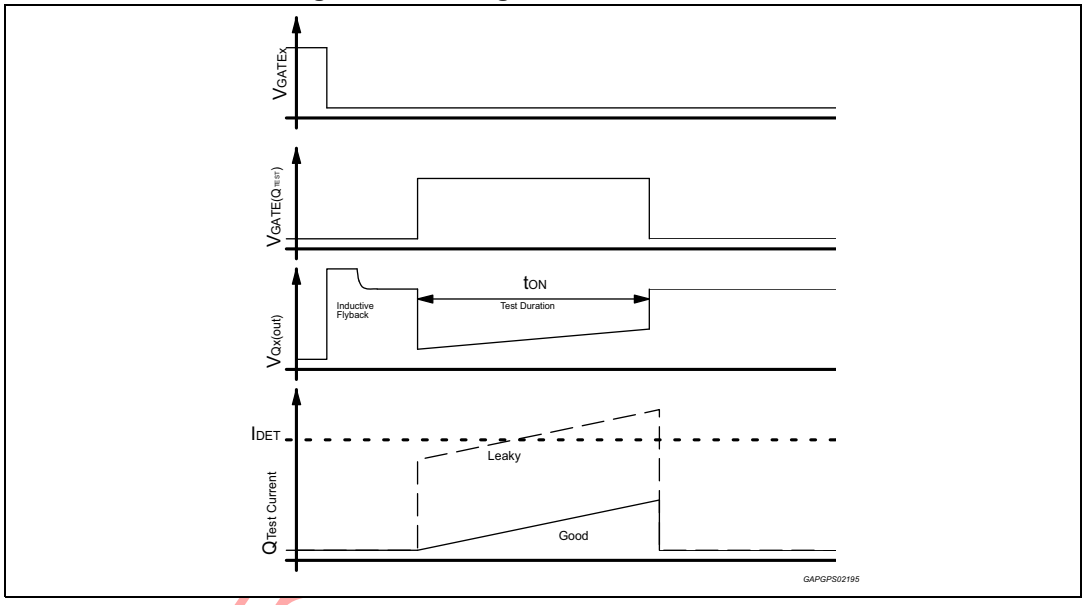
The current through the valve under test is expected to be zero (as the output is "off"). QTEST at OUTx will pull the voltage at OUTx low but the current flow through OUTx is

expected to be 0 at t = 0 since the inductive behavior of the valve leads to a controlled current increase proportional to the equation:

$$\text{ALVE} \approx \frac{v_s}{L} \cdot t_C$$

If there is a leakage current to Power Ground when Q_{TEST} is enabled the leakage current will flow through Q_{TEST} as the resistive path is much lower through Q_{TEST} +R_{TEST} than what was available prior to the initiation of the test. Even though the output voltage will drop the current will not change appreciatively as the load is fairly inductive.

Figure 11. Leakage detection waveforms



Measuring the voltage across RTEST determines the quality of the leakage current. If the leakage current measured is above IDET then the SPI bit LD_OUTx is set ("1"). This bit is reset upon reading this register.

Table 48. Leakage current test characteristics

Parameter	Condition	Min	Typ	Max	Units
Q_{TEST} $R_{DS(on)}$	T_j = 175 °C	-	-	5	Ω
RTEST	Test sense resistor value		1	-	Ω
t_{DELAY}	Q_{TEST} turn on delay time	-		250	ns
t_{ON} Q_{TEST} on-time	Q_{TEST} on for defined time	9	-	10	µs
I_{DET} threshold	Values above this level are determined to be high leakage	90	100	110	mA
t_{LK} Leakage current filter time	Duration based on CLK	7	-	8	µs
Δt, t_{ON}-t_{LK}	Time difference between t_{ON} and t_{LK}	1.5	-	2.5	µs

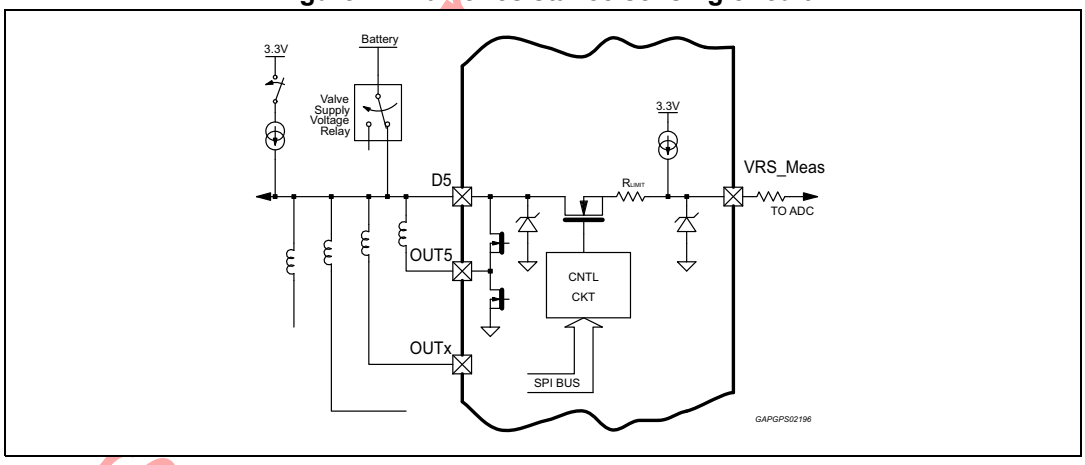
Verifying the leakage test circuit

To test the Leakage test circuit the reference to compare the leakage current can be disabled via SPI. If the SPI command LDT_En is set to "0", the leakage current reference (Vref) is disabled causing the leakage test to always fail even when no leakage current is present. By this we determine if the leakage test circuit is present and functioning.

6.2.13 Valve resistance sense switch

A cyclic test is done to measure the valve resistance to detect failures (inter-turn short circuit or contact resistance). For this test, the valve Supply Voltage relay is switched off and an external current source is switched on (see *Figure 12*). Then each valve driver is switched on in turn. At this point the voltage at the Valve Source voltage node depends on the current of the current source and the resistance of the valve and the valve driver. The Valve Source voltage must be read in by the ADC in the microcontroller. To get the necessary accuracy, the voltage must be read in directly and not divided. Therefore a switch from Valve Source voltage (at the D5 pin) is switched on to the VRS_Meas pin, which goes through a protection resistor to the ADC of the microcontroller. The switch is necessary to avoid a continuous clamping current in the ADC over the life of the module. The current source is external to the L9390.

Figure 12. Valve resistance sensing circuit



Description

The voltage is measured at D5, the diode connection of the valve driver Q5 free wheeling diode. The Valve Resistance Sense switch from D5 to VRS_meas is switched on by setting the SPI bit VRS_Meas to "x1" and switched off by setting the SPI bit VRS_Meas to "x0". The pull up current source is necessary to get a defined level, if the switch is switched off.

6.2.14 Valve resistance test sequence:

1. Disconnect the battery from the High side of the valves (open Valve Supply Voltage Relay- see *Figure 11*).
2. Bias up the current source (from the 3.3V supply).
3. Turn on any one valve.
4. Measure the voltage on D5 through the VRS_Meas pin using an ADC on the micro. This voltage will be a result of the bias current through the valve impedance.
5. Repeat for the other 11 valves.

6.3 Additional monitoring

6.3.1 SGND-loss

The SGND-loss monitors the voltage between SGND and PGND. If the measured value is higher than the threshold (VSGL) for (tSGL) the SPI bit SGND_L is set, all outputs are switched off immediately and all set points are reset. Once the fault is removed the SGND_L register can be cleared when the register is accessed.

Table 49. SGND-loss characteristics

Parameter	Condition	Min	Typ	Max	Units
V_{SGL} signal ground offset threshold	At voltages sensed above this value a fault is registered	0.2	0.35	0.5	V
t_{SGL}	Filtering time	0.5		2.0	ms

6.3.2 SPI-monitoring (SPI-watchdog)

If there is no SPI communication after a delay of tWDfault the L9390 exhibits the following behavior:

- All outputs disabled
- All set points set to "0"
- All duty cycle durations are set to "0"
- All counters are set to "0"
- All status registers are unmodified

Table 50. SPI-monitoring (SPI-watchdog) characteristics

Parameter	Condition	Min	Typ	Max	Units
$t_{WDfault}$ watchdog fault time	Incorrect or no SPI communication within this period determines a fault	20		25	ms

The SPI-watchdog is only reset by a correct SPI communication. (SPI transfer failure can also cause a SPI-watchdog failure)

6.3.3 Voltage reference monitoring (bandgap monitoring)

The L9390 internal bandgap voltage is compared to the external 3.3 V supply voltage (V3). If the bandgap voltage leaves the specified voltage range the V3_fail SPI bit will be set.

6.4 Silent valve driver test (SVDT)

The silent valve driver test (SVDT) checks the DMOS output as well as the valve loads. Because the valve is switched on for a very short time during the test, the current in the loads remain very low. Subsequently the valves are not actuated and there is no observable valve noise.

The SVDT is initiated via a SPI command and tests all outputs sequentially automatically. The SVDT is disabled immediately if an actuation request is made via the serial HET inputs. The following monitoring signals are used:

- Open load (off-state)
- Over current
- Under current
- Dx-loss
- Over temperature

The SVDT starts directly after the SPI command SVDT_EN (10) is communicated. This is a 2 bit command where only one combination is acceptable to begin the test.

Table 51. Silent valve driver test (SVDT) outputs

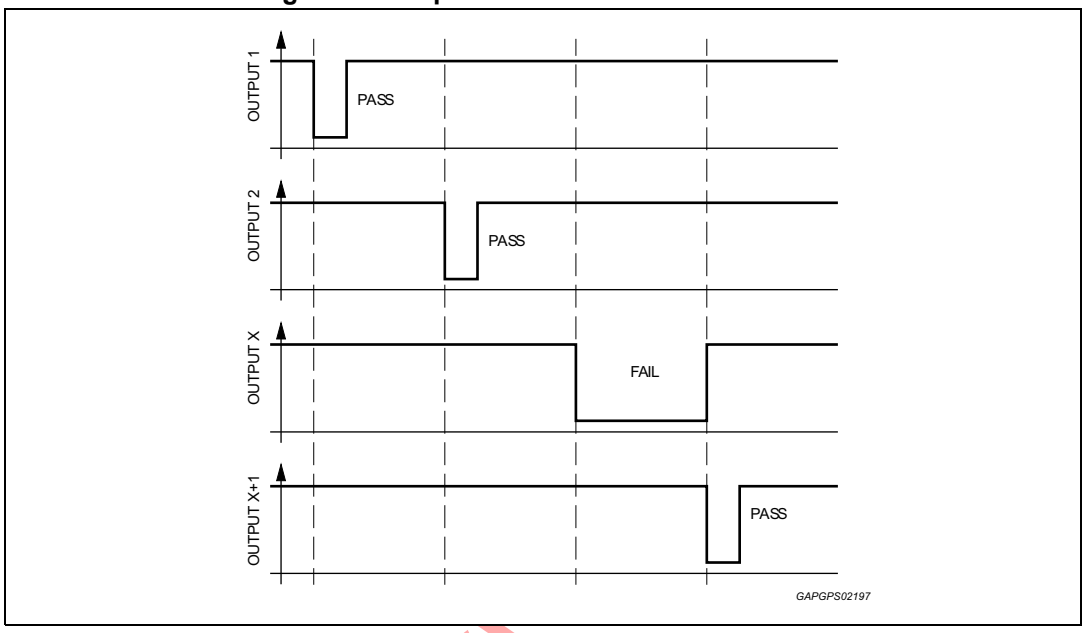
SVDT	Bit 1	Bit 0
Not possible	0	0
Normal operation / no test	0	1
SVDT active (in test mode)	1	0
Not possible	1	1

When the SVDT has completed testing all of the outputs, the SVDT_EN bits are reset (01) and the test is halted. To restart the test the SVDT_EN bits must be rewritten as (10). All of the output status bits are stored within the SPI output feedback registers (SPI address 23H-2EH). Accessing the output status registers after the SVDT is completed clears these registers.

Table 52. Silent valve driver test (SVDT) characteristics

Parameter	Condition	Min	Typ	Max	Units
tx Test time	Output passed	90	100	110	µs
ty Test time	Output failed	450	500	550	µs

Figure 13. Sequential nature of the SDVT test



6.4.1 The SVDT test sequence:

1. Software sets SVDT_EN to (10)
2. OUTx switches on at the next sync-signal (sequence of actuation: Q1.Q12)
3. Because the output is actuated the output current increases.
4. At time tx, if the output current has exceeded the under current value, I_{UC}, the output is switched off.
5. If the over current threshold (I_{OC}) is achieved prior to tx then the output is immediately disabled and an over current condition is detected.
6. The output will switch off any time prior to exceeding time ty if the undercurrent threshold, I_{UC}, has been met.
7. After the output is disabled if the output clamps the voltage to V_{CLAMP} (35V) a Dx_Loss is detected. This criterion only applies to those channels with freewheeling diodes.
8. If an Over temperature is not detected then the SDVT test is passed
9. The SVDT will then test at OUTPUT X+1 until all 12 outputs have been tested.

Figure 14. SVDT output voltages, normal and shorted loads

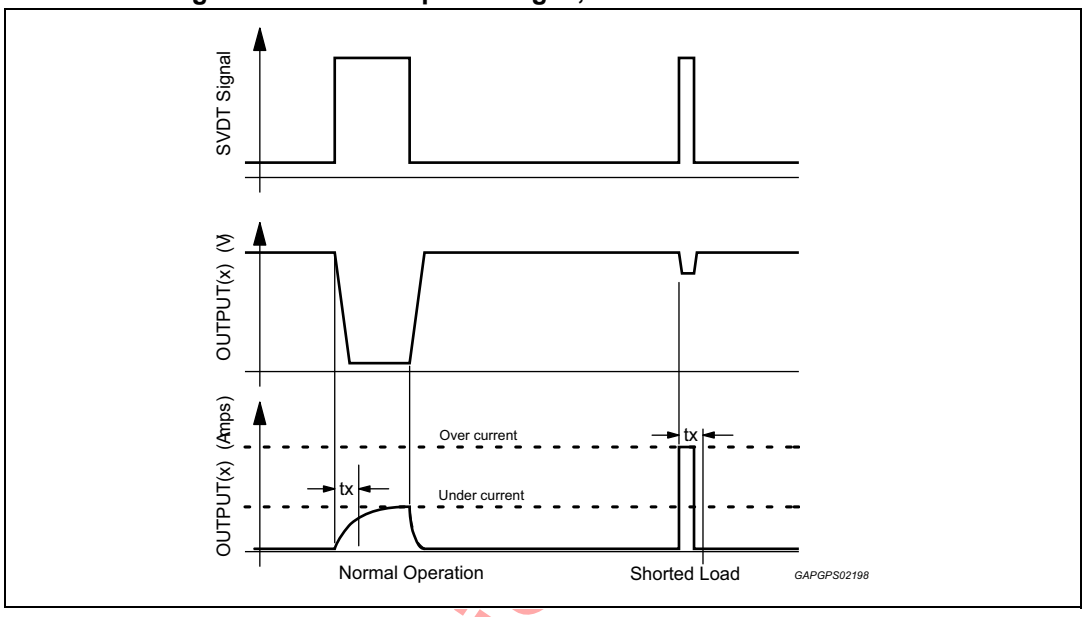
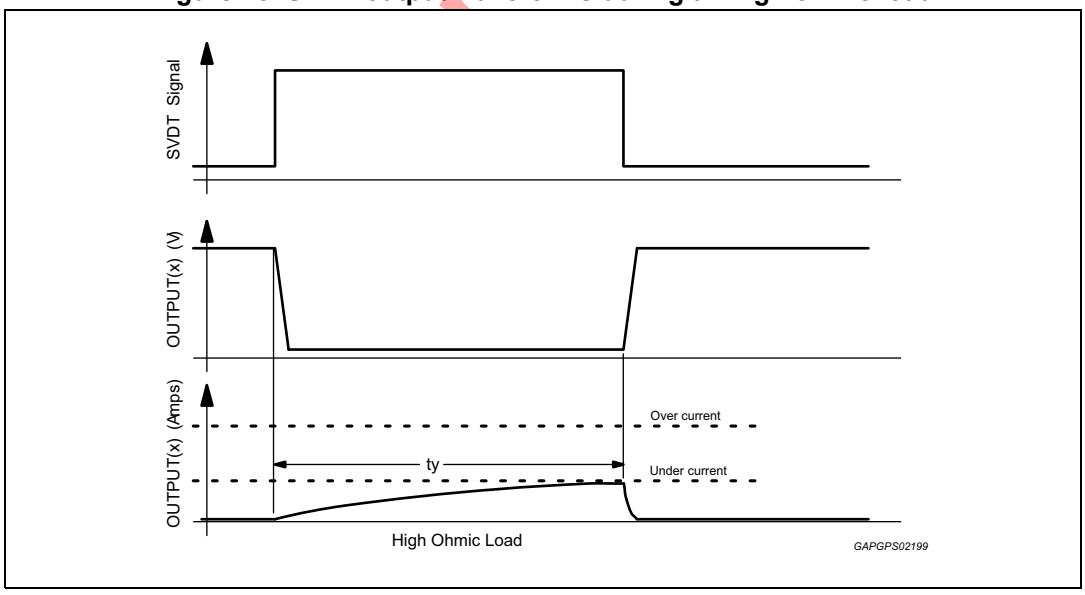


Figure 15. SVDT output waveforms during an high ohmic load



What is considered a passed SVDT test is:

1. No over current detected
2. The current increased to above the undercurrent value within the specified time, tx < t < ty.
3. No clamping function at turn off (free-wheeling diode present)

Table 53. Data results of SVDT

Dx_Loss	Over current	Under current	Description	SVDT State
0	0	0	Passed SVDT test	0
0	0	1	High ohmic or high inductance load	1
0	1	0	Over current or shorted load	1
0	1	1	Not possible	1
1	0	0	Dx_Loss	1
1	0	1	Dx_Loss or high ohmic or high inductance load	1
1	1	0	Dx_Loss or shorted load	1
1	1	1	Not possible	1

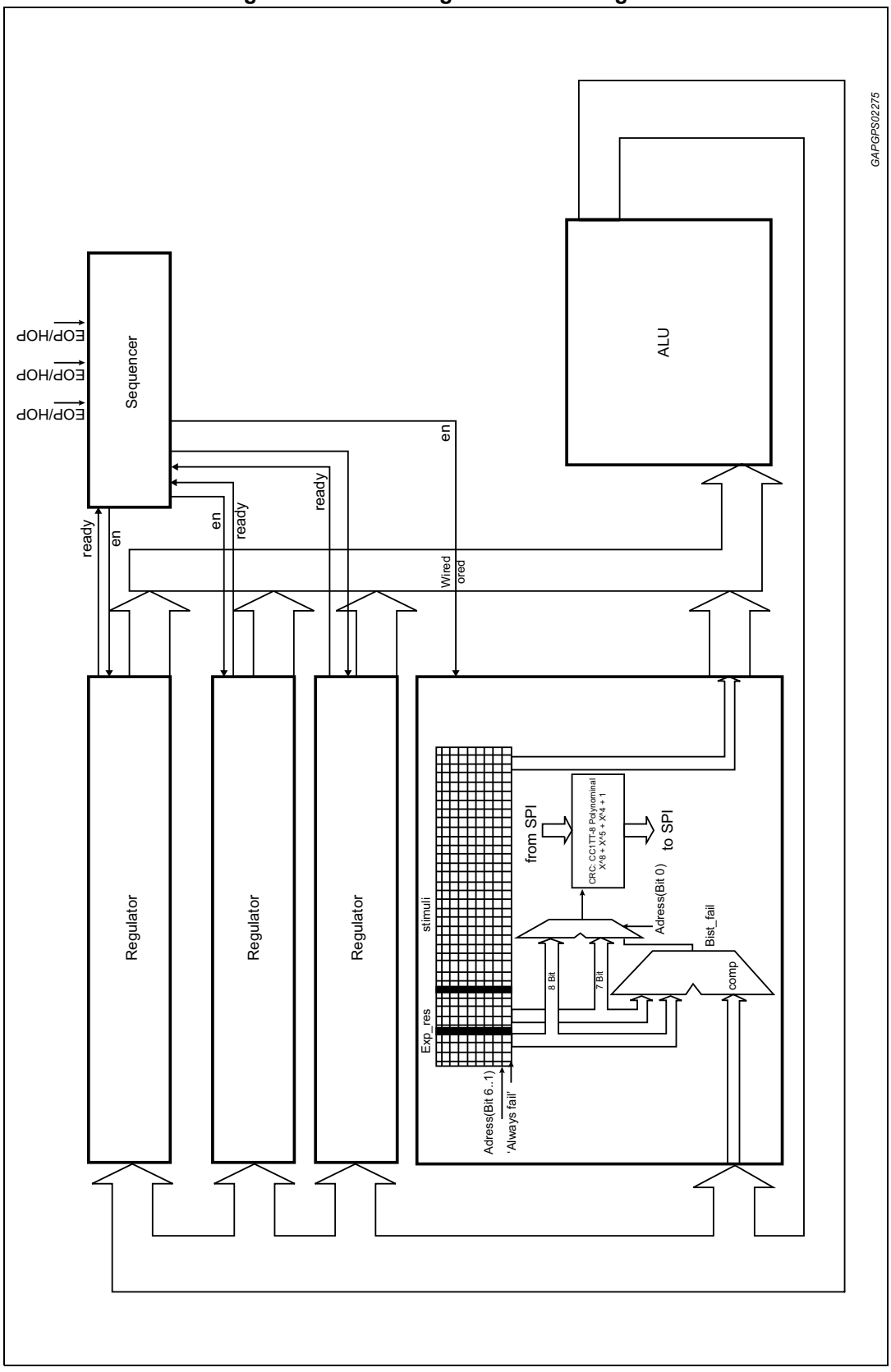
6.4.2 Built in self-test (BIST)

A built in self-test for the ALU of the current regulator is implemented according the block diagram shown in *Figure 16* below.

The BIST is initiated via a SPI command. The initial value (Init) of the CRC is programmed via SPI (8bit/ALU). The resulting CRC value can be read back by SPI after the BIST has been completed. The CRC value is depending on the programmed initial value of the CRC. To verify the BIST failure comparator, an "always fail" bit from the expected result address register is implemented. Current regulation takes precedence over the BIST. If during BIST, a regulation algorithm for the ALU is requested, the running BIST will be halted.

The maximum BIST test time (without interruption because of a regulation request) is 100µs.

Figure 16. Current regulator block diagram



6.4.3 Built-in self test CRC initiator and results

Table 54. Built-in self test CRC initiator and results

Init	Res	Init	Res	Init	Res	Init	Res	Init	Res	Init	Res	Init	Res	Init	Res
0	173	32	51	64	136	96	22	128	231	160	121	192	194	224	92
1	221	33	67	65	248	97	102	129	151	161	9	193	178	225	44
2	77	34	211	66	104	98	246	130	7	162	153	194	34	226	188
3	61	35	163	67	24	99	134	131	119	163	233	195	82	227	204
4	116	36	234	68	81	100	207	132	62	164	160	196	27	228	133
5	4	37	154	69	33	101	191	133	78	165	208	197	107	229	245
6	148	38	10	70	177	102	47	134	222	166	64	198	251	230	101
7	228	39	122	71	193	103	95	135	174	167	48	199	139	231	21
8	6	40	152	72	35	104	189	136	76	168	210	200	105	232	247
9	118	41	232	73	83	105	205	137	60	169	162	201	25	233	135
10	230	42	120	74	195	106	93	138	172	170	50	202	137	234	23
11	150	43	8	75	179	107	45	139	220	171	66	203	249	235	103
12	223	44	65	76	250	108	100	140	149	172	11	204	176	236	46
13	175	45	49	77	138	109	20	141	229	173	123	205	192	237	94
14	63	46	161	78	26	110	132	142	117	174	235	206	80	238	206
15	79	47	209	79	106	111	244	143	5	175	155	207	32	239	190
16	226	48	124	80	199	112	89	144	168	176	54	208	141	240	19
17	146	49	12	81	183	113	41	145	216	177	70	209	253	241	99
18	2	50	156	82	39	114	185	146	72	178	214	210	109	242	243
19	114	51	236	83	87	115	201	147	56	179	166	211	29	243	131
20	59	52	165	84	30	116	128	148	113	180	239	212	84	244	202
21	75	53	213	85	110	117	240	149	1	181	159	213	36	245	186
22	219	54	69	86	254	118	96	150	145	182	15	214	180	246	42
23	171	55	53	87	142	119	16	151	225	183	127	215	196	247	90
24	73	56	215	88	108	120	242	152	3	184	157	216	38	248	184
25	57	57	167	89	28	121	130	153	115	185	237	217	86	249	200
26	169	58	55	90	140	122	18	154	227	186	125	218	198	250	88
27	217	59	71	91	252	123	98	155	147	187	13	219	182	251	40
28	144	60	14	92	181	124	43	156	218	188	68	220	255	252	97
29	224	61	126	93	197	125	91	157	170	189	52	221	143	253	17
30	112	62	238	94	85	126	203	158	58	190	164	222	31	254	129
31	0	63	158	95	37	127	187	159	74	191	212	223	111	255	241

6.4.4 SPI command / register summary

Table 55. SPI command / register summary

Address	R R/W W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
20H	R	Revision identification								Device identification								EN_Set	TEST	SGND_L	AV_Config	Par_Fail	WAd_Fail	RAd_Fail	Takt_Fail
21H	R/W	OUT_ON12	OUT_ON11	OUT_ON10	OUT_ON9	OUT_ON8	OUT_ON7	OUT_ON6	OUT_ON5	OUT_ON4	OUT_ON3	OUT_ON2	OUT_ON1	CUR_PWM		VRS_Meas		LDT_En	SHAPE_En	ALL_OFF		Not used	OUT_ON_EN	SVDT	
22H	R	HET_Fail6	HET_Fail5	HET_Fail4	HET_Fail3	HET_Fail2	HET_Fail1	Not used	Osc_Fail	VCP_Fail	CLKin_	Vs_Fail	V3_Fail	LD_Fail12	LD_Fail11	LD_Fail10	LD_Fail9	LD_Fail8	LD_Fail7	LD_Fail6	LD_Fail5	LD_Fail4	LD_Fail3	LD_Fail2	LD_Fail1
23H	R	SVDT_out1	PWM_MUX1	Edge_OUT1						LOW_OUT1										PWM_CK1		Not used	OC_OUT1	UC_OUT1	OL_OUT1
24H	R	SVDT_out2	PWM_MUX2	Edge_OUT2						LOW_OUT2										PWM_CK2		Not used	OC_OUT2	UC_OUT2	OL_OUT2
25H	R	SVDT_out3	PWM_MUX3	Edge_OUT3						LOW_OUT3										PWM_CK3		Not used	OC_OUT3	UC_OUT3	OL_OUT3
26H	R	SVDT_out4	PWM_MUX4	Edge_OUT4						LOW_OUT4										PWM_CK4		Not used	OC_OUT4	UC_OUT4	OL_OUT4
27H	R	SVDT_out5	PWM_MUX5	Edge_OUT5						LOW_OUT5										PWM_CK5		Not used	OC_OUT5	UC_OUT5	OL_OUT5
28H	R	SVDT_out6	PWM_MUX6	Edge_OUT6						LOW_OUT6										PWM_CK6		Not used	OC_OUT6	UC_OUT6	OL_OUT6
29H	R	SVDT_out7	PWM_MUX7	Edge_OUT7						LOW_OUT7										PWM_CK7		Not used	OC_OUT7	UC_OUT7	OL_OUT7

Table 55. SPI command / register summary (continued)

Address	R R/W W	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
2AH	R	SVDT_out1	PWM_MUX	Edge_OUT8						LOW_OUT8										PWM_CK8		Not used	OC_OUT8	UC_OUT8	OL_OUT8
2BH	R	SVDT_out9	PWM_MUX	Edge_OUT9						LOW_OUT9										PWM_CK9		Not used	OC_OUT9	UC_OUT9	OL_OUT9
2CH	R	SVDT_out10	PWM_MUX	Edge_OUT10						LOW_OUT10										PWM_CK10		Not used	OC_OUT10	UC_OUT10	OL_OUT10
2DH	R	SVDT_out11	PWM_MUX	Edge_OUT11						LOW_OUT11										PWM_CK11		Not used	OC_OUT11	UC_OUT11	OL_OUT11
2EH	R	SVDT_out12	PWM_MUX	Edge_OUT12						LOW_OUT12										PWM_CK12		Not used	OC_OUT12	UC_OUT12	OL_OUT12
2FH	R	Not used	Not used	CNA_Fail6	CREG_OUT6										CNA_Fail5	CREG_OUT5									
30H	R	Not used	Not used	CNA_Fail8	CREG_OUT8										CNA_Fail7	CREG_OUT7									
31H	R	Not used	Not used	CNA_Fail12	CREG_OUT12										CNA_Fail11	CREG_OUT11									
32H	R	OT_1012	OT_911	OT_48	OT_37	OT_26	OT_15	PGL_1012	PGL_911	PGL_48	PGL_37	PGL_26	PGL1_5	D1_Loss	D2_Loss	D3_Loss	D4_Loss	D5_Loss	D6_Loss	D7_Loss	D8_Loss	D9_Loss	D10_Loss	D11_Loss	D12_Loss
33H	R	OUT1_off	OUT2_off	OUT3_off	OUT4_off	OUT5_off	OUT6_off	OUT7_off	OUT8_off	OUT9_off	OUT10_off	OUT11_off	OUT12_off	GATE1_on	GATE2_on	GATE3_on	GATE4_on	GATE5_on	GATE6_on	GATE7_on	GATE8_on	GATE9_on	GATE10_on	GATE11_on	GATE12_On
34H	R/W	KI_OUT12		KP_OUT12		KI_OUT11		KP_OUT11		KI_OUT8		KP_OUT8		KI_OUT7		KP_OUT7		KI_OUT6		KP_OUT6		KI_OUT5		KP_OUT5	
35H	R/W	Not used	Not used	Not used	Not used	Not used	Start/busy2	R = BIST2R W = BIST2C								Not used	Start/busy1	R = BIST1R W = BIST1C							

7 Package informations

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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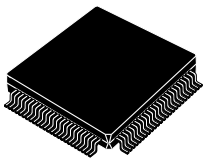
Figure 17. TQFP100 mechanical data and package dimensions

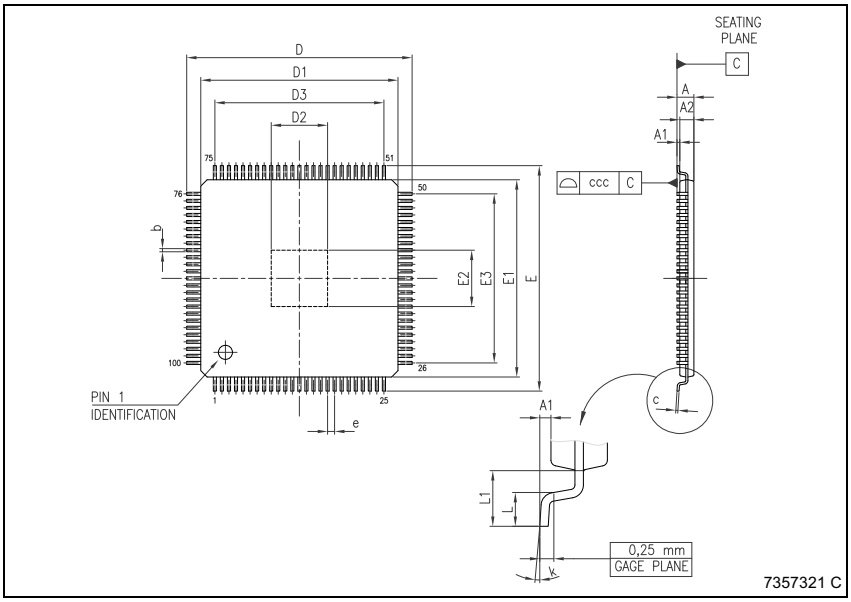
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.200			0.0472
A1	0.050		0.150	0.0020		0.0059
A2	0.950	1.000	1.050	0.0374	0.0394	0.0413
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D2(1)	2.000			0.0787		
D3		12.000			0.4724	
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E2(1)	2.000			0.0787		
E3		12.000			0.4724	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k		3.500	7.000		0.1378	0.2756
ccc			0.080			0.0031

(1) The size of exposed pad is variable depending of leadframe design pad size. End user should verify “D2” and “E2” dimensions for each device application.

OUTLINE AND MECHANICAL DATA



TQFP100 (14x14x1.40mm)
Exposed pad down



GAPGPS2200

8 Revision history

Table 56. Document revision history

Date	Revision	Changes
05-Jun-2013	1	Initial release.
27-Sep-2013	2	Updated disclaimer.

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