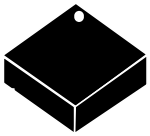
LSM330

iNEMO inertial module: 3D accelerometer and 3D gyroscope

Datasheet - production data



LGA-24L (3x3.5x1 mm)

Features

- Analog supply voltage: 2.4 V to 3.6 V
- Digital supply voltage IOs: 1.8 V
- Power-down and sleep modes
- 2 embedded programmable state machines
- 3 independent acceleration channels and 3 angular rate channels
- ±2/±4/±6/±8/±16 *g* selectable full scale
- ±250/±500/±2000 dps selectable full scale
- SPI/I^2C serial interface
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK® RoHS and “Green” compliant

Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion-activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM330 is a system-in-package featuring a 3D digital accelerometer with two embedded state machines that can be programmed to implement autonomous applications and a 3D digital gyroscope.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330 has a user-selectable full-scale acceleration range of ±2/±4/±6/±8/±16 *g* and an angular rate range of ±250/±500/±2000 dps. The accelerometer and gyroscope sensors can be either activated or separately put in power-down / sleep mode for applications optimized for power saving.

The LSM330 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM330	-40 to +85	LGA-24L (3x3.5x1mm)	Tray
LSM330TR	-40 to +85		Tape and reel

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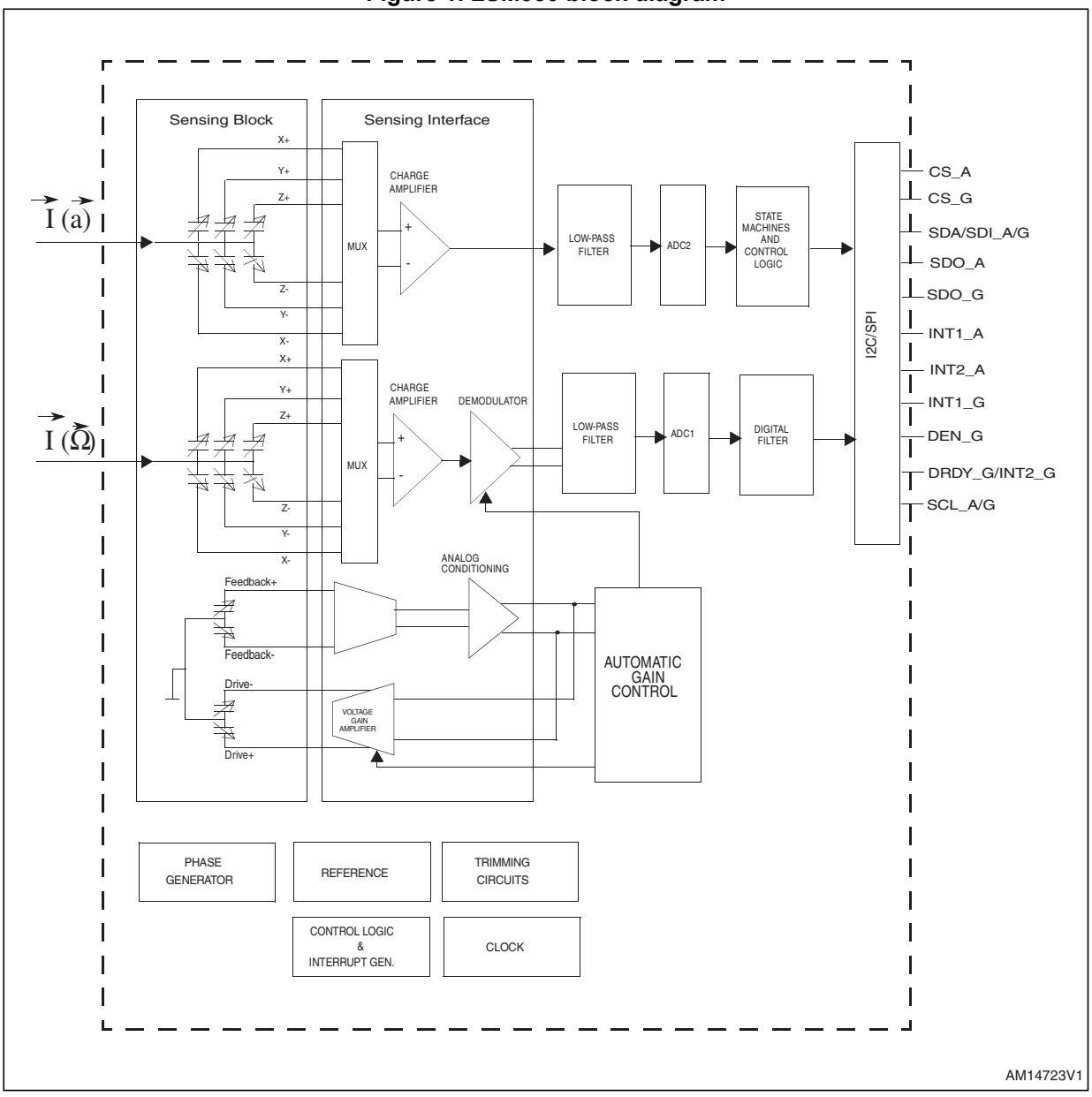
1.1 Block diagram

Figure 1. LSM330 block diagram



1.2 Pin description

Figure 2. Pin connections

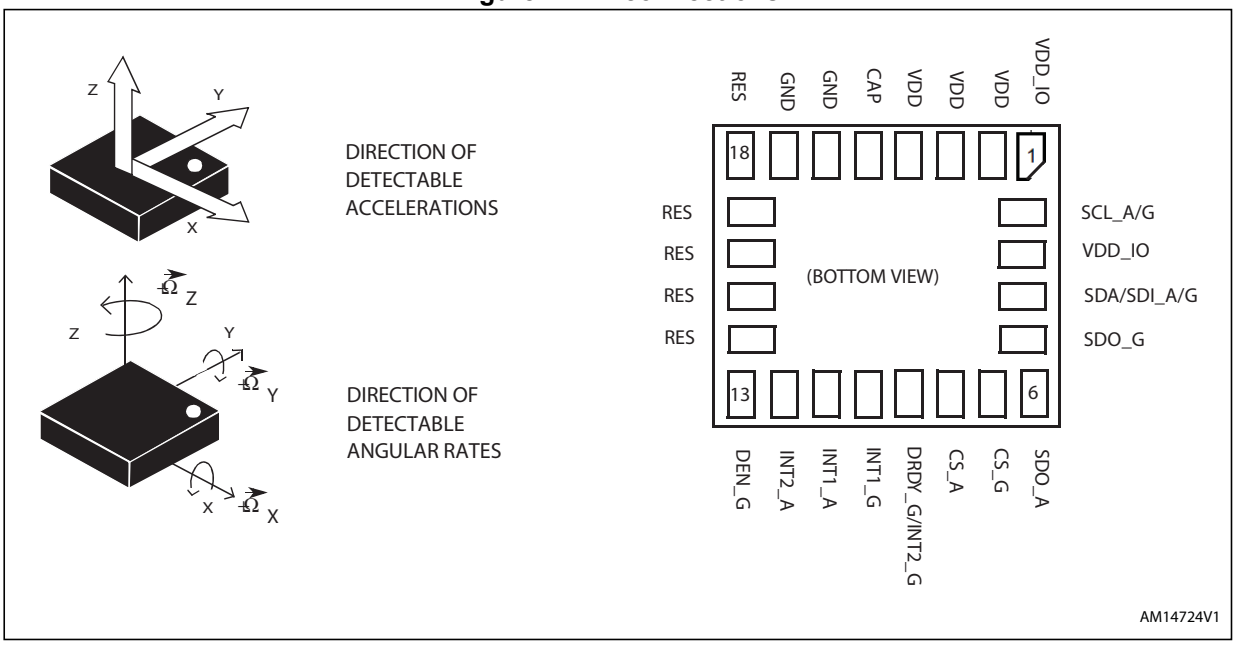


Table 2. Pin description

Pin #	Name	Function
1	Vdd_IO(1)	Power supply for IO pins
2	SCL_A/G	I^2C serial clock (SCL)/SPI serial port clock (SPC)
3	Vdd_IO(1)	Power supply for IO pins
4	SDA/SDI_A/G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SDO_G	Gyroscope: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
6	SDO_A	Accelerometer: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
7	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
8	CS_A	Accelerometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	DRDY_G/ INT2_G	Gyroscope Data Ready/FIFO Interrupt (Watermark/Overrun/Empty)

Table 2. Pin description (continued)

Pin #	Name	Function
10	INT1_G	Gyroscope interrupt signal
11	INT1_A	Accelerometer interrupt1 signal
12	INT2_A	Accelerometer interrupt2 signal
13	DEN_G	Gyroscope Data Enable
14	Res	Reserved. Connect to GND
15	Res	Reserved. Connect to GND
16	Res	Reserved. Connect to GND
17	Res	Reserved. Connect to GND
18	Res	Reserved. Connect to GND
19	GND	0 V supply
20	GND	0 V supply
21	CAP	Connect to GND with ceramic capacitor(2)
22	Vdd(3)	Power supply
23	Vdd(3)	Power supply
24	Vdd(3)	Power supply

1. 100 nF filter capacitor recommended.
2. 10 nF (+/- 10%), 25 V. 1nF minimum value has to be guaranteed under 11 V bias condition1.
3. 100 nF plus 10 µF capacitors recommended.

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		
		FS bit set to 010		±6.0		
		FS bit set to 011		±8.0		
		FS bit set to 100		±16.0		
G_FS	Angular rate measurement range(3)	FS bit set to 00		±250		dps
		FS bit set to 01		±500		
		FS bit set to 10		±2000		
LA_So	Linear acceleration sensitivity	FS bit set to 000		0.061		mg/digit
		FS bit set to 001		0.122		
		FS bit set to 010		0.183		
		FS bit set to 011		0.244		
		FS bit set to 100		0.732		
G_So	Angular rate sensitivity	FS = ±250 dps		8.75		mdps/ digit
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy(3)	FS bit set to 000		±60		m*g*
G_TyOff	Angular rate typical zero-rate level(4)	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd+0.1	V
LA_Idd	Accelerometer current consumption in normal mode	1.6 kHz ODR		250		µA
		3.125 Hz ODR		10		
LA_IddPdn	Accelerometer current consumption in power-down mode			1		µA
G_Idd	Gyroscope current consumption in Normal mode			6.1		mA
G_IddLowP	Gyroscope supply current in sleep mode(2)			2		mA
G_IddPdn	Gyroscope current consumption in power-down mode			5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

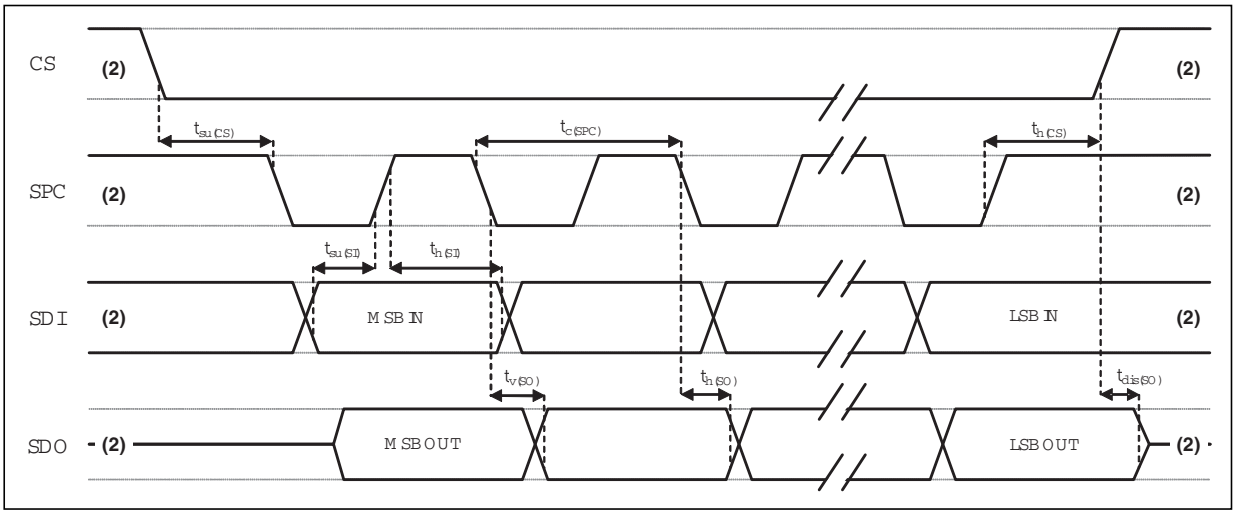
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter(1)	Value(2)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.
2. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results. Not tested in production.

Figure 3. SPI slave timing diagram



2. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

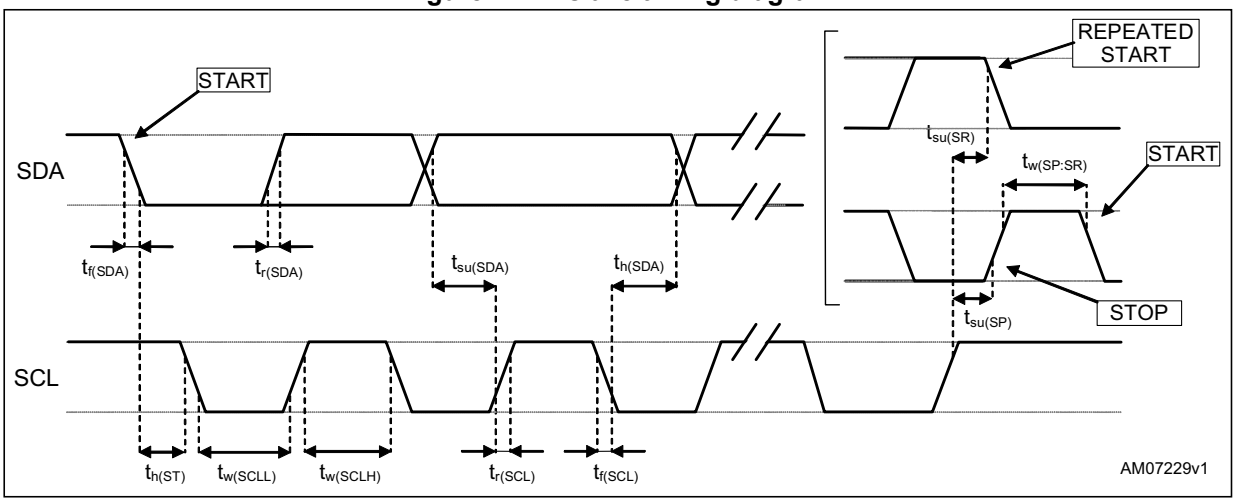
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter(1)	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20 + 0.1C_b (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. SCL (SCL_A/G pin), SDA (SDA_A/G pin).
2. C_b = total capacitance of one bus line, in pF

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings(1)

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL_A/G, SDA_A/G, SDO_A, SDO_G, CS_A, CS_G, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

1. Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

Linear acceleration sensitivity can be determined by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

Angular rate sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to the device. This value changes very little over temperature and also very little overtime.

3.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and over time.

4 Functionality

The LSM330 is a system-in-package featuring a 3D digital accelerometer with two embedded state machines and a 3D digital gyroscope, together with two FIFO memory blocks available to manage linear acceleration and angular rate data.

The device includes specific sensing elements and two IC interfaces capable of measuring both the acceleration and angular rate applied to the module and providing a signal to external applications through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

4.1 Power modes

The linear acceleration sensor and the angular rate sensor can be either activated or separately set in power-down/ sleep mode for applications optimized for power saving.

The acceleration sensor operating modes can be selected between normal or power-down through *CTRL_REG5_A (20h)*. The angular rate sensor operating mode can be selected among normal power-down or sleep mode, through *CTRL_REG1_G (20h)*.

4.2 Linear acceleration sensor digital main blocks

4.2.1 State machine

The LSM330 embeds two state machines able to run a user-defined program.

The program is composed of a set of instructions that defines the transition to successive states. Conditional branches are possible.

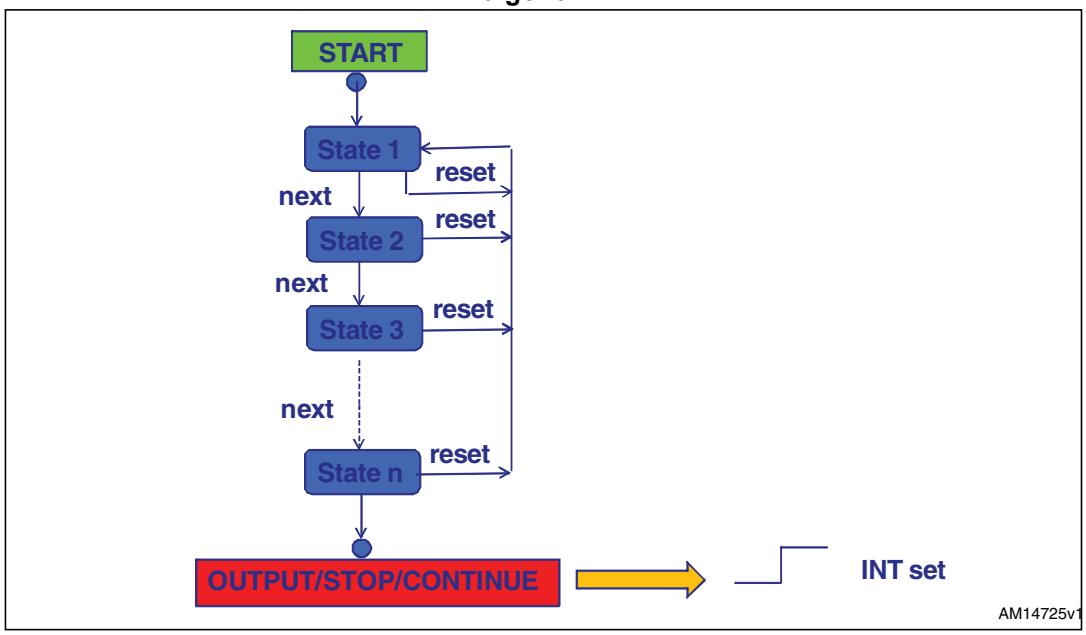
From each state (n) it is possible to have a transition to the next state (n+1) or to a reset state. The transition to the reset point happens when the “RESET condition” is true. The transition to the next step happens when the “NEXT condition” is true.

An interrupt is triggered when the Output/Stop/Continue state is reached.

Each State machine allows implementing, in a flexible way, gesture recognition, free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double-click, shake/double-shake, face-up/face-down, turn/double-turn:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Figure 5. LSM330 accelerometer state machines: sequence of state to execute an algorithm



4.2.2 FIFO

LSM330 embeds 32 slots of FIFO data for each of the three acceleration output channels X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. In order to use FIFO it is necessary to enable the FIFO_EN bit in the *CTRL_REG7_A (25h)* register.

The FIFO buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode and Bypass-to-Stream mode. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL_REG_A (2Eh)* register. Programmable watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT1_A/INT2_A pin (configured through the INT2_EN and INT1_EN bits in the *CTRL_REG4_A (23h)* register).

When FIFO is empty, the EMPTY bit in *FIFO_SRC_REG_A (2Fh)* is equal to '1' and no samples are available.

If the application requires a lower number of samples, a programmable watermark level can be set. In *FIFO_SRC_REG_A (2Fh)* the WTM bit is high if new data arrives and the FSS [4:0] bit in *FIFO_SRC_REG_A (2Fh)* is greater than or equal to the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register. In *FIFO_SRC_REG_A (2Fh)* the WTM bit goes to '0' if reading X, Y, Z data slot from FIFO and the FSS [4:0] bit in *FIFO_SRC_REG_A (2Fh)* is less than or equal to the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register.

When FIFO is completely full, the OVRN_FIFO bit in the *FIFO_SRC_REG_A (2Fh)* is equal to '1' and the FIFO slot is overwritten.

4.2.3 Bypass mode

In Bypass mode, the FIFO is not operational and it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (i.e. FIFO mode).

4.2.4 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (set of 32 samples stored). When the FIFO is full it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, P1_OVERRUN = '1' in the *CTRL_REG7_A (25h)* register, in order to be raised when the FIFO stops collecting data. When overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

At the end of the reads it is necessary to transition from Bypass mode to reset FIFO content. After this reset command it is possible to restart FIFO mode by writing '001' to FMODE [2:0] in the *FIFO_CTRL_REG_A (2Eh)* register.

The FIFO buffer can memorize 32 levels of X, Y and Z data, but the depth of the FIFO can be reduced by a programmable watermark. In order to enable a FIFO watermark, the WTM_EN bit in *CTRL_REG7_A (25h)* is high and the FIFO depth is set by the WTMP [4:0] bits in the *FIFO_CTRL_REG_A (2Eh)* register. The watermark interrupt can be enabled on the INT1_A pad if the P1_WTM bit in the *CTRL_REG7_A (25h)* register is enabled.

4.2.5 Stream mode

In Stream mode FIFO continues filling data from the X, Y, and Z accelerometer channels. When the buffer is full (set of 32 samples stored) the FIFO buffer index restarts from the beginning and older data is replaced by the current. The oldest values continue to be overwritten until a read operation makes free FIFO slots available.

An overrun interrupt can be enabled, P1_OVERRUN = '1' in the *CTRL_REG7_A (25h)* register, in order to read the entire FIFO content at once. If in the application it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data.

Setting the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading (see *FIFO_SRC_REG_A (2Fh)*).

At the end of the reads it is necessary to transition from Bypass mode to reset FIFO content.

4.2.6 Stream-to-FIFO mode

In Stream-to-FIFO mode FIFO behavior changes according to an interrupt generated by the configuration of the two state machines using the INT_SM1 and INT_SM2 bits in the *STAT (18h)* register.

When the INT_SM1, INT_SM2 bits in the *STAT (18h)* register are equal to '1', FIFO operates in FIFO mode. When the INT_SM1, INT_SM2 bits in the *STAT (18h)* register are equal to '0', FIFO operates in Stream mode.

4.2.7 Bypass-to-Stream mode

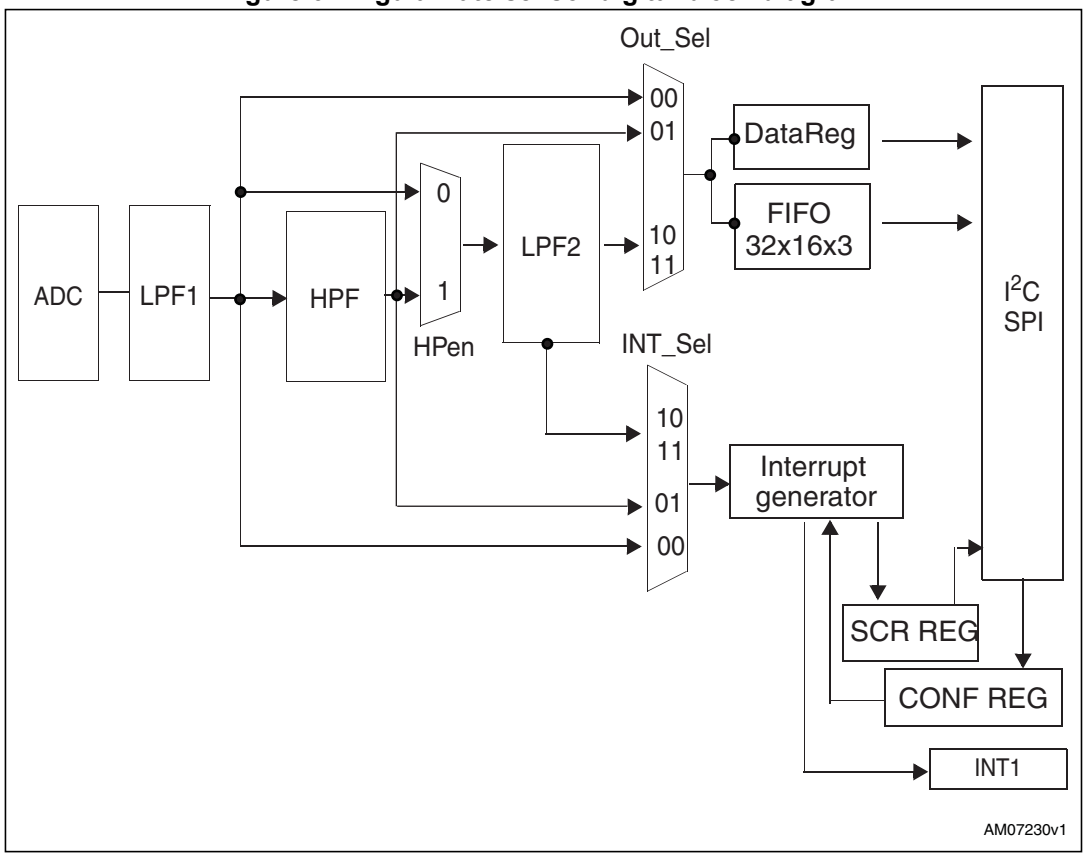
In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (*STAT (18h)*, the FIFO starts operating in Stream mode.

4.2.8 Retrieving data from FIFO

FIFO data is read from *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)*. When the FIFO is in Stream, Stream-to-FIFO mode or FIFO mode, a read operation from the *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* or *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.3 Angular rate sensor digital main blocks

Figure 6. Angular rate sensor digital block diagram



4.3.1 FIFO

The LSM330 embeds 32 slots of 16 bit data FIFO buffer for each of the three output channels, yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

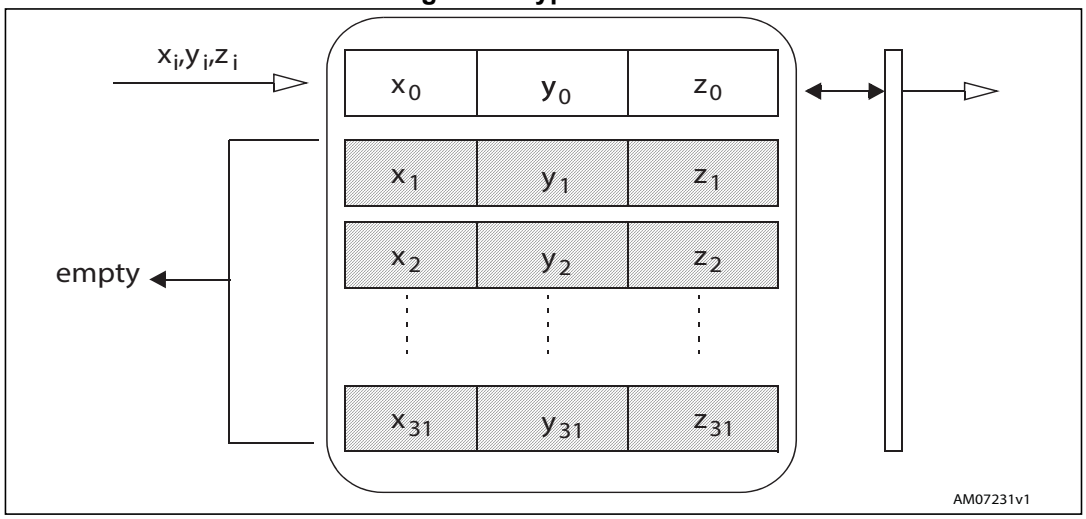
In order to use FIFO it is necessary to enable the FIFO_EN bit in the *CTRL_REG5_G (24h)* register. The FIFO buffer can work accordingly to five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM[2:0] bits in the *FIFO_CTRL_REG_G (2Eh)* register.

Programmable watermark level, FIFO empty or FIFO full events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configuration through *CTRL_REG3_G (22h)*) and event detection information is available from *FIFO_SRC_REG_G (2Fh)*. The watermark level can be configured by the WTM[4:0] bits in *FIFO_CTRL_REG_G (2Eh)*.

4.3.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in the next figure, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available the previous data is overwritten.

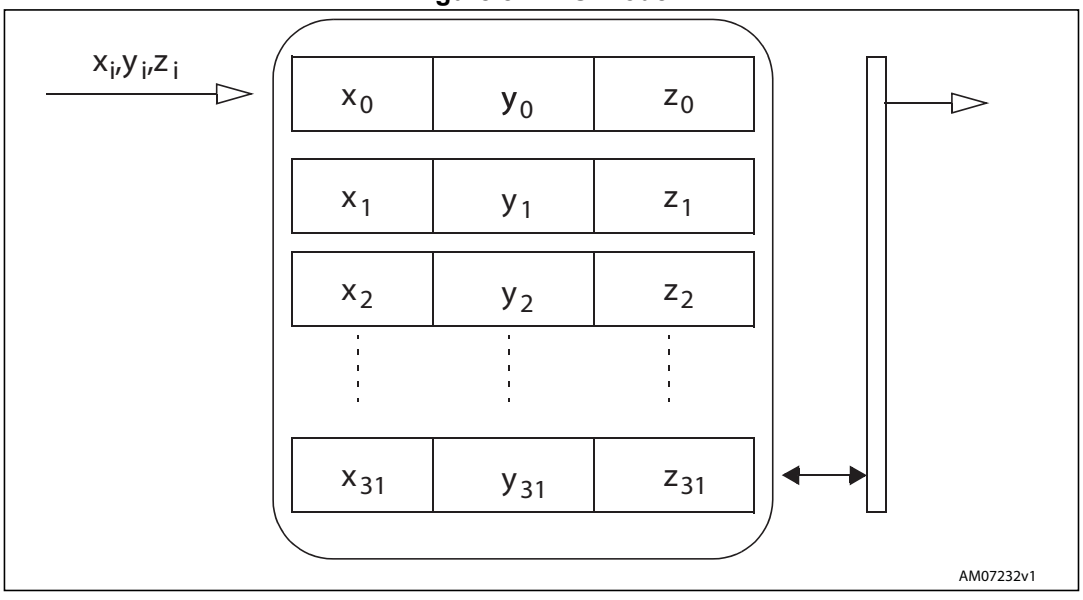
Figure 7. Bypass mode



4.3.3 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels are stored in the FIFO. A watermark interrupt can be enabled (I2_WTM bit in *CTRL_REG3_G (22h)*) in order to be raised when the FIFO is filled to the level specified by the WTM[4:0] bits of the *FIFO_CTRL_REG_G (2Eh)* register. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart collecting data *FIFO_CTRL_REG_G (2Eh)* must be written back to Bypass mode. FIFO mode is represented in the following figure.

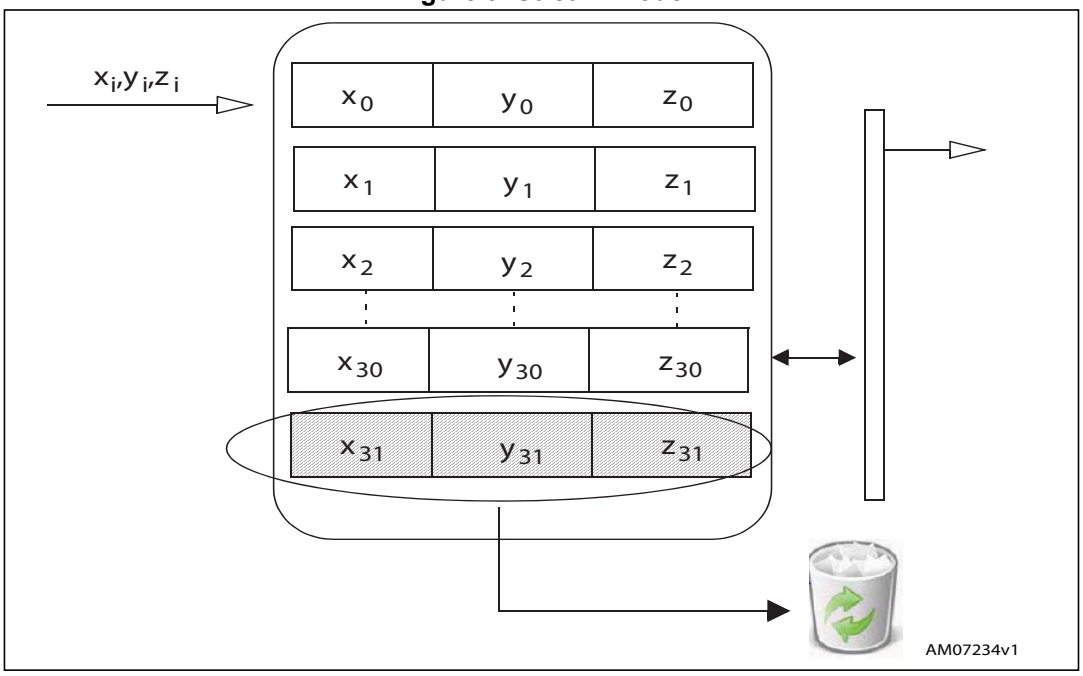
Figure 8. FIFO mode



4.3.4 Stream mode

In Stream mode, data from yaw, pitch and roll measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode. FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new arrive. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configuration through *CTRL_REG3_G (22h)*). Stream mode is represented in the following figure.

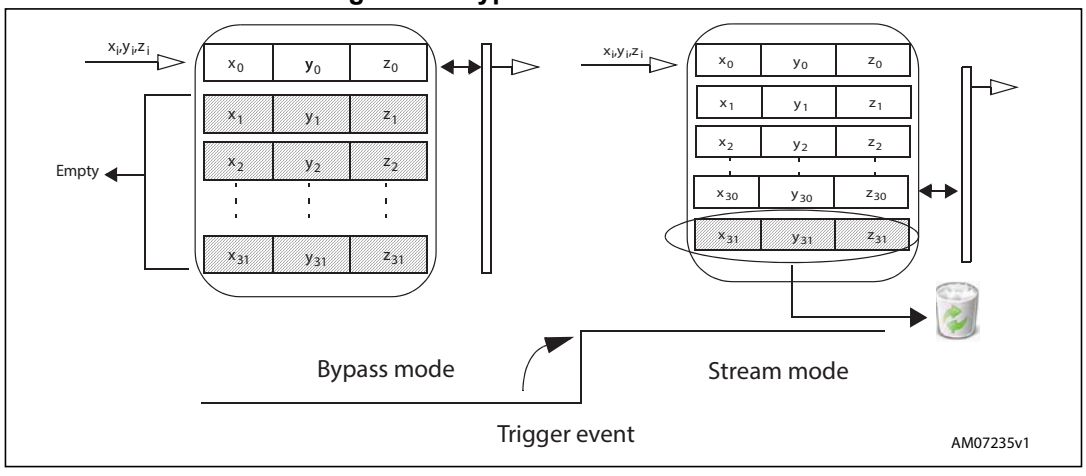
Figure 9. Stream mode



4.3.5 Bypass-to-Stream mode

In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to the *INT1_CFG_G (30h)* register events) the FIFO starts operating in Stream mode. Refer to the following figure.

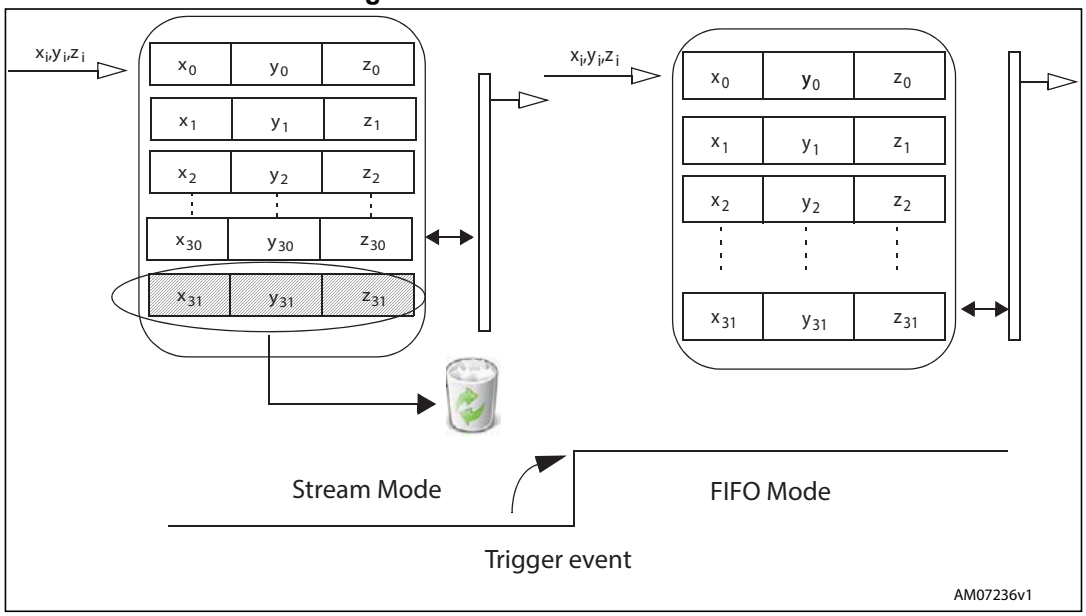
Figure 10. Bypass-to-stream mode



4.3.6 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurements are stored in the FIFO. A watermark interrupt can be enabled on the pin DRDY_G/INT2_G, setting the I2_WTM bit in *CTRL_REG3_G (22h)* in order to be raised when the FIFO is filled to the level specified by the WTM [4:0] bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it's full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrive. Once a trigger event occurs (related to *INT1_CFG_G (30h)* register events), the FIFO starts operating in FIFO mode. Refer to the following figure.

Figure 11. Stream-to-FIFO mode



4.3.7 Retrieving data from FIFO

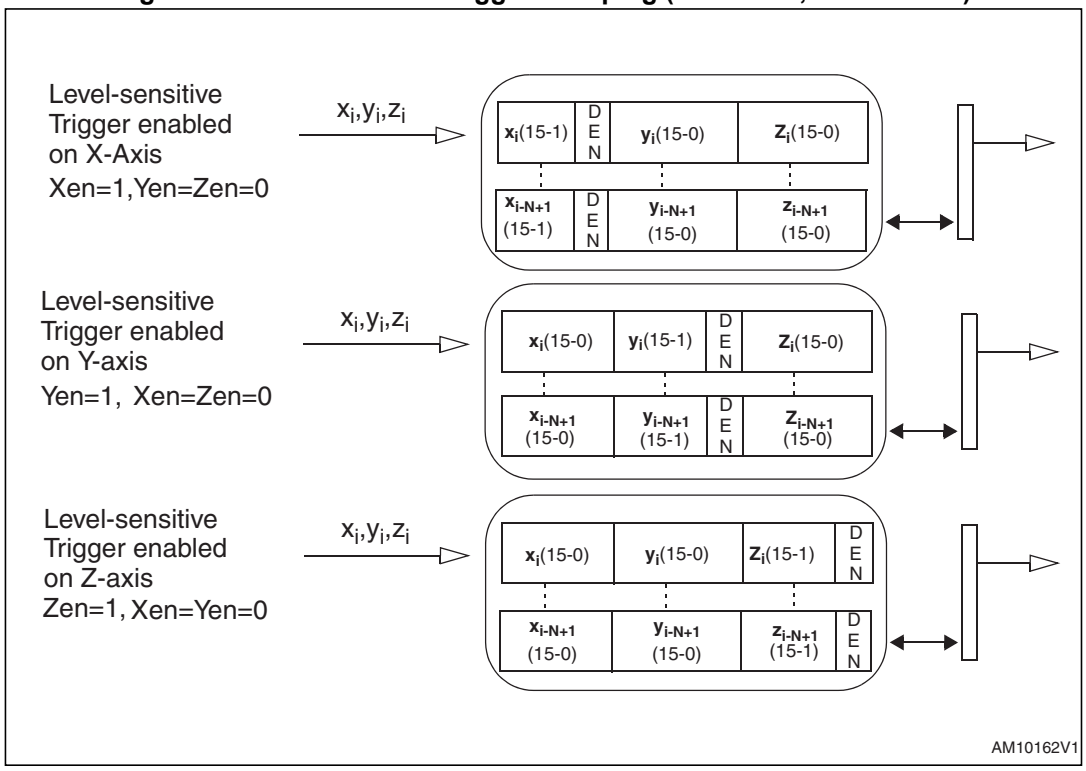
FIFO data is read from *OUT_X_L_G (28h), OUT_X_H_G (29h)* and *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)*. When the FIFO is in Stream, Stream-to-FIFO or FIFO mode, a read from the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers provides the data stored in the FIFO.

Each time data is read from the FIFO, the oldest pitch, roll and yaw data are placed in the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers and both single read and read_burst (X, Y and Z with autoincremental address) operations can be used. When data included in OUT_Z_H_G (2Dh) is read, the system restarts to read information from OUT_X_L_G (28h).

4.3.8 Level-sensitive / edge-sensitive data enable

The LSM330 allows external trigger level recognition through the enabling of the EXTRen and LVLen bits in the *CTRL_REG2_G register*. Two different modes can be used: level-sensitive or edge-sensitive trigger.

Figure 12. Level-sensitive trigger stamping (LVLen = 1; EXTRen = 0)



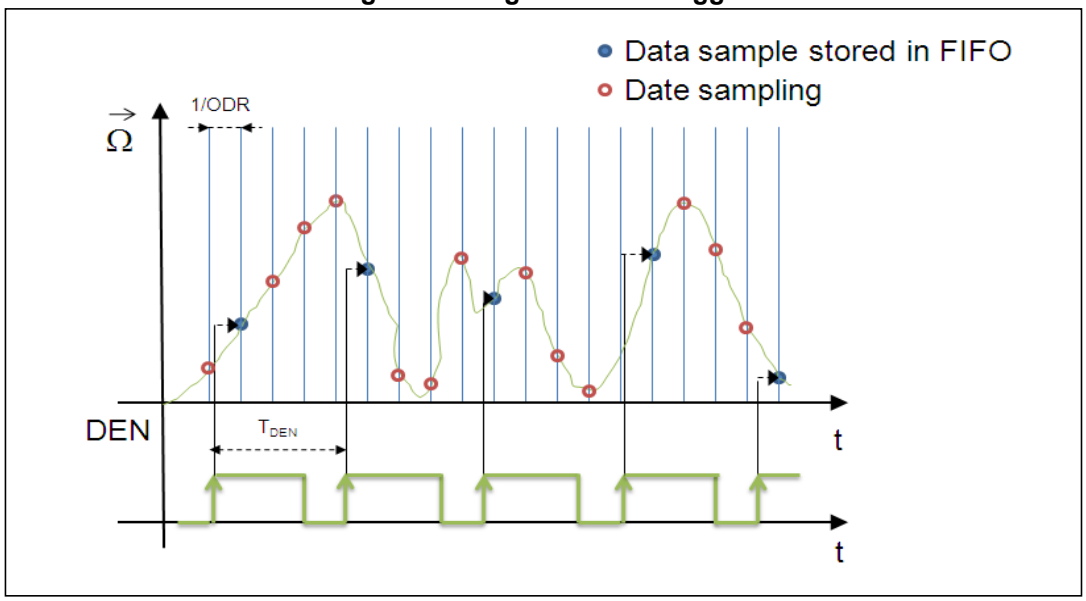
4.3.9 Level-sensitive trigger stamping

Once enabled, the DEN level replaces the LSb of the X, Y or Z axes, configurable through the Xen, Yen, Zen bits in the *CTRL_REG1_G register*. Data is stored in the FIFO with the internally-selected ODR.

4.3.10 Edge-sensitive trigger

Once enabled by setting EXTRen = 1, FIFO is filled with the pitch, roll and yaw data on the rising edge of the DEN input signal. When selected ODR is 800 Hz, the maximum DEN sample frequency is $f_{DEN} = 1/T_{DEN} = 400$ Hz.

Figure 13. Edge-sensitive trigger

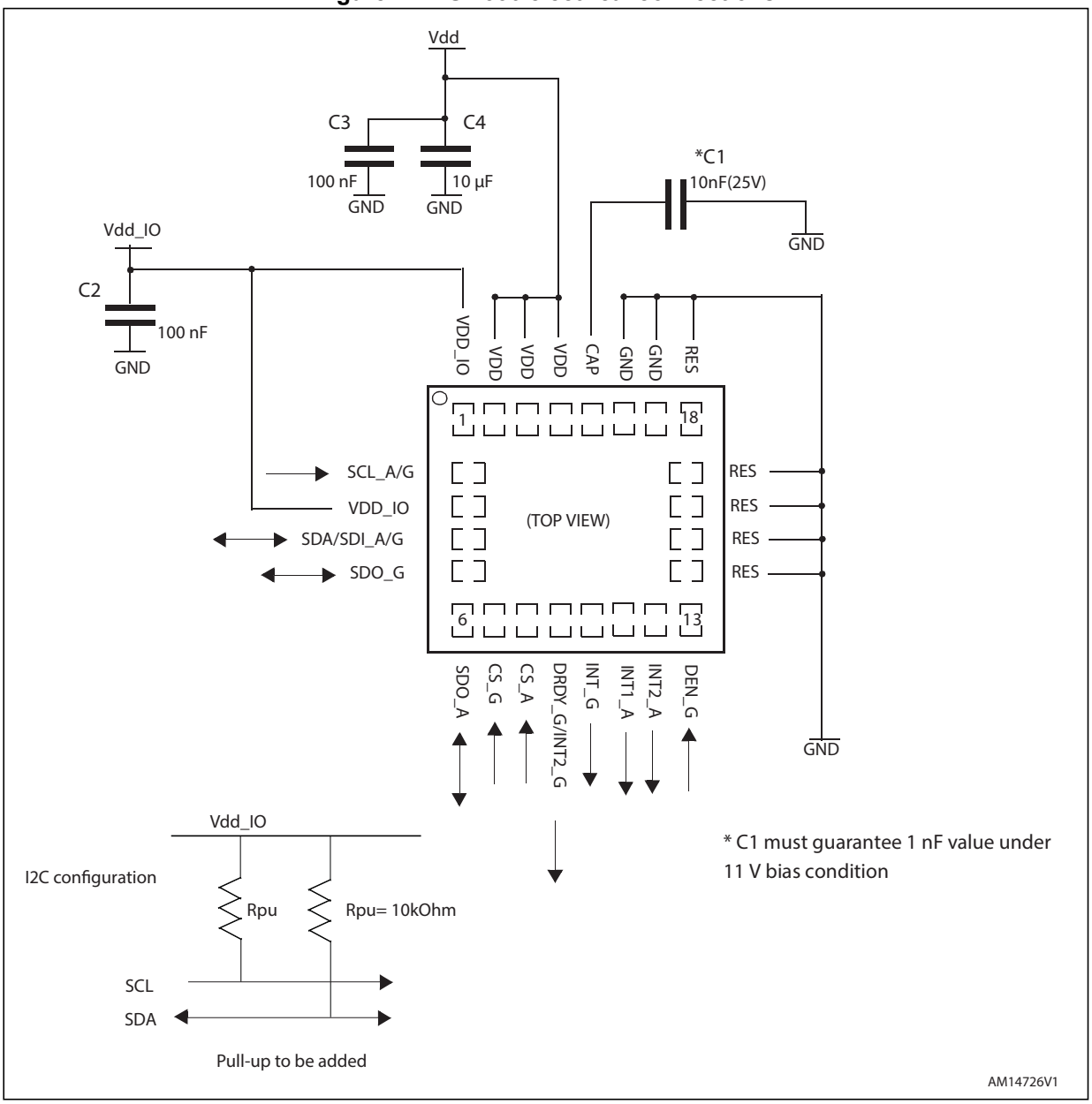


4.4 Factory calibration

The IC interface is factory calibrated for sensitivity and zero level. The trim values are stored in the device in nonvolatile memory. Any time the device is turned on, the trim parameters are downloaded to the registers to be used during normal operation. This allows use of the device without further calibration.

5 Application hints

Figure 14. LSM330 electrical connections



5.1 External capacitors

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C2, C3=100 *nF* ceramic, C4=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice).

All voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to *Figure 14*).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I^2C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I^2C interface.

5.2 Soldering information

The LGA package is compliant with ECOPACK®, RoHS and “Green” standards. It is qualified for soldering heat resistance according to JEDEC J-STD-020D.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

6 Digital interfaces

The registers embedded in the LSM330 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS_A	Linear acceleration SPI enable Linear acceleration I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
CS_G	Angular rate SPI enable Angular rate I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL_A/G	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA_A/G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO_A SDO_G	I^2C least significant bit of the device address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LSM330 I^2C is a bus slave. The I^2C is employed to write the data to the registers, whose content can also be read back.

The relevant I^2C terminology is provided in the table below.

Table 10. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits, and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM330 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST), a slave address is sent. Once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/write.

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by

the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pins (SDO_A / SDO_G) can be used to modify the least significant bits of the device address.The linear acceleration sensor slave address is 00111xxb whereas the xx bits are modified by the SDO_A pin. If the SDO/A pin is connected to the supply voltage, the address is 0011101b, otherwise if the SDO/A pin is connected to ground, the address is 0011110b.This solution allows to connect and address two different accelerometers to the same I^2C line.

The angular rate sensor slave address is 110101xb, whereas the x bit is modified by the SDO/G bit. If the SDO_G pin is connected to the supply voltage, LSb is ‘1’ (address 1101011b), otherwise, if the SDO_G pin is connected to ground, the LSb value is ‘0’ (address 1101010b).

The slave addresses are completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes. If the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 15* and *Table 16* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration sensor: the default (factory) 7-bit slave address is 00111xxb.

Table 15. Linear acceleration SAD+Read/Write patterns

Command	SAD[6:2]	SAD[1] = $\overline{\text{SDO\_A}}$	SAD[0] = SDO_A	R/W	SAD+R/W
Read	00111	1	0	1	00111101 (3Dh)
Write	00111	1	0	0	00111100 (3Ch)
Read	00111	0	1	1	00111011 (3Bh)
Write	00111	0	1	0	00111010 (3Ah)

Angular rate sensor: the default (factory) 7-bit slave address is 110101xb.

Table 16. Angular rate SAD+Read/Write patterns

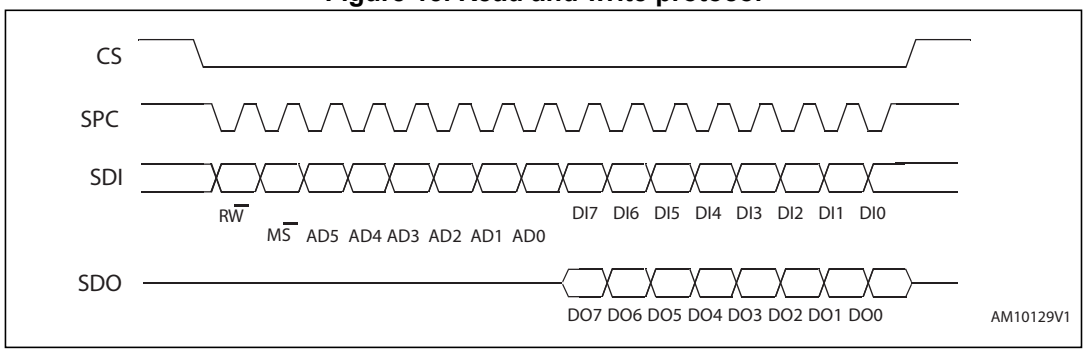
Command	SAD[6:1]	SAD[0] = SDO_G	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

6.2 SPI bus interface

The LSM330 SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the external world through 4 wires: **CS(CS_A,CS_G)**, **SPC**, **SDI** and **SDO (SDO_A,SDO_G);** (SPC, SDI are common).

Figure 15. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes low at the start of the transmission and returns high at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple-byte read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS**, while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that will be written to the device (MSb first).

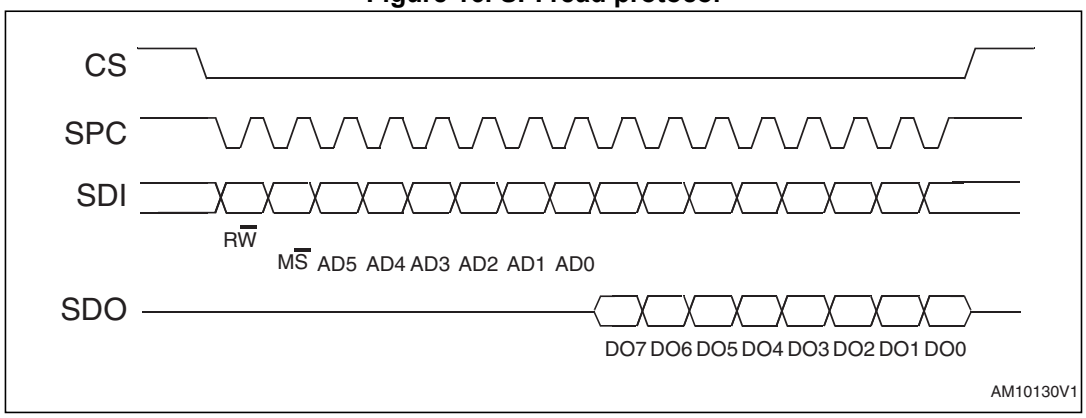
bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is ‘0’, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is ‘1’, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 16. SPI read protocol



Note: Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

The SPI read command is performed with 16 clock pulses. A multiple-byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

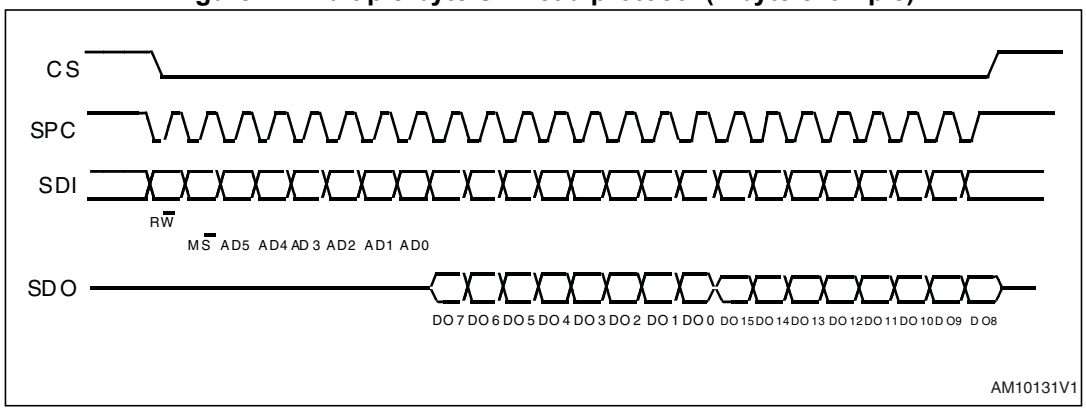
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

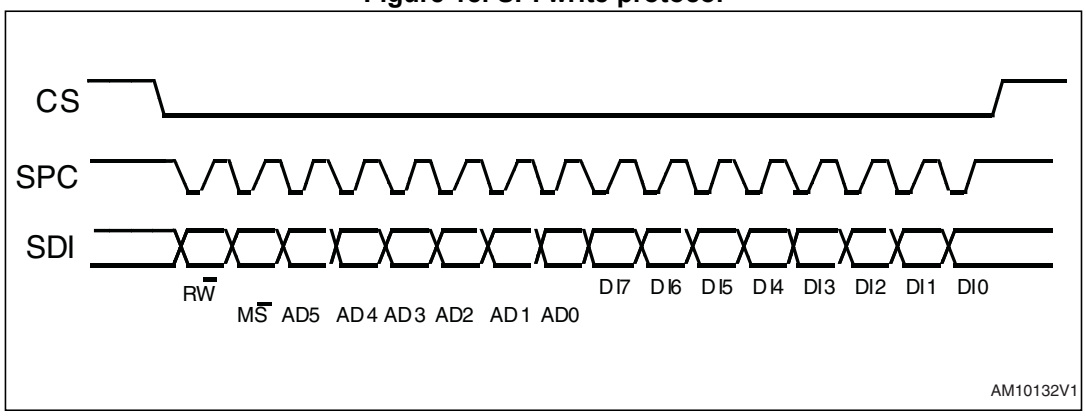
bit 16-... : data DO(...-8). Further data in multiple-byte reads.

Figure 17. Multiple-byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 18. SPI write protocol



Note: Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

The SPI write command is performed with 16 clock pulses. A multiple-byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

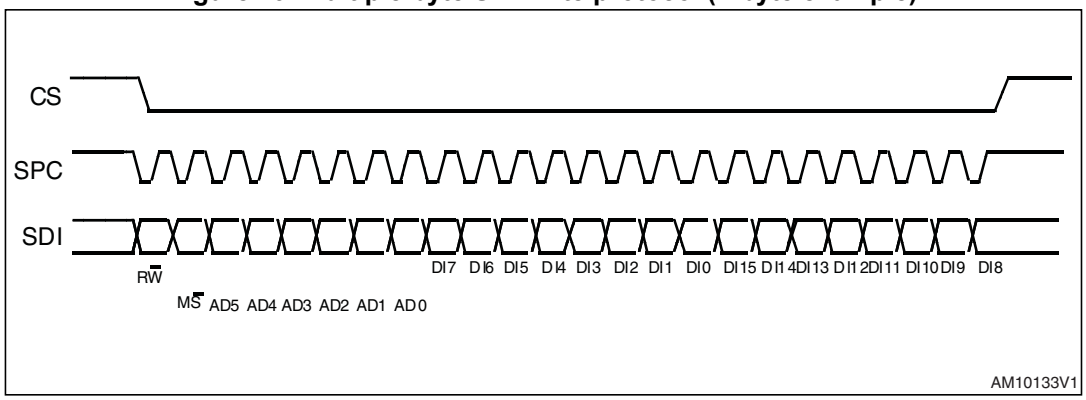
bit 1: M$\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that will be written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple-byte writes.

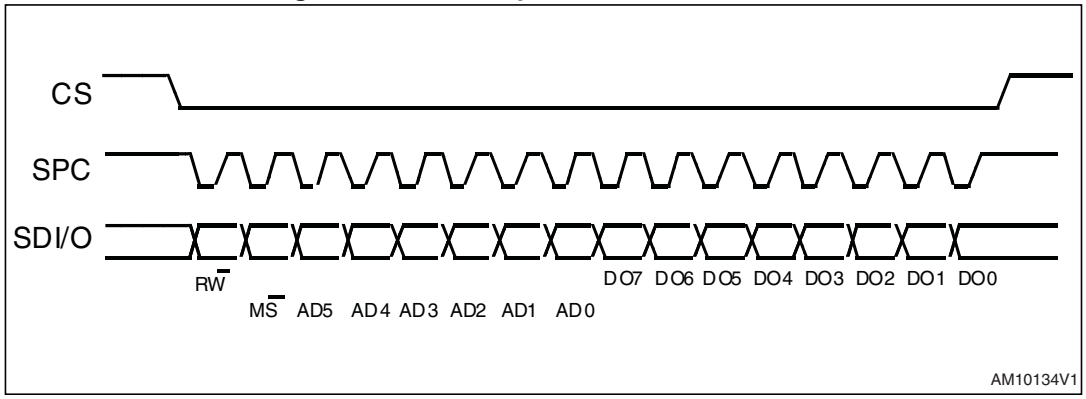
Figure 19. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM bits to '1' (SPI serial interface mode selection) in the *CTRL_REG6_A (24h)* and *CTRL_REG4_G (23h)*.

Figure 20. SPI read protocol in 3-wire mode



Note: Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that will be read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

7 Register mapping

The table below provides a list of the 8/16-bit registers embedded in the device, and their corresponding addresses.

Table 17. Register address map

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
WHO_AM_I_A	*Table 14*	r	0F	000 1111	01000000	Who am I linear acceleration sensor register
CTRL_REG4_A	*Table 14*	r/w	23	010 0011	00000000	Linear acceleration sensor control registers
CTRL_REG5_A	*Table 14*	r/w	20	010 0000	00000111	
CTRL_REG6_A	*Table 14*	r/w	24	010 0100	00000000	
CTRL_REG7_A	*Table 14*	r/w	25	010 0101	00000000	
STATUS_REG_A	*Table 14*	r	27	010 0111	output	Status register
OFF_X	*Table 14*	r/w	10	001 0000	output	Axis offset correction
OFF_Y	*Table 14*	r/w	11	001 0001	output	
OFF_Z	*Table 14*	r/w	12	001 0010	output	
CS_X	*Table 14*	r/w	13	001 0011	00000001	Constant shift registers
CS_Y	*Table 14*	r/w	14	001 0100	00000001	
CS_Z	*Table 14*	r/w	15	001 0101	00000001	
LC_L	*Table 14*	r/w	16	001 0110	00000001	Long counter registers
LC_H	*Table 14*	r/w	17	001 0111	00000000	
STAT	*Table 14*	r	18	001 1000	output	Interrupt sync
VFC_1	*Table 14*	r/w	1B	001 1011	00000000	Vector filter coefficient
VFC_2	*Table 14*	r/w	1C	001 1100	00000000	
VFC_3	*Table 14*	r/w	1D	001 1101	00000000	
VFC_4	*Table 14*	r/w	1E	001 1110	00000000	
THRS3	*Table 14*	r/w	1F	001 1111	00000000	Threshold value 3

Table 17. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
OUT_X_L_A	Table 14	r	28	010 1000	output	Linear acceleration sensor output registers
OUT_X_H_A	Table 14	r	29	010 1001	output	
OUT_Y_L_A	Table 14	r	2A	010 1010	output	
OUT_Y_H_A	Table 14	r	2B	010 1011	output	
OUT_Z_L_A	Table 14	r	2C	010 1100	output	
OUT_Z_H_A	Table 14	r	2D	010 1101	output	
FIFO_CTRL_REG_A	Table 14	r/w	2E	010 1110	00000000	Linear acceleration sensor FIFO registers
FIFO_SRC_REG_A	Table 14	r	2F	010 1111	output	
CTRL_REG2_A	Table 14	r/w	21	010 0001	00000000	SM1 control register
STx_1	Table 14	r/w	40-4F	100 0000 100 1111	00000000	SM1 code register (X=1-16)
TIM4_1	Table 14	r/w	50	101 0000	00000000	SM1 general timers
TIM3_1	Table 14	r/w	51	101 0001	00000000	
TIM2_1	Table 14	r/w	52-53	101 0010 101 0011	00000000	
TIM1_1	Table 14	r/w	54-55	101 0100 101 0101	00000000	
THRS2_1	Table 14	r/w	56	101 0110	00000000	SM1 threshold value 1
THRS1_1	Table 14	r/w	57	101 0111	00000000	SM1 threshold value 2
MASKB_1	Table 14	r/w	59	101 1001	00000000	SM1 axis and sign mask
MASKA_1	Table 14	r/w	5A	101 1010	00000000	
SETT1	Table 14	r/w	5B	101 1011	00000000	SM1 detection settings
PR1	Table 14	r/w	5C	101 1100	00000000	Program-reset pointer
TC1	Table 14	r	5D-5E	101 1101 101 1110	00000000	Timer counter
OUTS1	Table 14	r	5F	101 1111	00000000	Main set flag
PEAK1	Table 14	r	19	001 1001	00000000	Peak value
CTRL_REG3_A	Table 14	r/w	22	010 0010	00000000	SM2 control register

Table 17. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
STx_2	Table 14	r/w	60-6F	110 0000 110 1111	00000000	SM2 code register (X=1-16)
TIM4_2	Table 14	r/w	70	111 0000	00000000	SM2 general timers
TIM3_2	Table 14	r/w	71	111 0001	00000000	
TIM2_2	Table 14	r/w	72-73	111 0010 111 0011	00000000	
TIM1_2	Table 14	r/w	74-75	111 0100 111 0101	00000000	
THRS2_2	Table 14	r/w	76	111 0110	00000000	SM2 threshold value 1
THRS1_2	Table 14	r/w	77	111 0111	00000000	SM2 threshold value 2
MASKB_2	Table 14	r/w	79	111 1001	00000000	SM2 axis and sign mask
MASKA_2	Table 14	r/w	7A	111 1010	00000000	
SETT2	Table 14	r/w	7B	111 1011	00000000	SM2 detection settings
PR2	Table 14	r/w	7C	111 1100	00000000	Program-reset pointer
TC2	Table 14	r	7D-7E	111 1101 111 1110	00000000	Timer counter
OUTS2	Table 14	r	7F	111 1111	00000000	Main set flag
PEAK2	Table 14	r	1A	001 1010	00000000	Peak value
DES2	Table 14	w	78	111 1000	00000000	Decimation factor
WHO_AM_I_G	Table 15	r	0F	000 1111	11010100	Who I am ID
Reserved	-	-	10-1F	-	-	-
CTRL_REG1_G	Table 15	r/w	20	010 0000	00000111	Angular rate sensor control registers
CTRL_REG2_G	Table 15	r/w	21	010 0001	00000000	
CTRL_REG3_G	Table 15	r/w	22	010 0010	00000000	
CTRL_REG4_G	Table 15	r/w	23	010 0011	00000000	
CTRL_REG5_G	Table 15	r/w	24	010 0100	00000000	
REFERENCE_G	Table 15	r/w	25	010 0101	00000000	Reference value for interrupt generation

Table 17. Register address map (continued)

Name	Slave address	Type	Register address		Default	Comment
			Hex	Binary		
OUT_TEMP_G	Table 15	r	26	010 0110	output	Temperature data output
STATUS_REG_G	Table 15	r	27	010 0111	output	Status register
OUT_X_L_G	Table 15	r	28	010 1000	output	Angular rate sensor output registers
OUT_X_H_G	Table 15	r	29	010 1001	output	
OUT_Y_L_G	Table 15	r	2A	010 1010	output	
OUT_Y_H_G	Table 15	r	2B	010 1011	output	
OUT_Z_L_G	Table 15	r	2C	010 1100	output	
OUT_Z_H_G	Table 15	r	2D	010 1101	output	
FIFO_CTRL_REG_G	Table 15	r/w	2E	010 1110	00000000	Angular rate sensor FIFO registers
FIFO_SRC_REG_G	Table 15	r	2F	010 1111	output	
INT1_CFG_G	Table 15	r/w	30	011 0000	00000000	Angular rate sensor interrupt registers
INT1_SRC_G	Table 15	r/w	31	011 0001	output	
INT1_THS_XH_G	Table 15	r/w	32	011 0010	00000000	
INT1_THS_XL_G	Table 15	r/w	33	011 0011	00000000	
INT1_THS_YH_G	Table 15	r/w	34	011 0100	00000000	
INT1_THS_YL_G	Table 15	r/w	35	011 0101	00000000	
INT1_THS_ZH_G	Table 15	r/w	36	011 0110	00000000	
INT1_THS_ZL_G	Table 15	r/w	37	011 0111	00000000	
INT1_DURATION_G	Table 15	r/w	38	011 1000	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

8.1 WHO_AM_I_A (0Fh)

Who am I linear acceleration sensor register (r)

Table 18. WHO_AM_I_A register default value

0	1	0	0	0	0	0	0

8.2 CTRL_REG4_A (23h)

Linear acceleration sensor control register 4 (r/w)

Table 19. CTRL_REG4_A register

DR_EN	IEA	IEL	INT2_EN	INT1_EN	VFILT	-	STRT

Table 20. CTRL_REG4_A register description

DR_EN	DRDY signal enable on INT1_A. Default value: 0 0 = Data ready signal disabled, 1 = Data ready signal routed to INT1_A
IEA	Interrupt signal polarity. Default value: 0 0 = Interrupt signal active LOW, 1 = Interrupt signal active high
IEL	Interrupt signal latching. Default value: 0 0 = Interrupt signal latched, 1 = Interrupt signal pulsed
INT2_EN	Interrupt 2 enable on INT2_A. Default value: 0 0 = INT2_A signal disabled, 1 = INT2_A signal enable
INT1_EN	Interrupt 1 enable on INT1_A. Default value: 0 0 = INT1_A signal disabled, 1 = INT1_A signal enable
VFILT	Vector filter enable. Default value: 0 0 = Vector filter disabled, 1 = Vector filter enabled
STRT	Soft-reset bit. Default value: 0 0= no soft reset, 1= Soft-reset (POR function)

8.3 CTRL_REG5_A (20h)

Linear acceleration sensor control register 5 (r/w)

Table 21. CTRL_REG5_A register

ODR3	ODR2	ODR1	ODR0	BDU	ZEN	YEN	XEN

Table 22. CTRL_REG5_A register description

ODR [3:0]	Output data rate & power mode selection. Default value:0000 (see *Table 23*)
BDU	Block Data Update. Default value: 0 0:continuous update,1:output registers not updated until MSB and LSB read
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value:1 (0:Y axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value:1 (0: X-axis disabled;1: X-axis enabled)

ODR [3:0] is used to set power mode, ODR selection. The following table lists all frequencies available.

Table 23. CTRL_REG5_A output data rate selection

ODR3	ODR2	ODR1	ODR0	ODR selection
0	0	0	0	Power-down
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	400 Hz
1	0	0	0	800 Hz
1	0	0	1	1600 Hz

The BDU bit is used to inhibit the update of the output registers until both upper and lower registers are read. In default mode (BDU='0') the output register values are updated continuously. If for any reason it is not sure to read faster than the output data rate it is recommended to set the BDU bit to '1'. In this way the content of output register is not updated until both MSB and LSB are read, avoiding to read values related to different sample times.

8.4 CTRL_REG6_A (24h)

Linear acceleration sensor control register 6 (r/w).

Table 24. CTRL_REG6_A register

BW2	BW1	FSCALE2	FSCALE1	FSCALE0	-	-	SIM

Table 25. CTRL_REG6_A register description

BW [2:1]	Anti-aliasing filter bandwidth. Default value: 00 00 = 800 Hz; 01 = 200 Hz; 10 =400 Hz; 11 =50 Hz)
FSCALE [2:0]	Full-scale selection. Default value: 000 000 = ±2*g*; 001 = ±4*g*; 010 = ±6*g*; 011 = ±8*g*; 100 = ±16*g*
SIM	SPI Serial Interface Mode selection. Default value: 0 0 = 4-wire interface; 1 = 3-wire interface

8.5 CTRL_REG7_A (25h)

Linear acceleration sensor control register 7(r/w).

Table 26. CTRL_REG7_A register

BOOT	FIFO_EN	WTM_EN	ADD_ INC	P1_ EMPTY	P1_WTM	P1_OVER RUN	BOOT_ INT

Table 27. CTRL_REG7_A register description

BOOT	Force reboot, cleared as soon as the reboot is finished. Active high. Default value: 0
FIFO_EN	FIFO enable. Default value: 0. 0 = Disable; 1 = Enable
WTM_EN	Enable FIFO watermark level use. Default value: 0. 0 = Disable; 1 = Enable
ADD_INC	Register address automatically incremented during a multiple byte access with a serial interface (I^2C or SPI). Default value: 0 0 = Disable; 1 = Enable
P1_EMPTY	Enable FIFO empty indication on INT1_A. Default value: 0. 0 = Disable; 1 = Enable
P1_WTM	FIFO Watermark interrupt on INT1_A. Default value: 0. 0 = Disable; 1 = Enable
P1_OVERRUN	FIFO Overrun interrupt on INT1_A. Default value: 0. 0 = Disable; 1 = Enable
P2_BOOT	BOOT interrupt on INT2_A. Default value: 0. 0 = Disable; 1 = Enable

8.6 STATUS_REG_A (27h)

Linear acceleration sensor status register (r).

Table 28. STATUS_REG_A register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 29. STATUS_REG_A register description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 0 = no overrun has occurred; 1 = a new set of data has overwritten the previous data
ZOR	Z-axis data overrun. Default value: 0 0 = no overrun has occurred; 1 = a new set of data for the Z-axis has overwritten the previous data.
YOR	Y-axis data overrun. Default value: 0 0 = no overrun has occurred; 1 = new data for the Y-axis has overwritten the previous data
XOR	X-axis data overrun. Default value: 0 0 = no overrun has occurred; 1 = new data for the X-axis has overwritten the previous data
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 0 = a new set of data is not yet available; 1 = a new set of data is available
ZDA	Z-axis new data available. Default value: 0 0 = new data for the Z-axis is not yet available; 1 = new data for the Z-axis is available
YDA	Y-axis new data available. Default value: 0 0 = new data for the Y-axis is not yet available; 1 = new data for the Y-axis is available
XDA	X-axis new data available. Default value: 0 0 = new data for the X-axis is not yet available; 1 = new data for the X-axis is available

8.7 OFF_X (10h)

Offset correction x-axis register, signed value (r/w).

Table 30. OFF_X default values

0	0	0	0	0	0	0	0

8.8 OFF_Y (11h)

Offset correction y-axis register, signed value (r/w).

Table 31. OFF_Y default values

0	0	0	0	0	0	0	0

8.9 OFF_Z (12h)

Offset correction z-axis register, signed value (r/w).

Table 32. OFF_Z default values

0	0	0	0	0	0	0	0

8.10 CS_X (13h)

Constant shift signed value x-axis register (r/w).

Table 33. CS_X default values

0	0	0	0	0	0	0	1

8.11 CS_Y (14h)

Constant shift signed value y-axis register (r/w).

Table 34. CS_Y default values

0	0	0	0	0	0	0	1

8.12 CS_Z (15h)

Constant shift signed value z-axis register (r/w).

Table 35. CS_Z default values

0	0	0	0	0	0	0	1

8.13 LC_L (16h) and LC_H (17h)

16-bit long-counter register for interrupt state machine programs timing (r/w)

Table 36. LC_L default values

0	0	0	0	0	0	0	1

Table 37. LC_H default values

0	0	0	0	0	0	0	0

01h = counting stopped, 00h = counter full: interrupt available and counter is set to default values higher than 00h: counting

8.14 STAT (18h)

Interrupt synchronization register (r).

Table 38. STAT register

LONG	SYNCW	SYNC1	SYNC2	INT_SM1	INT_SM2	DOR	DRDY

Table 39. STAT register description

LONG	LC interrupt flag. 0 = no interrupt; 1 = Long Counter (LC) interrupt flag common for both SM
SYNCW	Synchronization for external host controller interrupt based on output data 0 = no action waiting from host; 1 = action from host based on output data
SYNC1	0 = SM1 running normally; 1 = SM1 stopped and wait restart request from SM2
SYNC2	0 = SM2 running normally; 1 = SM2 stopped and wait restart request from SM1
INT_SM1	SM1- interrupt selection. 1 = SM1 interrupt generated; 0 = SM1 interrupt not generated
NT_SM2	SM2- interrupt selection. 1= SM2 interrupt generated; 0 = SM2 interrupt not generated
DOR	Data overrun indicates data not read from output register when the measurement of the next data samples starts. 0 = no overrun; 1 = data overrun data overrun bit is reset when next sample is ready
DRDY	data ready from output register. 0 = data not ready; 1 = data ready

8.15 VFC_1 (1Bh)

Vector coefficient register 1 for DIff filter (r/w).

Table 40. VFC_1 default values

0	0	0	0	0	0	0	0

8.16 VFC_2 (1Ch)

Vector coefficient register 2 for DIff filter (r/w).

Table 41. VFC_2 default values

0	0	0	0	0	0	0	0

8.17 VFC_3 (1Dh)

Vector coefficient register 3 for DIff filter (r/w).

Table 42. VFC_3 default values

0	0	0	0	0	0	0	0

8.18 VFC_4 (1Eh)

Vector coefficient register 4 for DIff filter (r/w).

Table 43. VFC_4 default values

0	0	0	0	0	0	0	0

8.19 THRS3 (1Fh)

Threshold value register (r/w).

Table 44. THRS3 default values

0	0	0	0	0	0	0	0

8.20 OUT_X_L_A (28h) and OUT_X_H_A (29h)

X-axis linear acceleration output data register (r). The value is expressed as two's complement.

8.21 OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)

Y-axis linear acceleration output data register (r). The value is expressed as two's complement.

8.22 OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)

X-axis linear acceleration output data register (r). The value is expressed as two's complement.

8.23 FIFO_CTRL_REG_A (2Eh)

linear acceleration sensor FIFO control register (r/w).

Table 45. FIFO_CTRL_REG_A register

FMODE2	FMODE1	FMODE0	WTMP4	WTMP3	WTMP2	WTMP1	WTMP0

Table 46. FIFO_CTRL_REG_A register description

FMODE [2:0]	FIFO mode selection. Default value: 000 (see *Table 47*)
WTMP [4:0]	FIFO threshold. Watermark level setting. FIFO depth if the watermark is enabled

Table 47. FIFO mode configuration

FMODE2	FMODE1	FMODE0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

Other configurations are not used.

8.24 FIFO_SRC_REG_A (2Fh)

Linear acceleration sensor FIFO source control register (r).

Table 48. FIFO_SRC_REG_A register

WTM	OVRN_ FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 49. IFO_SRC_REG_A register description

WTM	Watermark status. 0 = FIFO filling is lower than WTM level; 1 = FIFO filling is equal or higher than WTM level
OVRN_FIFO	Overrun bit status. 0 = FIFO is not completely filled; 1 = FIFO is completely filled
EMPTY	FIFO empty bit. 0 = FIFO not empty; 1 = FIFO empty)
FSS [4:0]	FIFO stored data level

8.25 CTRL_REG2_A (21h)

State machine 1 control register (r/w).

Table 50. CTRL_REG2_A register

HYST2_1	HYST1_1	HYST0_1	-	SM1_PIN	-	-	SM1_EN

Table 51. CTRL_REG2_A register description

HYST2_1 HYST1_1 HYST0_1	Hysteresis unsigned value to be added or subtracted from threshold value in SM1 Default value: 000
SM1_PIN	0 = SM1 interrupt routed to INT1_A pin, 1 = SM1 interrupt routed to INT2_A pin Default value: 0
SM1_EN	0 = SM1 disabled, 1 = SM1 enabled Default value: 0

8.26 STx_1 (40h-4Fh)

State machine 1 code register (r/w).

State machine 1 system register is composed of 16, 8-bit registers, to implement 16 steps op-code (STx_1 (x = 1-16)).

Table 52. STx_1 registers default values

0	0	0	0	0	0	0	0

0	0	0	0	0	0	0	0

8.27 TIM4_1 (50h)

8-bit general timer (unsigned value) for state machine 1 operation timing register (r/w).

Table 53. TIM4_1 default values

0	0	0	0	0	0	0	0

8.28 TIM3_1 (51h)

8-bit general timer (unsigned value) for state machine 1 operation timing register (r/w).

Table 54. TIM3_1 default values

0	0	0	0	0	0	0	0

8.29 TIM2_1 (52h - 53h)

16-bit general timer (unsigned value) for state machine 1 operation timing register (r/w).

Table 55. TIM2_1_L default values

0	0	0	0	0	0	0	0

Table 56. TIM2_1_H default values

0	0	0	0	0	0	0	0

8.30 TIM1_1 (54h - 55h)

16-bit general timer (unsigned value) for state machine 1 operation timing register (r/w).

Table 57. TIM1_1_L default values

0	0	0	0	0	0	0	0

Table 58. TIM1_1_H default values

0	0	0	0	0	0	0	0

8.31 THRS2_1 (56h)

Threshold signed value for state machine 1 operation register (r/w).

Table 59. THRS2_1 default value

0	0	0	0	0	0	0	0

8.32 THRS1_1 (57h)

Threshold signed value for state machine 1 operation register (r/w).

Table 60. THRS1_1 default values

0	0	0	0	0	0	0	0

8.33 MASKB_1 (59h)

Axis and sign mask (swap) for state machine 1 motion-detection operation register (r/w).

Table 61. MASKB_1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 62. MASKB_1 register description

P_X	0 = X + disabled, 1 =X+ enabled.Default value: 0
N_X	0 = X - disabled, 1 = X – enabled. Default value: 0
P_Y	0 = Y+ disabled, 1 = Y+ enabled. Default value: 0
N_Y	0 = Y- disabled, 1 = Y– enabled. Default value: 0
P_Z	0 = Z+ disabled, 1 = Z + enabled. Default value: 0
N_Z	0 = Z - disabled, 1 = Z – enabled. Default value: 0
P_V	0 = V + disabled, 1 = V + enabled. Default value: 0
N_V	0 = V - disabled, 1 = V – enabled. Default value: 0

8.34 MASKA_1(5Ah)

Axis and sign mask (default) for state machine 1 motion-detection operation register (r/w).

Table 63. MASKA_1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 64. MASKA_1 register description

P_X	0 = X + disabled, 1 =X+ enabled. Default value: 0
N_X	0 = X - disabled, 1 = X – enabled. Default value: 0
P_Y	0 = Y+ disabled, 1 = Y+ enabled. Default value: 0
N_Y	0 = Y- disabled, 1 = Y– enabled. Default value: 0
P_Z	0 = Z+ disabled, 1 = Z + enabled. Default value: 0
N_Z	0 = Z - disabled, 1 = Z – enabled. Default value: 0
P_V	0 = V + disabled, 1 = V + enabled. Default value: 0
N_V	0 = V - disabled, 1 = V – enabled. Default value: 0

8.35 SETT1 (5Bh)

Setting of threshold, peak detection and flags for state machine 1 motion-detection operation register (r/w)

Table 65. SETT1 register

P_DET	THR3_SA	ABS	-	-	THR3_MA	R_TAM	SITR

Table 66. SETT1 register description

P_DET	SM1 peak detection.Default value: 0 0 = peak detection disabled, 1 = peak detection enabled
THR3_SA	Default value: 0 0 = no action, 1 = Threshold 3 limit value for axis and sign mask reset (MASKB_1)
ABS	Default value: 0 0 = unsigned thresholds, 1 = signed thresholds
THR3_MA	Default value: 0 0 = no action, 1 = Threshold 3 limit value for axis and sign mask reset (MASKA_1)
R_TAM	Next condition validation flag. Default value: 0 0 = no valid next condition found, 1= valid next condition found and reset
SITR	Default value: 0 0 = no actions, 1 = program flow can be modified by STOP and CONT commands

8.36 PR1 (5Ch)

Program and reset pointer for state machine 1 motion-detection operation register (r/w)

Table 67. PR1 register

PP3	PP2	PP1	PP0	RP3	RP2	RP1	RP0

Table 68. PR1 register description

PP [3:0]	SM1 program pointer address. Default value: 0000
RP [3:0]	SM1 reset pointer address. Default value: 0000

8.37 TC1 (5Dh-5E)

16-bit general timer (unsigned output value) for state machine 1 operation timing register (r).

Table 69. TC1_L default values

0	0	0	0	0	0	0	0

Table 70. TC1_H default values

0	0	0	0	0	0	0	0

8.38 OUTS1 (5Fh)

Output flags on axis for interrupt state machine 1 management register (r).

Table 71. OUTS1 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 72. OUTS1 register description

P_X	0 = X + not shown, 1 = X+ shown. Default value: 0
N_X	0 = X - not shown, 1 = X – shown. Default value: 0
P_Y	0 = Y + not shown, 1 = Y+ shown. Default value: 0
N_Y	0 = Y - not shown, 1 = Y – shown. Default value: 0
P_Z	0 = Z + not shown, 1 = Z+ shown. Default value: 0
N_Z	0 = Z - not shown, 1 = Z – shown. Default value: 0
P_V	0 = V + not shown, 1 = V + shown. Default value: 0
N_V	0 = V - not shown, 1 = V – shown. Default value: 0

8.39 PEAK1 (19h)

Peak detection value register for state machine 1 operation register (r).

Table 73. PEAK1 default values

0	0	0	0	0	0	0	0

Peak detected value for next condition SM1

8.40 CTRL_REG3_A (22h)

State machine 2 control register (r/w).

Table 74. CTRL_REG3_A register

HYST2_2	HYST1_2	HYST0_2	-	SM2_PIN	-	-	SM2_EN

Table 75. CTRL_REG3_A register description

HYST2_2 HYST1_2 HYST0_2	Hysteresis unsigned value to be added or subtracted from threshold value in SM2 Default value = 000
SM2_PIN	0 = SM2 interrupt routed to INT1_A, 1 = SM2 interrupt routed to INT1_A pin Default value = 0
SM2_EN	0 = SM2 disabled, 1 = SM2 enabled Default value = 0

8.41 STx_2 (60h-6Fh)

State machine 2 code register (r/w).

State machine 2 system register is composed of 16, 8-bit registers, to implement 16 steps op-code (STx_2 (x = 1-16)).

Table 76. STx_2 register default values

0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---
0	0	0	0	0	0	0	0

8.42 TIM4_2 (70h)

8-bit general timer (unsigned value) for state machine 2 operation timing register (r/w).

Table 77. TIM4_2 default values

0	0	0	0	0	0	0	0

8.43 TIM3_2 (71h)

8-bit general timer (unsigned value) for state machine 2 operation timing (r/w).

Table 78. TIM3_2 default values

0	0	0	0	0	0	0	0

8.44 TIM2_2 (72h - 73h)

16 -bit general timer (unsigned value) for state machine 2 operation timing register (r/w).

Table 79. TIM2_2_L default values

0	0	0	0	0	0	0	0

Table 80. TIM2_2_H default values

0	0	0	0	0	0	0	0

8.45 TIM1_2 (74h - 75h)

16-bit general timer (unsigned value) for state machine 2 operation timing register (r/w).

Table 81. TIM1_2_L default values

0	0	0	0	0	0	0	0

Table 82. TIM1_2_H default values

0	0	0	0	0	0	0	0

8.46 THRS2_2 (76h)

Threshold signed value for state machine 2 operation register (r/w).

Table 83. THRS2_2 default values

0	0	0	0	0	0	0	0

8.47 THRS1_2 (77h)

Threshold signed value for state machine 2 operation register (r/w).

Table 84. THRS1_2 default values

0	0	0	0	0	0	0	0

8.48 MASKB_2 (79h)

Axis and sign mask (swap) for state machine 2 motion detection operation register (r/w).

Table 85. MASKB_2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 86. MASKB_2 register description

P_X	0 = X + disabled, 1 =X+ enabled. Default value: 0
N_X	0 = X - disabled, 1 = X – enabled. Default value: 0
P_Y	0 = Y+ disabled, 1 = Y+ enabled. Default value: 0
N_Y	0 = Y- disabled, 1 = Y– enabled. Default value: 0
P_Z	0 = Z+ disabled, 1 = Z + enabled. Default value: 0
N_Z	0 = Z - disabled, 1 = Z – enabled. Default value: 0
P_V	0 = V + disabled, 1 = V + enabled. Default value: 0
N_V	0 = V - disabled, 1 = V – enabled. Default value: 0

8.49 MASKA_2 (7Ah)

Axis and sign mask (default) for state machine 2 motion-detection operation register (r/w).

Table 87. MASKA_2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Table 88. MASKA_2 register description

P_X	0 = X + disabled, 1 =X+ enabled. Default value: 0
N_X	0 = X - disabled, 1 = X – enabled. Default value: 0
P_Y	0 = Y+ disabled, 1 = Y+ enabled. Default value: 0
N_Y	0 = Y- disabled, 1 = Y– enabled. Default value: 0
P_Z	0 = Z+ disabled, 1 = Z + enabled. Default value: 0
N_Z	0 = Z - disabled, 1 = Z – enabled. Default value: 0
P_V	0 = V + disabled, 1 = V + enabled. Default value: 0
N_V	0 = V - disabled, 1 = V – enabled. Default value: 0

8.50 SETT2 (7Bh)

Setting of threshold, peak detection and flags for state machine 2 motion detection operation register (r/w).

Table 89. SETT2 register

P_DET	THR3_SA	ABS	-	-	THR3_MA	R_TAM	SITR

Table 90. SETT2 register description

P_DET	SM2 peak detection. Default value: 0 0 = peak detection disabled, 1 = peak detection enabled
THR3_SA	Default value: 0 0 = no action, 1 = Threshold 3 limit value for axis and sign mask reset (MASKB_2)
ABS	Default value: 0 0 = unsigned thresholds, 1 = signed thresholds
THR3_MA	Default value: 0 0 = no action, 1 = Threshold 3 limit value for axis and sign mask reset (MASKA_2)
R_TAM	Next condition validation flag. Default value: 0 0 = no valid next condition found, 1 = valid next condition found and reset
SITR	Default value: 0 0 = no actions, 1 = program flow can be modified by STOP and CONT commands

8.51 PR2 (7Ch)

Program and reset pointer for state machine 2 motion-detection operation register (r/w).

Table 91. PR2 register

PP3	PP2	PP1	PP0	RP3	RP2	RP1	RP0

Table 92. PR2 register description

PP [3:0]	SM2 program pointer address.Default value: 0
RP [3:0]	SM2 reset pointer address. Default value: 0

8.52 TC2 (7Dh-7E)

16-bit general timer (unsigned output value) for state machine 2 operation timing register (r).

Table 93. TC2_L default values

0	0	0	0	0	0	0	0

Table 94. TC2_H default values

0	0	0	0	0	0	0	0

8.53 OUTS2 (7Fh)

Output flags on axis for interrupt SM2 management register (r).

Table 95. OUTS2 register

P_X	N_X	P_Y	N_Y	P_Z	N_Z	P_V	N_V

Read action of this register, depending on the flag will affect SM2 interrupt functions.

Table 96. OUTS2 register description

P_X	0 = X + not shown, 1 =X+ shown. Default value: 0
N_X	0 = X - not shown, 1 = X – shown. Default value: 0
P_Y	0 = Y + not shown, 1 =Y+ shown. Default value: 0
N_Y	0 = Y - not shown, 1 = Y – shown. Default value: 0
P_Z	0 = Z + not shown, 1 = Z+ shown. Default value: 0
N_Z	0 = Z - not shown, 1 = Z – shown. Default value: 0
P_V	0 = V + not shown, 1 = V + shown. Default value: 0
N_V	0 = V - not shown, 1 = V – shown. Default value: 0

8.54 PEAK2 (1Ah)

Peak detection value register for state machine 2 operation register (r).

Table 97. PEAK2 default values

0	0	0	0	0	0	0	0

Peak detected value for next condition SM2.

8.55 DES2 (78h)

Decimation counter value register for SM2 operation (w).

Table 98. DES2 default values

0	0	0	0	0	0	0	0

8.56 WHO_AM_I_G (0Fh)

Who am I angular rate sensor register (r)

Table 99. WHO_AM_I_G register

1	1	0	1	0	1	0	0

8.57 CTRL_REG1_G (20h)

Angular rate sensor control register 1 (r/w).

Table 100. CTRL_REG1_G register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 101. CTRL_REG1_G description

DR [1:0]	Output data rate selection. Default value: 00. Refer to*Table 102*
BW [1:0]	Bandwidth selection. Default value: 00. Refer to *Table 102*
PD	Power-down mode enable. Default value: 0 (0: Power-down mode, 1: Normal mode or Sleep mode)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

DR [1:0] is used to set ODR selection. **BW [1:0]** is used to set bandwidth selection.

The table below provides all the frequencies resulting from DR / BW bit combinations.

Table 102. DR and BW configuration setting

DR [1:0]	BW [1:0]	ODR [Hz]	Cut-off [Hz](1)
00	00	95	12.5
00	01	95	25
00	10	95	25
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

The combination of **PD, Zen, Yen, Xen** is used to set the angular rate sensor in different modes (Power-down / Normal / Sleep mode) according to the following table:

Table 103. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

8.58 CTRL_REG2_G (21h)

Angular rate sensor control register 2 (r/w).

Table 104. CTRL_REG2_G register

EXTRen	LVLen	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0

Table 105. CTRL_REG2_G description

EXTRen	Edge-sensitive trigger enable: Default value: 0 (0: external trigger disabled; 1: External trigger enabled)
LVLen	Level-sensitive trigger enable: Default value: 0 (0: level-sensitive trigger disabled; 1: level-sensitive trigger enabled)
HPM [1:0]	High-pass filter mode selection. Default value: 00 Refer to *Table 106*
HPCF [3:0]	High-pass filter cutoff frequency selection. Default value: 0000 Refer to *Table 107*

Table 106. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset by reading *REFERENCE_G (25h)* register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 107. High-pass filter cutoff frequency configuration [Hz](1)

HPCF[3:0]	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

1. Values in the table are indicative and can vary proportionally with the specific ODR value.

8.59 CTRL_REG3_G (22h)

Angular rate sensor control register 3 (r/w).

Table 108. CTRL_REG3_G register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 109. CTRL_REG3_G description

I1_Int1	Interrupt enable on INT1_G pin. Default value: 0. (0: Disable; 1: Enable)
I1_Boot	Boot status available on INT1_G. Default value: 0. (0: Disable; 1: Enable)
H_Lactive	Interrupt active configuration on INT1_G. Default value: 0. (0: High; 1: Low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: Push-pull; 1: Open drain)
I2_DRDY	Date ready on DRDY_G/INT2_G. Default value: 0. (0: Disable; 1: Enable)
I2_WTM	FIFO watermark interrupt on DRDY_G/INT2_G. Default value: 0. (0: Disable; 1: Enable)
I2_ORun	FIFO overrun interrupt on DRDY_G/INT2_G Default value: 0. (0: Disable; 1: Enable)
I2_Empty	FIFO empty interrupt on DRDY_G/INT2_G. Default value: 0. (0: Disable; 1: Enable)

8.60 CTRL_REG4_G (23h)

Angular rate sensor control register 4 (r/w).

Table 110. CTRL_REG4_G register

BDU	BLE	FS1	FS0	0	0	0	SIM

Table 111. CTRL_REG4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little Endian data selection. Default value: 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS [1:0]	Full-scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	3-wire SPI serial interface read mode enable. Default value: 0 (0: 3-wire read mode disabled; 1: 3-wire read enabled).

8.61 CTRL_REG5_G (24h)

Angular rate sensor control register 5 (r/w).

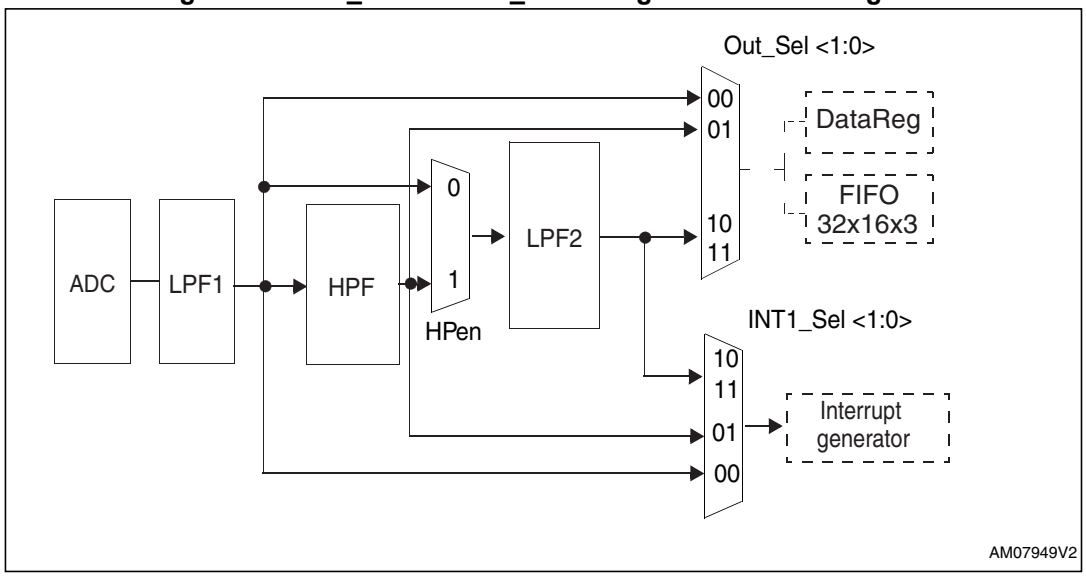
Table 112. CTRL_REG5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 113. CTRL_REG5_G description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disabled; 1: FIFO enabled)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, see *Figure 21*)
INT1_Sel [1:0]	INT1 selection configuration. Default value: 0 (see *Figure 21*)
Out_Sel [1:0]	Out selection configuration. Default value: 0 (see *Figure 21*)

Figure 21. INT1_Sel and Out_Sel configuration block diagram



8.62 REFERENCE_G (25h)

Interrupt reference value register (r/w).

Table 114. REFERENCE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 115. REFERENCE_G register description

Ref [7:0]	Reference value for interrupt generation. Default value: 0000 0000

8.63 OUT_TEMP_G (26h)

Temperature data output register (r).

Table 116. OUT_TEMP_G register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 117. OUT_TEMP_G register description

Temp [7:0]	Temperature data (1LSb/deg - 8-bit resolution). The value is expressed as two's complement.

8.64 STATUS_REG_G (27h)

Angular rate sensor register (r).

Table 118. STATUS_REG_G register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 119. STATUS_REG_G register description

ZYXOR	X-, Y-, Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y-, Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.65 OUT_X_L_G (28h), OUT_X_H_G (29h)

X-axis angular rate output data register (r). The value is expressed as two’s complement.

8.66 OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)

Y-axis angular rate output data register (r). The value is expressed as two’s complement.

8.67 OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)

Z-axis angular rate output data register (r). The value is expressed as two’s complement.

8.68 FIFO_CTRL_REG_G (2Eh)

Angular rate sensor FIFO control register (r/w).

Table 120. FIFO_CTRL_REG_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 121. FIFO_CTRL_REG_G register description

FM [2:0]	FIFO mode selection. Default value: 000 (see *Table 122*)
WTM [4:0]	FIFO threshold. Watermark level setting

Table 122. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

8.69 FIFO_SRC_REG_G (2Fh)

Angular rate sensor FIFO source control register (r).

Table 123. FIFO_SRC_REG_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 124. FIFO_SRC_REG_G register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal to or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS [4:0]	FIFO stored data level

8.70 INT1_CFG_G (30h)

Angular rate sensor FIFO source control register (r/w).

Table 125. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 126. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch Interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC_G reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

8.71 INT1_SRC_G (31h)

Angular rate sensor interrupt source register (r).

Table 127. INT1_SRC_G register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 128. INT1_SRC_G register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT1_SRC_G (31h)* IA bit (and eventually the interrupt signal on the INT1_G pin) and allows the refresh of data in the *INT1_SRC_G register* if the latched option was chosen.

8.72 INT1_THS_XH_G (32h)

Angular rate sensor interrupt threshold x-axis high register (r/w).

Table 129. INT1_THS_XH_G register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 130. INT1_THS_XH_G description

THSX [14:8]	Interrupt threshold. Default value: 000 0000

8.73 INT1_THS_XL_G (33h)

Angular rate sensor interrupt threshold x-axis low register (r/w).

Table 131. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 132. INT1_THS_XL_G description

THSX [7:0]	Interrupt threshold. Default value: 0000 0000

8.74 INT1_THS_YH _G (34h)

Angular rate sensor interrupt threshold y-axis high register (r/w).

Table 133. INT1_THS_YH_G register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 134. INT1_THS_YH_G description

THSY [14:8]	Interrupt threshold. Default value: 000 0000

8.75 INT1_THS_YL_G (35h)

Angular rate sensor interrupt threshold y-axis low register (r/w).

Table 135. INT1_THS_YL_G register

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 136. INT1_THS_YL_G description

THSY [7:0]	Interrupt threshold. Default value: 0000 0000

8.76 INT1_THS_ZH_G (36h)

Angular rate sensor interrupt threshold z-axis high register (r/w).

Table 137. INT1_THS_ZH_G register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 138. INT1_THS_ZH_G description

THSZ [14:8]	Interrupt threshold. Default value: 000 0000

8.77 INT1_THS_ZL_G (37h)

Angular rate sensor interrupt threshold z-axis low register (r/w).

Table 139. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 140. INT1_THS_ZL_G description

THSZ [7:0]	Interrupt threshold. Default value: 0000 0000

8.78 INT1_DURATION_G (38h)

Angular rate sensor interrupt duration register (r/w).

Table 141. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 142. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D [6:0]	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

WAIT bit has the following meaning:

Wait = '0': the interrupt falls immediately if signal crosses the selected threshold

Wait = '1': if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 22. Wait disabled

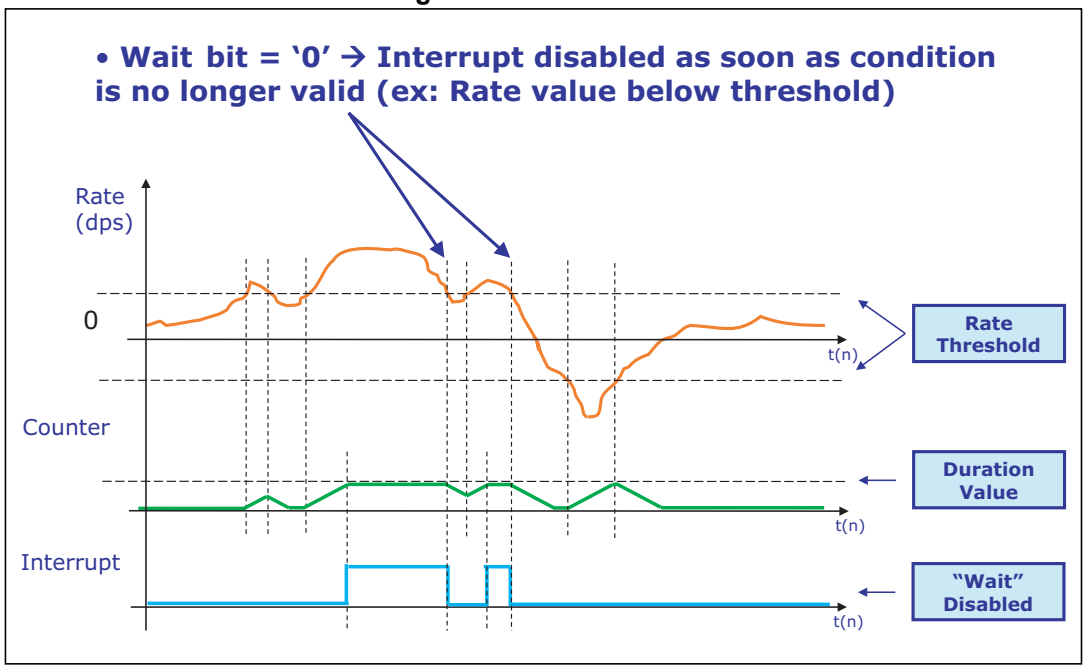
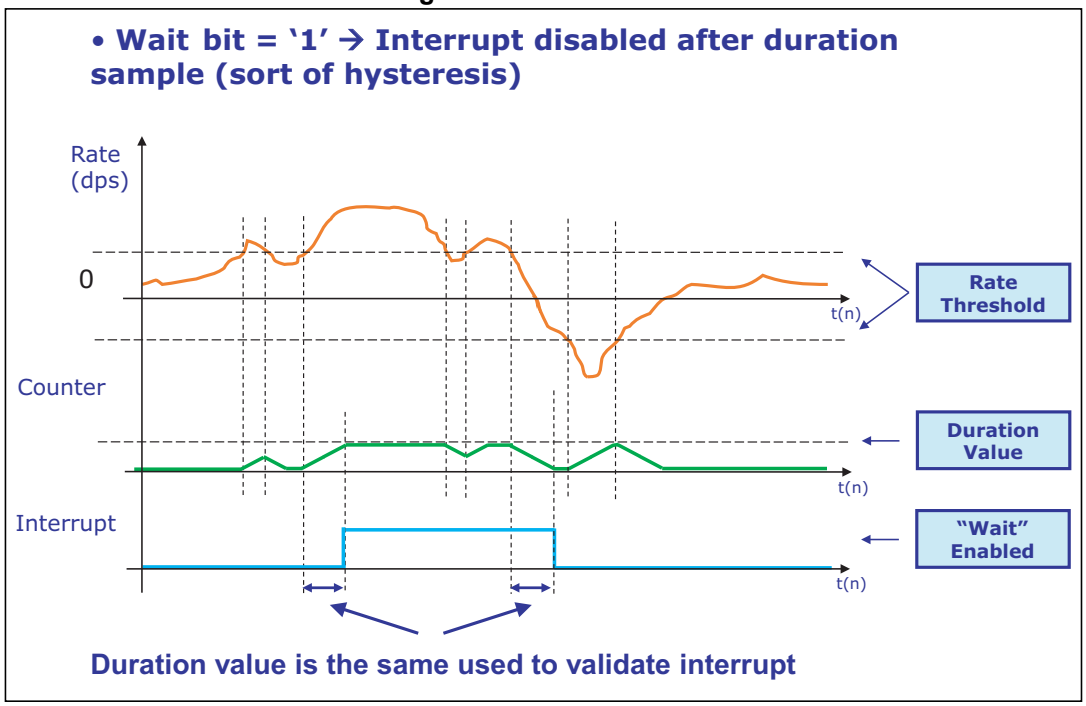


Figure 23. Wait enabled



9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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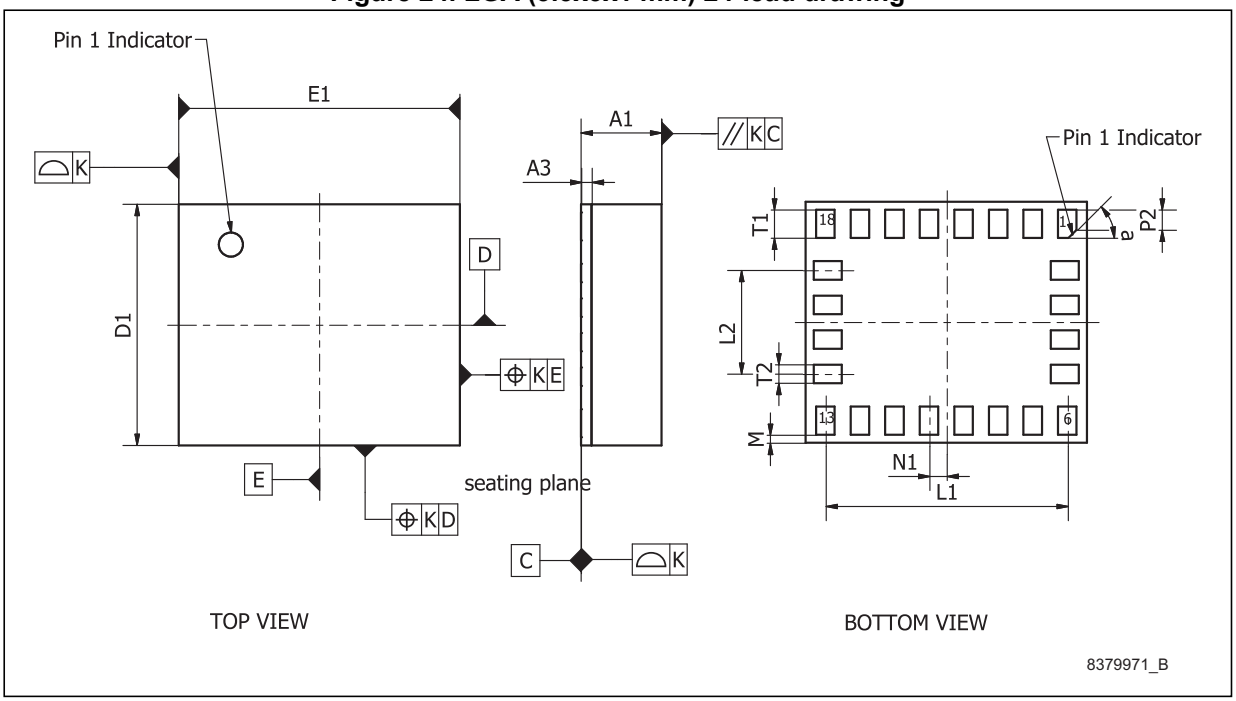
Table 143. LGA (3.5x3x1 mm) 24-lead mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1		1.000	1.027
A3		0.130	
D1	2.850	3.000	3.150
E1	3.350	3.500	3.650
L1	2.960	3.010	3.060
L2	1.240	1.290	1.340
N1	0.165	0.215	0.265
P2	0.200	0.250	0.300
a		45°	
T1	0.300	0.350	0.400
T2	0.180	0.230	0.280
M		0.100	
K		0.050	

Figure 24. LGA (3.5x3x1 mm) 24-lead drawing



10 Revision history

Table 144. Document revision history

Date	Revision	Changes
10-Jul-2012	1	Initial release.
04-Apr-2013	2	Document status promoted from preliminary data to production data.
09-Dec-2103	3	Updated *Table 143: LGA (3.5x3x1 mm) 24-lead mechanical data* and *Figure 24: LGA (3.5x3x1 mm) 24-lead drawing* Minor textual changes throughout document

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