SiT9002

LVPECL / HCSL / LVDS / CML

1 to 220 MHz High Performance Spread Spectrum Oscillator

Features

- World's first differential spread spectrum oscillator
- Extremely low cycle-cycle jitter
  - As low as10 ps (typical)
- Wide frequency range
  - 1 MHz to 220 MHz
  - 220 MHz to 800 MHz (contact SiTime)
- Eight spread selections (31.5 KHz modulation rate)
  - Center Spread: ±0.25%, ±0.5%, ±1.0%, ±2.0%
  - Down Spread: -0.5%, -1.0%, -2.0%, -4.0%
  - For -0.25% and ±0.125% contact SiTime
- Low frequency stability (Spread = OFF)
  - ±25 ppm or ±50 ppm
- Operating voltage
  - 1.8V or 2.5 or 3.3 V
- Operating temperature range:
  - Industrial, -40°C to 85°C
  - Extended Commercial, -20°C to 70°C
- Small footprint
  - 5.0 x 3.2 x 0.75 mm
  - 7.0 x 5.0 x 0.90 mm
- Pb-free and RoHS compliant
- Ultra-reliable start up and greater immunity from interference

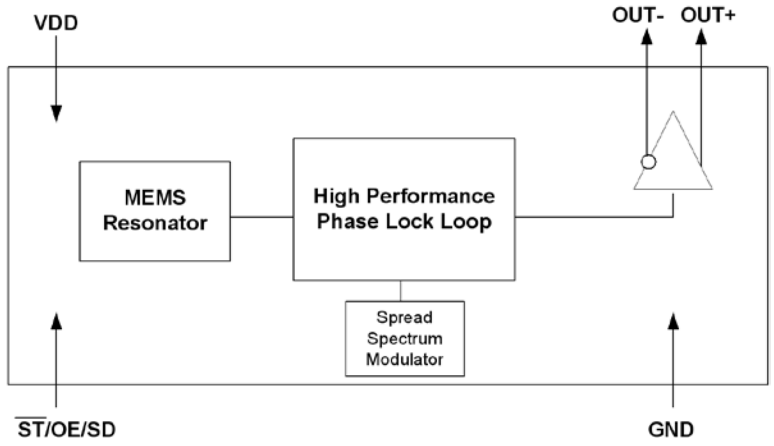
Benefits

- Services most PC peripherals, networking, and consumer applications
- Provides wide range of spread percentage for maximum electromagnetic interference (EMI) reduction
- Up to -17 dB reduction on third homonic and -12dB on the fundamental
- Fast time to market due to not needing to redesign the PCB for EMI reduction
- Factory programmable for ultra-fast lead time
- No crystal or load capacitors required
- Eliminates crystal qualification time
- 50%+ board saving space
- Completely quartz-free

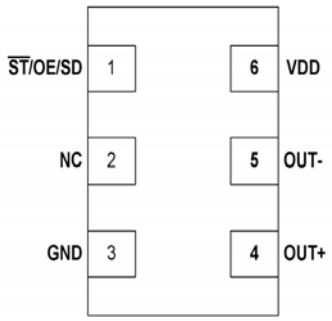
Applications

- PCI-Express
- USB 3.0
- Fully Buffered DIMM
- Blade Server
- Router
- System Clock
- Networking and Computing
- Automotive
- Industrial

Block Diagram



Pinout



Pin Description

Pin No.	Name		Pin Description
1	ST/OE/SD	Input	Standby or Output Enable pin for OUT+ and OUT-. OE: When High or Open : OUT+ and OUT- = active When Low : OUT+ and OUT- = High Impedance state ST: When High or Open : OUT+ and OUT- = active When Low : OUT+ and OUT- = Output is low (weak pull down), oscillation stops SD: Spread Disable - disables spread spectrum When High or Open : Spread Spectrum modulation = active When Low : Spread Spectrum modulation = Off
2	NC	NA	No connect pin, leave it floating.
3	GND	Power	VDD power supply ground. Connect to ground
4	OUT+	Output	1 to 220 MHz programmable clock output. For frequencies > 220 MHz contact SiTime
5	OUT-	Output	
6	VDD	Power	Power supply

Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not absolute maximum ratings.

Absolute Maximum Table

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Vin	GND - 0.5	VDD + 0.5	V
Theta JA (with copper plane on VDD and GND) 5.0 x 3.2 package	–	68	°C/W
7.0 x 5.0 package when center pad is soldered down	–	38	°C/W
7.0 x 5.0 package when center pad is not soldered down	–	90	°C/W
Theta JC (with PCB traces of 0.010 inch to all pins) 5.0 x 3.2 package	–	45	°C/W
7.0 x 5.0 package when center pad is soldered down	–	35	°C/W
7.0 x 5.0 package when center pad is not soldered down	–	48	°C/W
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Number of Program Writes	–	1	NA
Program Retention over -40 to 125C, Process, VDD (0 to 3.6V)	–	1,000+	years
Human Body Model (JESD22-A114)	2000	–	V
Charged Device Model (JESD22-C101)	750	–	–
Machine Model (JESD22-A115)	200	–	–

DC Electrical Specifications

Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	MIL-STD-883F, Method 1010-65-150°C (1000 cycle)
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

LVCMOS input, OE or $\overline{ST}$ pin, 3.3V ± 10% or 2.5V ± 10% or 1.8V ± 5%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		70	–	–	%Vdd
V_{IL}	Input Low Voltage		–	–	30	%Vdd
I_{IH}	Input High Current	OE or ST or SD pin	–	–	10	uA
I_{IL}	Input Low Current	OE or ST or SD pin	-10	–	–	uA
T_{pu}	Power Up Time	Time from minimum power supply voltage to the first cycle (Guaranteed no runt pulses)	–	–	10	ms

LVPECL, 3.3V ± 10% or 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD} = 3.3, Excluding Load Termination Current	–	75	84	mA
		V_{DD} = 2.5, Excluding Load Termination Current	–	75	84	mA
V_{OH}	Output High Voltage	50 Ohm termination to V_{DD} - 2.0V See Figure 2,3.	V_{DD}-1.1	–	V_{DD}-0.7	V
V_{OL}	Output Low Voltage		V_{DD}-2.0	–	V_{DD}-1.4	V
V_{swing}	Pk-Pk Output Voltage Swing		600	800	1000	mV

HCSL, 3.3V ±10% or 2.5V ±10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD} = 3.3, Excluding Load Termination Current	–	73	80	mA
		V_{DD} = 2.5, Excluding Load Termination Current	–	73	80	mA
V_{OH}	Output High Voltage	50 Ohm termination to GND See Figure 4.	0.6	0.75	0.95	V
V_{OL}	Output Low Voltage		0.0	–	50	mV
V_{swing}	Pk-Pk Output Voltage Swing		600	750	950	mV

LVDS, 3.3V ± 10% or 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
I_{DD}	Supply Current	V_{DD} = 3.3, Excluding Load Termination Current	–	75	85	mA
		V_{DD} = 2.5, Excluding Load Termination Current	–	70	77	mA
V_{OD1}	Differential Output Voltage	Swing Mode = Normal Single load termination. See Figure 5.	250	350	450	mV
ΔV_{OD1}	V_{OD} Magnitude Change		–	–	50	mV
V_{OS1}	Offset Voltage		–	1.2	–	V
ΔV_{OS1}	V_{OS} Magnitude Change		–	–	50	mV
V_{OD2}	Differential Output Voltage	Swing Mode = High Single load termination. See Figure 5.	500	700	900	mV
ΔV_{OD2}	V_{OD} Magnitude Change		–	–	50	mV
V_{OS2}	Offset Voltage		–	1.2	–	V
ΔV_{OS2}	V_{OS} Magnitude Change		–	–	50	mV
V_{OD3}	Differential Output Voltage	Swing Mode = High Double load termination. See Figure 6.	250	350	450	mV
ΔV_{OD3}	V_{OD} Magnitude Change		–	–	50	mV
V_{OS3}	Offset Voltage		–	1.2	–	V
ΔV_{OS3}	V_{OS} Magnitude Change		–	–	50	mV

CML, 3.3V ± 10% or 2.5V ± 10% or 1.8V ± 5%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			2.97	3.3	3.63	V
				2.25	2.5	2.75	V
				1.71	1.8	1.89	V
I_{DD}	Supply Current	V_{DD} = 3.3V	Excluding Load Termination Current	–	48	51	mA
		V_{DD} = 2.5V		–	48	51	mA
		V_{DD} = 1.8V		–	48	51	mA
V_{OH1}	Output High Voltage	Swing Mode = Normal Single Load Termination See Figure 7.		V_{DD}-0.1	–	V_{DD}	V
V_{OL1}	Output Low Voltage			V_{DD}-0.55	V_{DD}-0.425	V_{DD}-0.3	V
V_{swing1}	Pk-Pk Output Voltage Swing			300	425	550	mV
V_{OH2}	Output High Voltage	Swing Mode = High Single Load Termination See Figure 7.		V_{DD}-0.1	–	V_{DD}	V
V_{OL2}	Output Low Voltage			V_{DD}-1.1	V_{DD}-0.85	V_{DD}-0.6	V
V_{swing2}	Pk-Pk Output Voltage Swing			600	850	1100	mV
V_{OH3}	Output High Voltage	Swing Mode = High Double Load Termination See Figure 8.		V_{DD}-0.1	–	V_{DD}	V
V_{OL3}	Output Low Voltage			V_{DD}-0.55	V_{DD}-0.425	V_{DD}-0.3	V
V_{swing3}	Pk-Pk Output Voltage Swing			300	425	550	mV

AC Electrical Specifications

LVPECL, 3.3V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		100	150	300	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	10	16	ps
		F_{out} = 150 MHz, -0.5% down spread		–	8	14	ps
		F_{out} = 200 MHz, -0.5% down spread		–	8	14	ps

LVPECL, 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		100	150	300	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	10	16	ps
		F_{out} = 150 MHz, -0.5% down spread		–	8	14	ps
		F_{out} = 200 MHz, -0.5% down spread		–	8	14	ps

HCSL, 3.3V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	280	375	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	10	16	ps
		F_{out} = 150 MHz, -0.5% down spread		–	10	15	ps
		F_{out} = 200 MHz, -0.5% down spread		–	10	15	ps

HCSL, 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		200	300	400	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	9	19	ps
		F_{out} = 150 MHz, -0.5% down spread		–	9	17	ps
		F_{out} = 200 MHz, -0.5% down spread		–	9	15	ps

LVDS, 3.3V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		100	200	325	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	11	19	ps
		F_{out} = 150 MHz, -0.5% down spread		–	11	20	ps
		F_{out} = 200 MHz, -0.5% down spread		–	11	21	ps

LVDS, 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		100	260	325	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	14	26	ps
		F_{out} = 150 MHz, -0.5% down spread		–	14	26	ps
		F_{out} = 200 MHz, -0.5% down spread		–	14	27	ps

CML, 3.3V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		150	220	300	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	11	20	ps
		F_{out} = 150 MHz, -0.5% down spread		–	11	18	ps
		F_{out} = 200 MHz, -0.5% down spread		–	10	19	ps

CML, 2.5V ± 10%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		150	230	300	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	13	22	ps
		F_{out} = 150 MHz, -0.5% down spread		–	12	19	ps
		F_{out} = 200 MHz, -0.5% down spread		–	11	20	ps

CML, 1.8V ± 5%, -40 to 85°C

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
F_{out}	Output Frequency			1.0	–	220	MHz
F_{stab}	Frequency Stability	Inclusive of initial stability, operating temp., rated power supply voltage change, load change	-20 to 70°C	-25	–	+25	ppm
			-40 to 85°C	-50	–	+50	ppm
F_{age}	Aging	First year @ 25°C		–	–	1	PPM
DC	Duty Cycle			45	–	55	%
t_R/t_F	Output Rise/Fall Time	20% to 80%		150	230	300	ps
T_{CCJ}	Cycle-Cycle Jitter	F_{out} = 100 MHz, -0.5% down spread		–	13	23	ps
		F_{out} = 150 MHz, -0.5% down spread		–	12	22	ps
		F_{out} = 200 MHz, -0.5% down spread		–	12	21	ps

Termination Diagrams

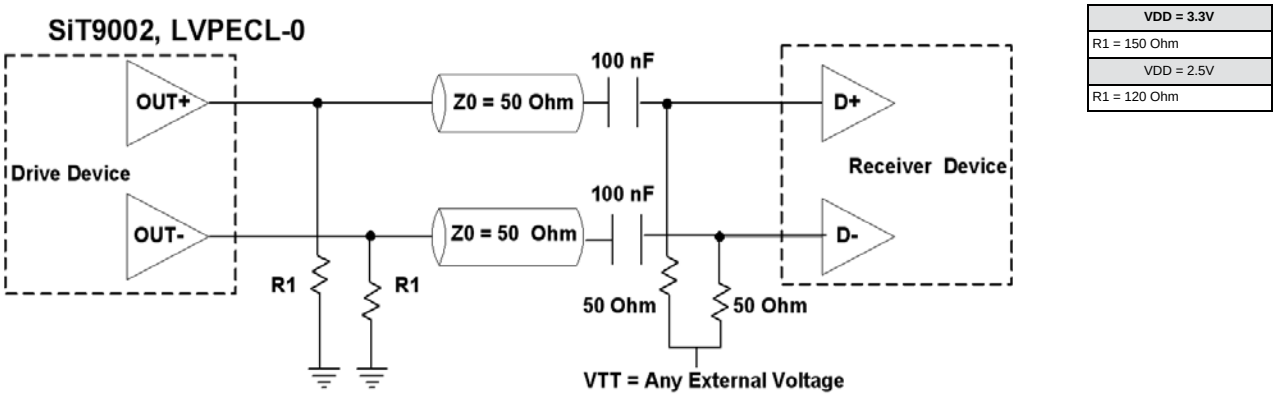


Figure 1. LVPECL AC Coupled Typical Termination

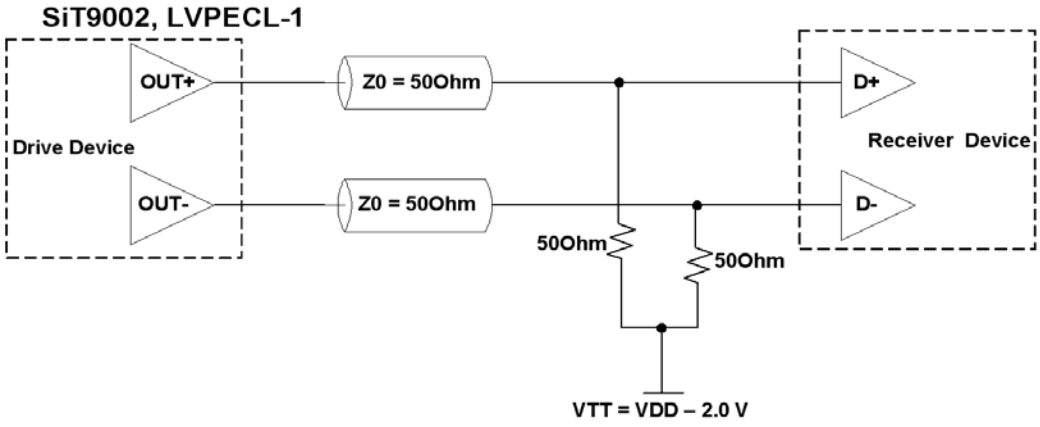
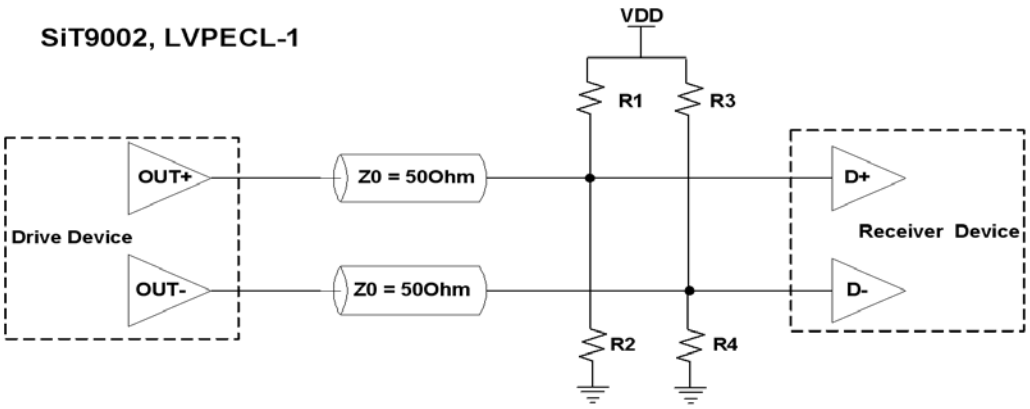
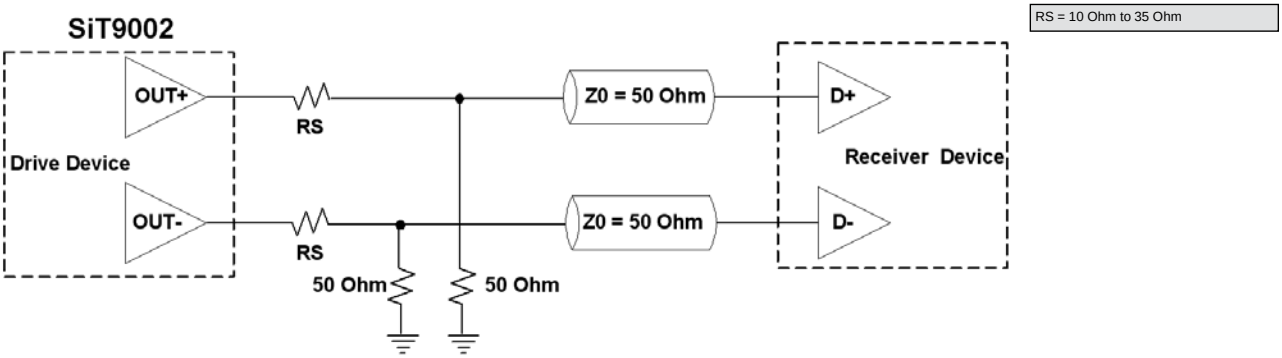


Figure 2. LVPECL DC Coupled Typical Termination with Termination Voltage



VDD = 3.3V
R1 = R3 = 133 Ohm
R2 = R4 = 82 Ohm
VDD = 2.5V
R1 = R3 = 250 Ohm
R2 = R4 = 62.5 Ohm

Figure 3. LVPECL DC Coupled Typical Termination without Termination Voltage



RS = 10 Ohm to 35 Ohm

Figure 4. HCSL Typical Termination

Note:
1. All the tests are done with RS = 20 Ohm (recommended).

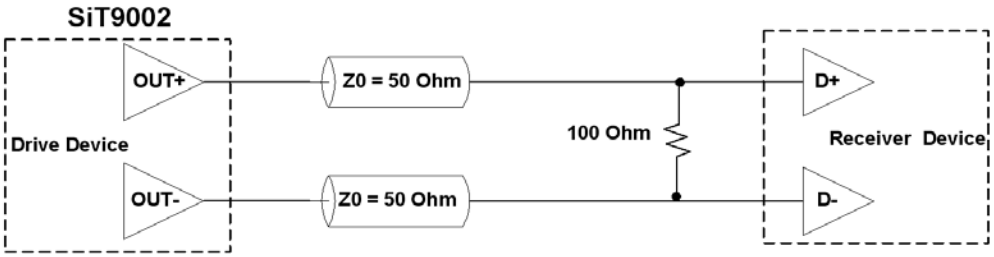
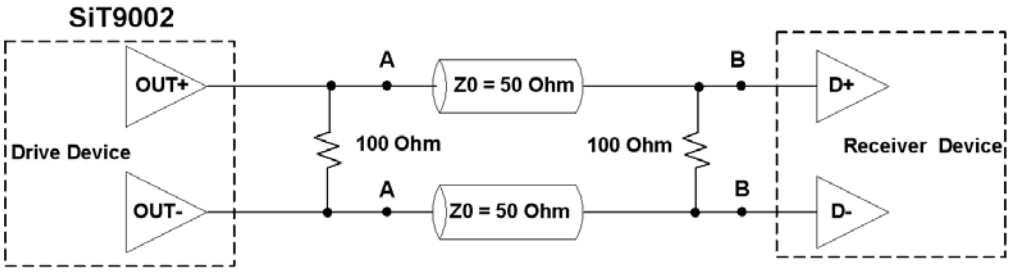


Figure 5. LVDS Single Load Termination (Load Terminated)



*Note: For AC coupled operation, include/insert decoupling caps at points **A** or **B***

Figure 6. LVDS Double Termination (Source + Load Terminated)

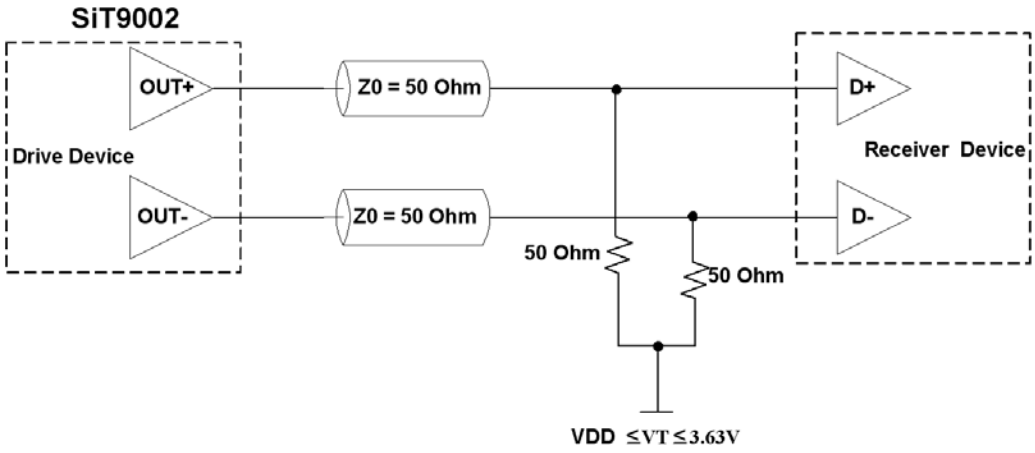
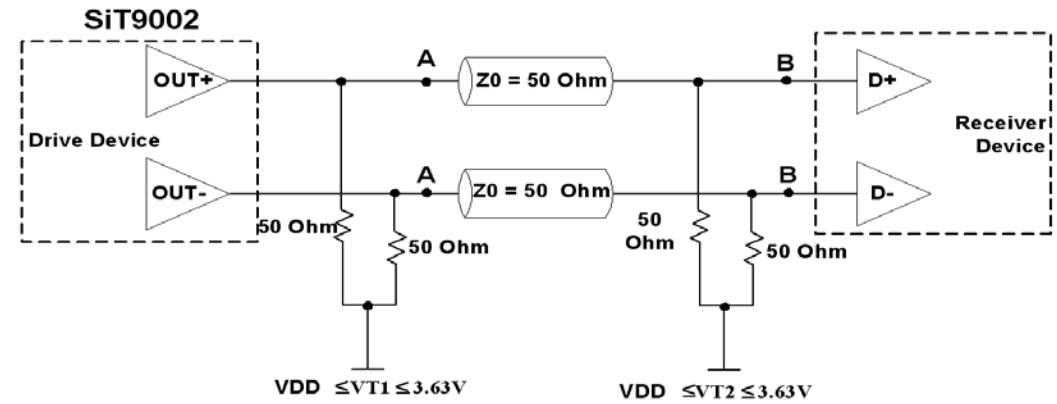


Figure 7. CML Single Load Termination

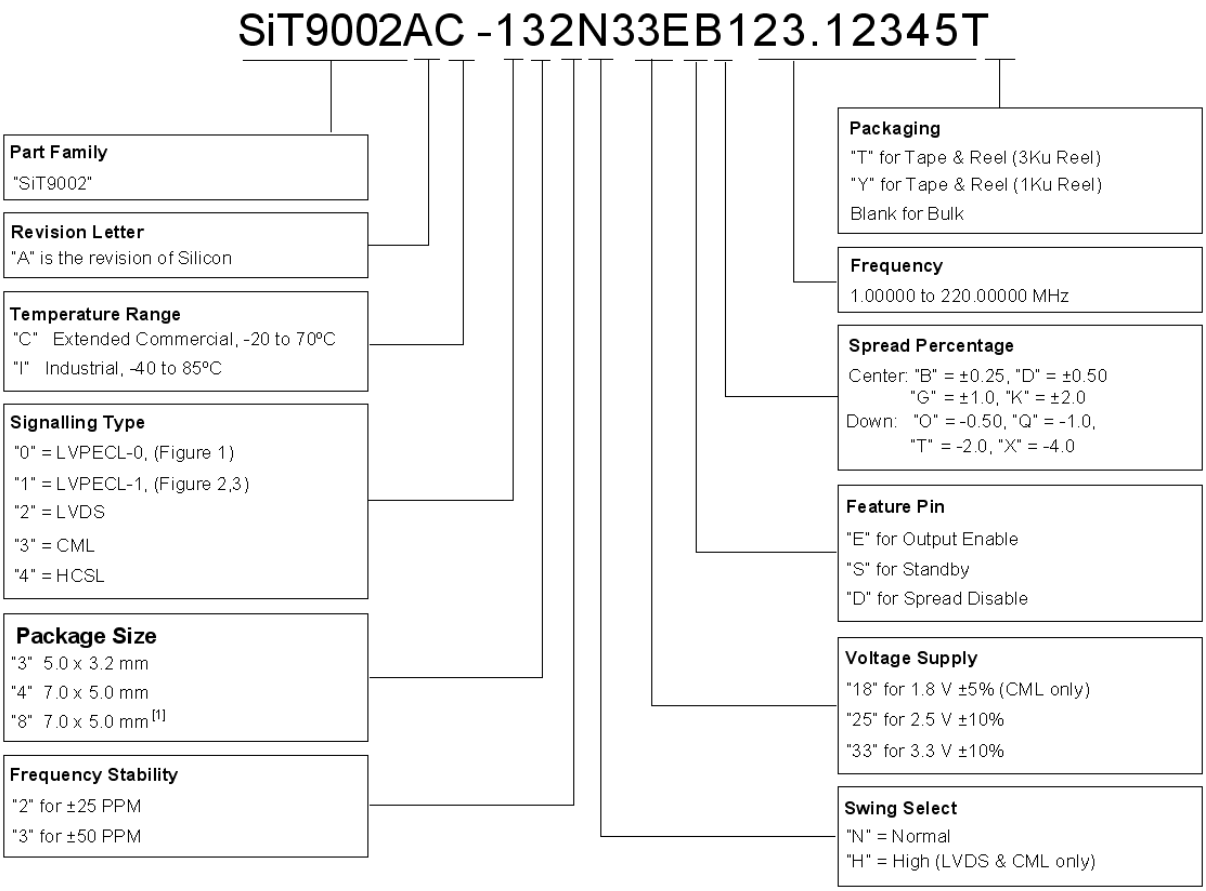


Notes:
1. For DC-coupled operation, VT1 = VT2
2. For AC coupled operation, include/insert decoupling caps at points A or B
3. For AC-coupled operation with capacitors placed at point A, VT2 sets the input common mode of Receiver Device and need not to be related to VT1

Figure 8. CML Double Load Termination

Ordering Information

The Part No. Guide is for reference only. For real-time customization and exact part number, use the SiTime Part Number Generator.



Frequency Stability vs. Temperature Range Options

Frequency Stability (PPM)	Temperature Range	Supply Voltage		
		1.8 V	2.5 V	3.3 V
±25	C (-20 to +70°C)	✓	✓	✓
	I (-40 to +85°C)	✓	✓	✓
±50	C (-20 to +70°C)	✓	✓	✓
	I (-40 to +85°C)	✓	✓	✓

Signaling Type vs. Swing Select Options

Signaling Type	Swing Select	Supply Voltage		
		1.8 V	2.5 V	3.3 V
LVPECL-0	Normal	–	✓	✓
	High	–	–	–
LVPECL-1	Normal	–	✓	✓
	High	–	–	–
LVDS	Normal	–	✓	✓
	High	–	✓	✓
CML	Normal	✓	✓	✓
	High	✓	✓	✓
HCSL	Normal	–	✓	✓
	High	–	–	–

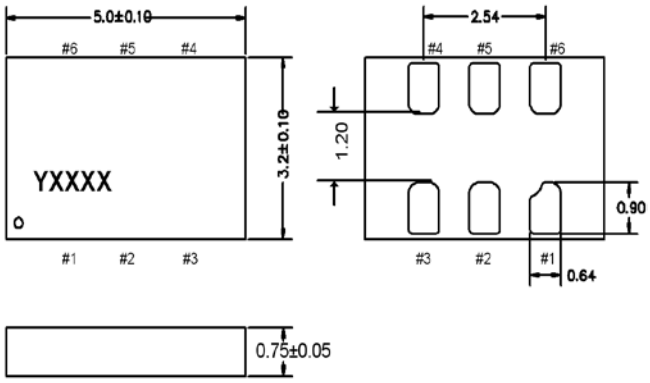
Note:
1. Without Center Pad.

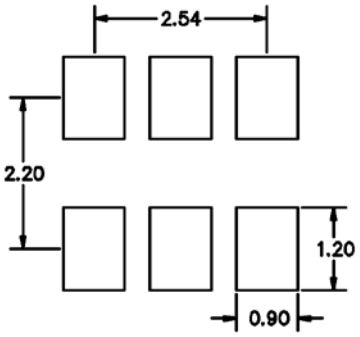
Package Information [2]

Dimension (mm)

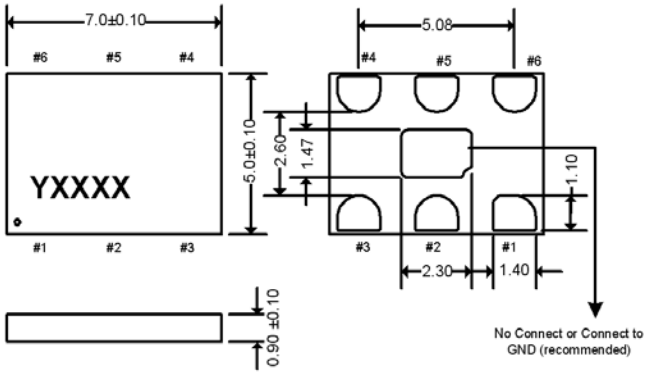
Land Pattern[3] (recommended) (mm)

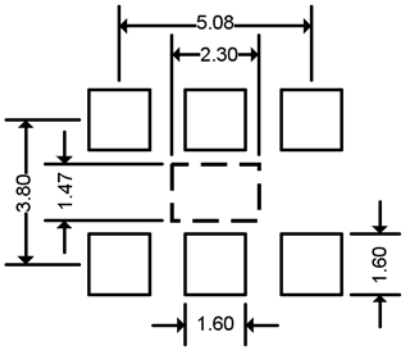
5.0 x 3.2 x 0.75mm





7.0 x 5.0 x 0.90mm





Notes:

2. Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
3. A capacitor of value 0.1µF between VDD and GND is recommended.
4. The 7050 package with part number designation "-8" has NO center pad.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

SiTime:

SiT9002AC-032N25DO133.000000Y SiT9002AC-043N33EQ200.000000Y SiT9002AC-083N33DO100.000000Y SiT9002AI-032N33DO180.00000Y SiT9002AI-232N25DO150.000000Y SiT9002AI-233N33DQ100.000000Y SiT9002AI-233N33DQ100.00000X SIT9002AI-232N33DO135.00000X SIT9002AI-233N25DO100.00000Y SiT9002AI-232N33DO90.000000T