

SiT3372

Advanced Information

10 MHz to 220 MHz Ultra-low Jitter Differential VCXO



Features

- Any frequency between 10 MHz and 220 MHz accurate to 6 decimal places
- Widest pull range options: ± 25 , ± 50 , ± 80 , ± 100 , ± 150 , ± 200 , ± 400 , ± 800 , ± 1600 , ± 3200 ppm
- 0.23 ps RMS phase jitter (Typ) over 12 kHz to 20 MHz bandwidth
- Wide temperature range support from -40°C to 85°C
Contact SiTime for other temperature range options
- Industry-standard packages: 3.2x2.5, 7.0x5.0 mm
Contact SiTime for 5.0 x 3.2 mm package
- For frequencies 220 MHz to 700 MHz, refer to SiT3373 datasheet

Applications

- Remote Radio Head (RRH), Cable Modem Termination System (CMTS), Video, Broadcasting System, Audio, Industrial Sensors
- SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express



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Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage

Table 1. Electrical Characteristics - Common to LVPECL, LVDS and HCSL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	10	–	220	MHz	Accurate to 6 decimal places
Frequency Stability						
Frequency Stability	F_stab	-15	–	+15	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variations, and first year aging at 25°C condition
		-25	–	+25	ppm	
		-30	–	+30	ppm	
		-50	–	+50	ppm	
Temperature Range						
Operating TemperatureRange	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact SiTime for other temperature range options
Supply Voltage						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.7	3.0	3.3	V	
		2.52	2.8	3.08	V	
		2.25	2.5	2.75	V	
Voltage Control Characteristics						
Pull Range	PR	±25, ±50, ±80, ±100, ±150, ±200, ±400, ±800, ±1600, ±3200ppm			ppm	See the last page for Absolute Pull Range, APR Table. Contact SiTime for custom pull range options.
Upper Control Voltage	VC_U	90%	–	–	Vdd	Voltage at which maximum frequency deviation is guaranteed
Lower Control Voltage	VC_L	–	–	10%	Vdd	Voltage at which minimum frequency deviation is guaranteed
Control Voltage Input Impedance	VC_z	–	10	–	MΩ	
Control Voltage Input Bandwidth	V_c	–	10	–	kHz	Contact SiTime for other input bandwidth options
Pull Range Linearity	Lin	–	1	TBD	%	
Frequency Change Polarity	–	Positive Slope			–	
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pin 2, OE
Input Voltage Low	VIL	–	–	30%	Vdd	Pin 2, OE
Input Pull-up Impedance	Z_in	–	100	-	kΩ	Pin 2, OE logic high or logic low

Table 2. Electrical Characteristics - Common to LVPECL, LVDS and HCSL (Cont'd)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Startup and OE Timing						
Start-up Time	T_start	–	–	5	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T_oe	–	–	515	ns	f = 212.5 MHz - For other frequencies, T_oe = 500ns + 3 period

Table 3. Electrical Characteristics - LVPECL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	84	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	55	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	μA	OE = Low
Maximum Output Current	I_driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output Characteristics						
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 2
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 2
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	250	–	ps	20% to 80%, see Figure 2
Jitter						
RMS Period Jitter ^[1]	T_jitt	–	1	2	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.23	–	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

1. Measured according to JESD65B

Table 4. Electrical Characteristics – LVDS Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	Idd	–	–	76	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	55	mA	OE = Low
Output Disable Leakage Current	I_leak	–	0.15	–	μA	OE = Low
Output Characteristics						
Differential Output Voltage	VOD	250	–	450	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	–	340	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
Jitter						
RMS Period Jitter ^[2]	T_jitt	–	1	2	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.23	–	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

2. Measured according to JESD65B

Table 5. Electrical Characteristics – HCSL Specific

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption						
Current Consumption	I _{dd}	–	–	84	mA	Excluding Load Termination Current, V _{dd} = 3.3V or 2.5V
OE Disable Supply Current	I _{OE}	–	–	55	mA	OE = Low
Output Disable Leakage Current	I _{leak}	–	0.15	–	μA	OE = Low
Output Characteristics						
Output High Voltage	VOH	0.6	–	0.8	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.05	V	See Figure 2
Output Differential Voltage Swing	V _{Swing}	1	1.4	1.8	V	See Figure 3
Rise/Fall Time	Tr, Tf	–	350	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 2
Jitter						
RMS Period Jitter ^[3]	T _{jitt}	–	1	2	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T _{phj}	–	0.23	–	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
		–	0.1	–	ps	f = 156.25 MHz, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, all Vdds

Notes:

3. Measured according to JESD65B

Table 6. Pin Description

Pin	Symbol	Functionality	
1	VIN	Input	Control Voltage
2	NC/OE	No Connect (NC)	No Connect: Leave it floating or connect to GND for better heat dissipation
		Output Enable (OE)	H ^[4] : specified frequency output L: output is high impedance. Only output driver is disabled
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage ^[5]

Notes:

- In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- A capacitor of value 0.1 μF or higher between Vdd and GND is required. An Additional 10 pF between Vdd and GND is required for the best phase jitter performance

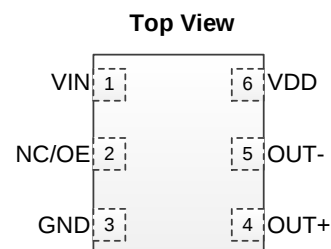


Figure 1. Pin Assignments

Table 7. Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge (HBM)	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C

Table 8. Thermal Consideration^[6]

Package	θ_{JA} , 4 Layer Board (°C/W)	θ_{JC} , Bottom (°C/W)
3225, 6-pin	TBD	TBD
7050, 6-pin	TBD	TBD

Notes:

6. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 9. Maximum Operating Junction Temperature^[7]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	80
85°C	95

Notes:

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 10. Environmental Compliance

Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

Waveform Diagrams

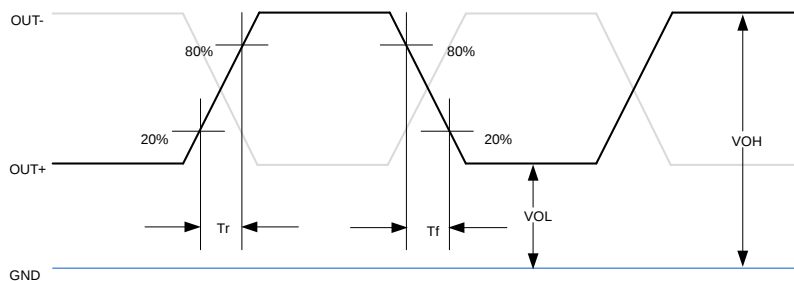


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

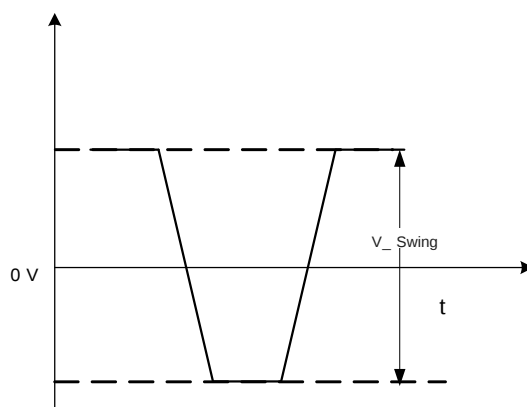


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

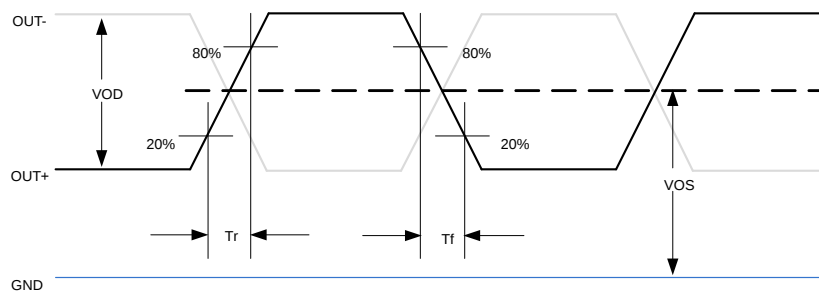


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

Termination Diagrams

LVPECL:

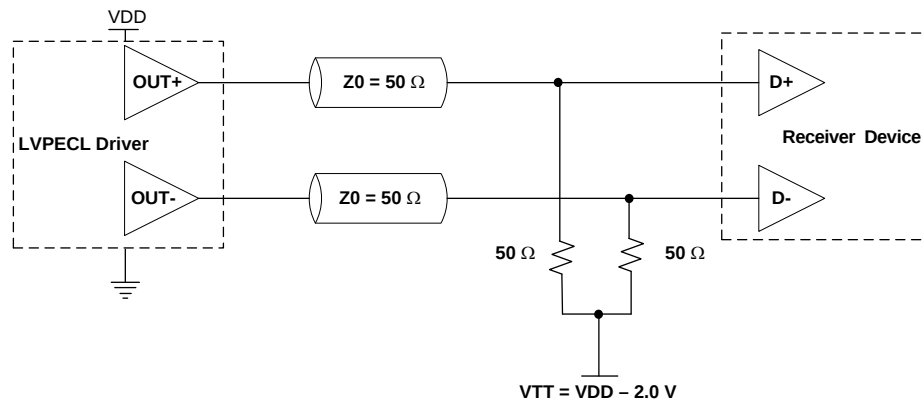


Figure 5. LVPECL Typical Termination

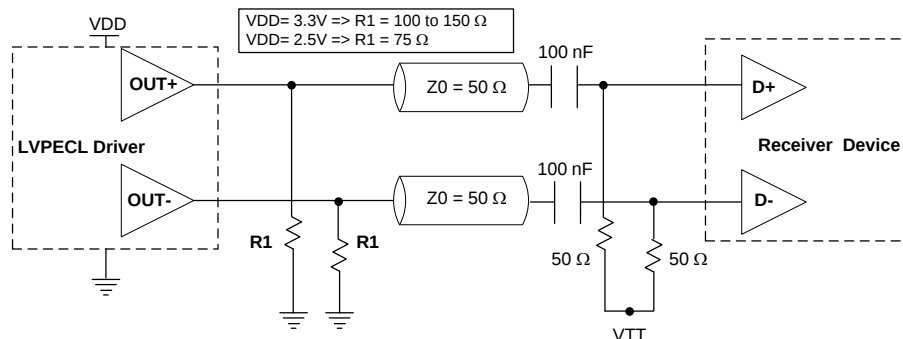


Figure 6. LVPECL AC Coupled Termination

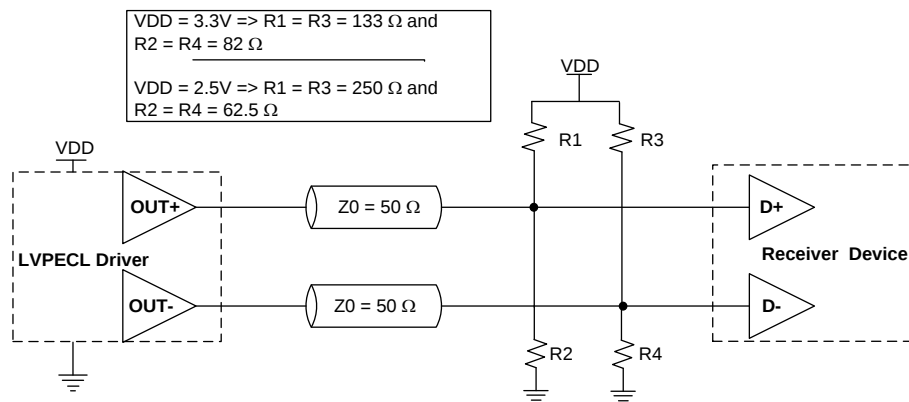


Figure 7. LVPECL with Thevenin Typical Termination

Termination Diagrams (Continued)

LVDS:

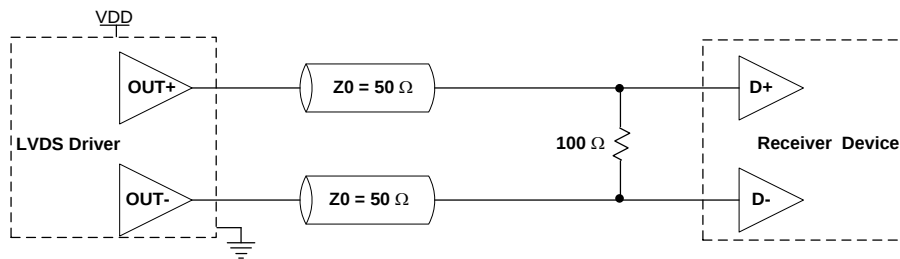


Figure 8. LVDS Single Termination (Load Terminated)

HCSL:

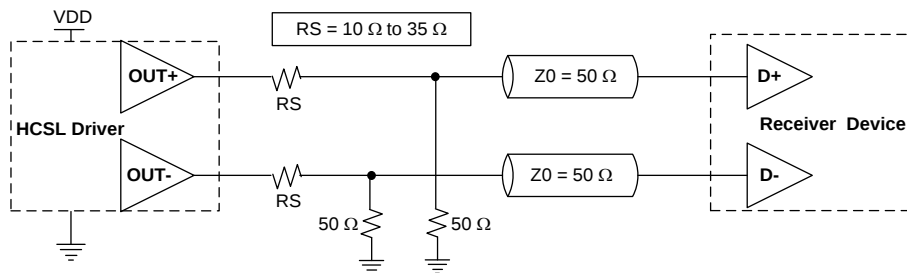
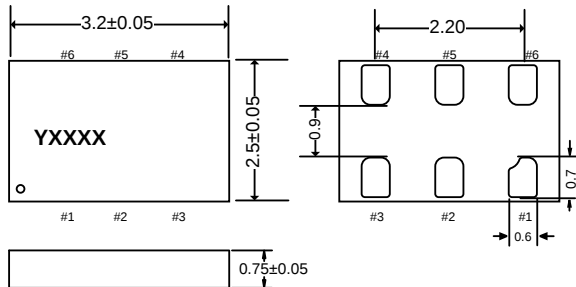
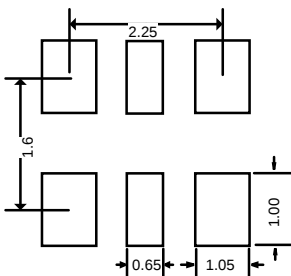
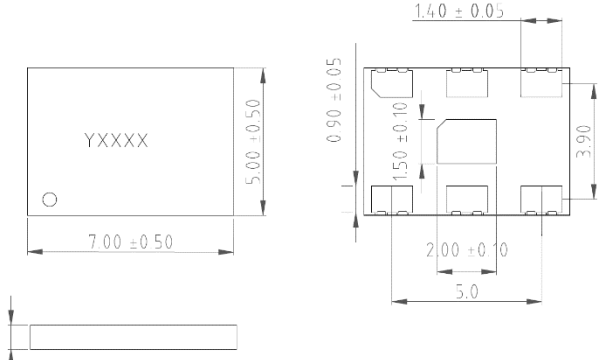
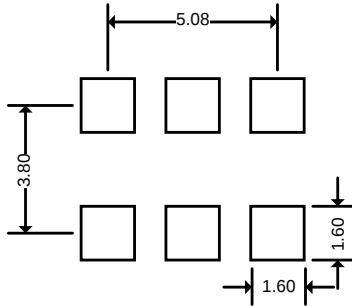


Figure 9. HCSL Typical Termination

Dimensions and Patterns

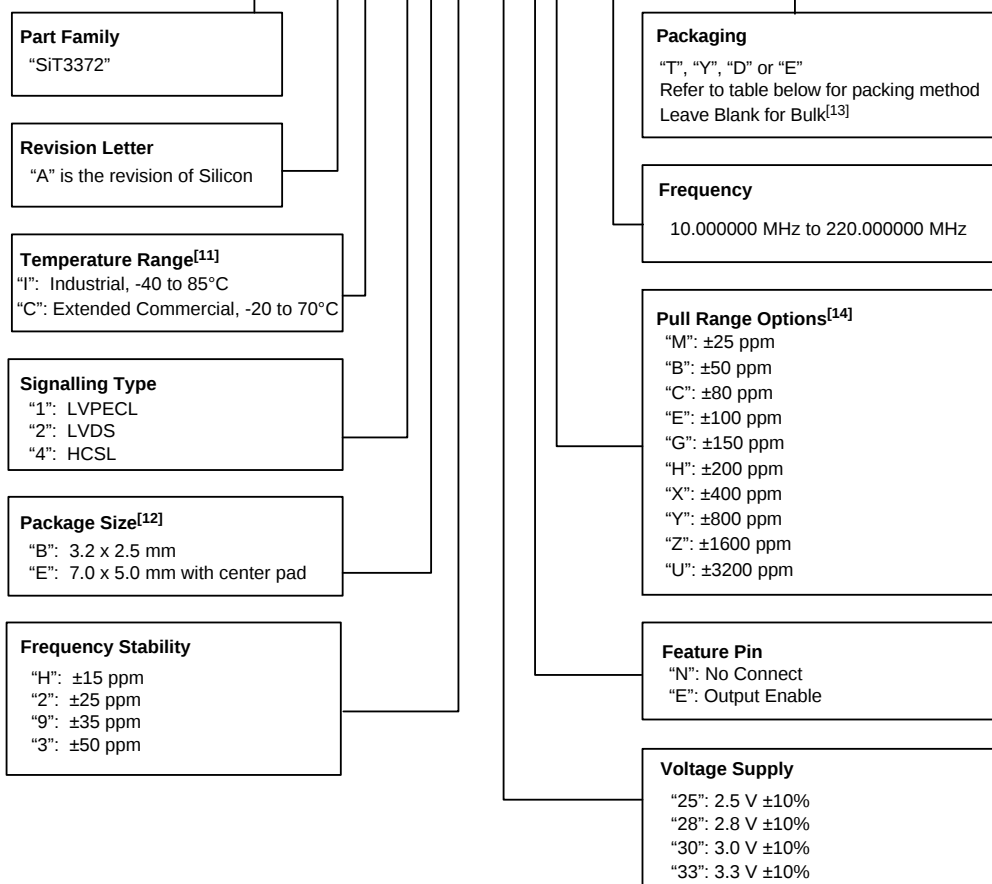
Package Size – Dimensions (Unit: mm) ^[8]	Recommended Land Pattern (Unit: mm) ^[9]
3.2 x 2.5x 0.75 mm 	
7.0 x 5.0x 0.90 mm^[10] 	

Notes:

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
9. A capacitor of value 0.1 μ F or higher between Vdd and GND is required.
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

Ordering Information

SiT3372AC-1B2-33-H122.123456T



Notes:

11. Contact SiTime for higher temperature options
12. Contact SiTime for 5.0 x 3.2 package
13. Bulk is available for sampling only
14. Contact SiTime for custom pull range options

Table 11. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

Table 12. APR Table

Absolute pull range (APR) = Nominal pull range (PR) - frequency stability (F_stab)

Nominal Pull Range	Frequency Stability			
	± 15	± 25	± 35	±50
	APR (ppm)			
± 25	± 5	—	—	—
± 50	± 30	± 20	± 10	—
± 80	± 60	± 50	± 40	± 25
± 100	± 80	± 70	± 60	± 45
± 150	± 130	± 120	± 110	± 95
± 200	± 180	± 170	± 160	± 145
± 400	± 380	± 370	± 360	± 345
± 800	± 780	± 770	± 760	± 745
± 1600	± 1580	± 1570	± 1560	± 1545
± 3200	± 3180	± 3170	± 3160	± 3145

Table 13. Revision History

Revision	Release Date	Change Summary
0.1	09/14/16	Initial draft
0.2	9/16/16	Removed 5.0 x 3.2 package
0.25	9/21/16	Revised the Electrical characteristics tables Revised frequency stability values in the ordering information Added Output Enable option into Pin 2 function Revised 7050 package dimension

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