

# UG256: Si5383 Evaluation Board User's Guide

The Si5383-EVB is used for evaluating the Si5383 Network Synchronizer Clock for SyncE/1588 and Stratum 3/3E applications. The Si5383 contains three independent DSPLLs in a single IC with programmable jitter attenuation bandwidth on a per DSPLL basis. The Si5383-EVB supports three independent differential input clocks, two independent CMOS input clocks, and seven independent output clocks via onboard SMA connectors. The Si5383-EVB can be controlled and configured via a USB connection to a host PC running Silicon Labs' next generation Clock Builder Pro<sup>™</sup> (CBPro<sup>™</sup>) software tool. Test points are provided on-board for external monitoring of supply voltages.

#### EVB FEATURES

- Powered from USB port or external +5 V power supply via screw terminals
- Onboard 48 MHz XTAL and included SiOCXO1-EB reference board allows standalone or holdover mode of operation on the Si5383
- CBPro™ GUI programmable V<sub>DDO</sub> supplies allow each of the seven outputs to have its own supply voltage selectable from 3.3, 2.5, or 1.8 V
- CBPro<sup>™</sup> GUI allows control and measurement of voltage, current, and power of VDD and all 7 VDDO supplies
- Status LEDs for power supplies and control/status signals of Si5383
- SMA connectors for input clocks, output clocks and optional external timing reference clock



# 1. Si5383-EVB Functional Block Diagram, Support Documentation, and ClockBuilder Pro™ Software

Below is a functional block diagram of the Si5383-EVB. This EVB can be connected to a PC via the main USB connector for programming, control, and monitoring. See 2. Quick Start and Jumper Defaults for more information.



Figure 1.1. Si5383-EVB Functional Block Diagram

All Si5383 EVB schematics, BOMs, User's Guides, and software can be found online at the following link:http://www.silabs.com/prod-ucts/clocksoscillators/pages/Si538x-4x-evb.aspx

# 2. Quick Start and Jumper Defaults

- 1. Install ClockBuilder Pro desktop software from EVB support web page given in Section 1.
- 2. Connect the USB cable from Si5383-EVB to PC with ClockBuilder Pro software installed.
- 3. Connect the SIOCXO1-EB to the reference input using the included SMA cable.
- 4. Leave the jumpers as installed from the factory, and launch the ClockBuilder Pro software.
- 5. You can use ClockBuilder Pro to create, download, and run a frequency plan on the Si5383-EVB.

6. For the Si5383 data sheet, go to http://www.silabs.com/timing

#### Table 2.1. Si5383 EVB Jumper Defaults<sup>1</sup>

Location	Туре	I = Installed O = Open	Location	Туре	I = Installed O = Open
JP2	2 pin	I	JP21	3 pin	0
JP3	2 pin	I	JP22	2 pin	0
JP4	2 pin	I	JP23	2 pin	0
JP5	3 pin	1	JP24	3 pin	0
JP13	2 pin	O (Jumper sup- plied)	JP25	2 pin	0
JP14	2 pin	0	JP26	3 pin	0
JP15	2 pin	0	JP27	2 pin	0
JP16	3 pin	0	JP28	3 pin	0
JP17	3 pin	0	JP29	2 pin	0
JP18	2 pin	0	JP31-J34	2 pin	Probe Points
JP19	2 pin	0	J48	3x2 Hdr	3 installed
JP20	3 pin	0	J22	5x2 Hdr	0

#### Note:

1. Refer to the Si5383 EVB schematics for the functionality associated with each jumper.

2. J31-J34 are intended to be probe points and jumpers should not be installed.

# 3. Status LEDs

Location	Silkscreen	Color	Status Function Indication	
D11	+5V PWR, EXT USB	Green	Main USB +5V present	
D12	READY	Green	MCU Ready	
D13	BUSY	Green	MCU Busy	
D5	INTRB	Blue	Si5383 Interrupt Active	
D7	LOL_REFB	Blue	Loss of Reference Lock	
D8	LOL_AB	Blue	Loss of Lock, DSPLL A	
D18	LOL_DC	Blue	Loss of Lock, DSPLL C	
D19	LOL_DB	Blue	Loss of Lock, DSPLL D	

#### Table 3.1. Si5383 EVB Status LEDs

D11 is illuminated when the USB+5V supply voltage is present. D12 and D13 are illuminated when the MCU is either Ready or Busy, respectively. D5 is illuminated when the Si5383's interrupt alarm is asserted. D7, D8, D18, and D19 are illuminated when the associated PLL is not locked, D7 is the Reference PLL, D8 is for PLLA, D18 is for PLLC, and D19 is for PLLD.



Figure 3.1. Si5383-EVB LED Locations

# 4. External Crystal Oscillator Input (XA/XB)

An on board 48 MHz XTAL is used in combination with the internal oscillator to produce an ultra-low jitter reference clock for the DSPLL. The Si5383-EVB can also accommodate an external reference clock, such as a crystal oscillator, instead of a crystal. To evaluate the device with an external crystal oscillator, C93 and C94 must be populated and XTAL Y1 removed (see figure below). A crystal oscillator's output can then be applied to SMA connectors J26 and J25. The figure below is used for a differential input such as LVPECL, LVDS, etc. See the Si5383 data sheet for more details on connecting a single ended versus differential input clock.

Note: Using an external crystal oscillator can result in reduced phase jitter performance and is not recommended for this reason.





# 5. Clock Input and Output Circuits

#### 5. Clock and Reference Input Circuits (IN0/IN0B-IN2/IN2B, IN3, IN4 and REF/REFB)

The Si5383-EVB has eight SMA connectors (REF/REFB, IN0/IN0B-IN2/IN2B) for receiving external differential signals. IN0/IN0B, IN1/ IN1B and IN2/IN2B are differential clock inputs, which single ended clocks may also be applied.

The REF/REFB differential input clock is intended to support a TCXO or OCXO, such as the included SiOCXO1-EB, which determines the Si5383's wander and holdover over performance. (Please note that this input clock is different from the optional reference clock that may be applied at XA/XB.)

All differential inputs are terminated as shown in the figure below. The only exception is that the terminating 49.9 $\Omega$  resistor for REF is not installed. This is labelled R40 on the EB in the figure below. The reason for this exception is that single-ended TCXOs and OCXOs typically cannot drive a 50  $\Omega$  load. Note that input clocks are ac-coupled and 50  $\Omega$  terminated. Single-ended clocks can be used by appropriately driving one side of the differential pair with the single-ended clock. For details on how to configure inputs as single-ended, please refer to the Si5383 data sheet.



Figure 5.1. REF/REFB Input Terminations



Figure 5.2. Differential Clock Input Terminations

In addition, the Si5383-EVB supports two SMA connectors (IN3, IN4) for receiving external single-ended LVCMOS clocks, such as PPS inputs. Each of these clocks connects to its respective Si5383 pins via a single installed 0  $\Omega$  resistor with a 4.7 K  $\Omega$  pull down resistor. Alternatively, R217, R218, R219, R220, C139, and C140 can be modified such as to attenuate a 5V swing.



Figure 5.3. IN3 and IN4, CMOS Input Terminations

#### 5.1 Clock Output Circuits (OUTx/OUTxB)

Twelve output drivers, six differential pairs (OUT0/OUT0B - OUT4/OUT4B and OUT6/OUT6B), are AC coupled to their respective SMA connectors and two output drivers are optimized for a 1 Hz/CMOS output, which is OUT5/OUT5B. If dc coupling is required, the ac coupling capacitors can be replaced with a resistor of appropriate value. The Si5383-EVB provides pads for optional output termination resistors and/or low frequency capacitors. Note that components with a schematic "NI" designation is "not installed" and are normally not populated on the Si5383-EVB and provide locations on the PCB for optional dc/ac terminations by the end user.



Figure 5.4. Output Clock Termination Circuit



Figure 5.5. OUT5 Termination Circuit

# 6. Using the Si5383 EVB and Installing ClockBuilder Pro (CB Pro) Desktop Software

#### 6.1 Installing ClockBuilder Pro (CB Pro) Desktop Software

To install the CB Pro software on any Windows 7 (or above) PC:

Go to http://www.silabs.com/CBPro and download ClockBuilder Pro software.

Installation instructions and the user's guide for ClockBuilder can be found at the download link shown above. Please follow the instructions as indicated.

Note: ClockBuilder Pro software may periodically be updated and it's recommended to allow these updates as requested. Additional tools and features, as well as frequency plan optimization can be included in updates.

#### 6.2 Connecting the EVB to Your Host PC

Once ClockBuilder Pro software is installed, connect to the EVB with a USB cable as shown below.





#### 6.3 Additional Power Supplies

The Si5383-EVB comes preconfigured with jumpers installed at JP5 in order to select the "USB" power. These jumpers, together with the components installed, configure the evaluation board to obtain all +5 V power solely through the main USB connector at J20. This setup is the default configuration and should normally be sufficient.

The general guidelines for USB power supply operation are listed below:

- Use either USB 4.0, USB 3.0 or USB 2.0 port. USB 3.0 is specified to supply 900 mA and USB 4.0 and 2.0 is 500 mA, at +5V.
- If you are working with a USB 4.0 or USB 2.0 port and you are current limited, turn off enough DUT output voltage regulators to drop the total DUT current ≤470 mA. (Note: USB 2.0 ports may supply >500 mA. Provided the nominal + 5V drops gracefully by less than 10%, the EVB will still work.)
- If you are working with a USB 4.0 or USB 2.0 and you are current limited and need all output clock drivers enabled, reconfigure the EVB to drive the DUT output voltage regulators from an external +5 power supply as follows:
  - Connect external +5 V power supply to terminal block J20 on the back side of the PCB.
  - Move the jumper at JP5 from pins 1-2 USB to pins 2-3 EXT.

#### 6.4 Inputs

A TCXO, OCXO, or frequency generator supplying 12.800 MHz (or other desired frequency) is applied to the Reference Input. Clock signal(s) are applied to the inputs and the frequency is determined when configuring using CBPro. In most cases, a 1 PPS signal is applied to IN3 and/or IN4 and should be a 3.3V CMOS signal swing. IN0, IN1, and IN2 are configured for differential inputs. See Figure 5.2 Differential Clock Input Terminations on page 7

# 6.5 Overview of ClockBuilder Pro Applications

The ClockBuilder Pro installer will install two main applications, ClockBuilder Pro Wizard and CB Pro EVB GUI:

ClockBuilder Pro Wizard - Silicon Labs							
ClockBuilder Pro WizardSILICON LABSWe Make Timing Simple							
Work With a Design	Quick Links						
Create New Design	Clock Generators & Jitter Attenuators Knowledge Base						
Open Design Project File	<u>Custom Part Number Lookup</u> <u>ClockBuilder Go iOS App</u>						
ex <u>Open Sample Design</u>	Applications Documentation						
Evaluation Board Detected Si5383 EVB Open Default Plan EVB GUI	<u>10/40/100G Line Card White Paper</u> <u>Clock Generators for Cloud Data Centers White Paper</u> <u>Optimizing Si534x Jitter Performance App Note</u> <u>SyncE and IEEE 1588 App Note</u>						
	ClockBuilder Pro Documentation						
	<u>CBPro Overview</u> Command Line Interface: <u>Overview</u> • <u>User's Guide</u> <u>Release Notes</u> • <u>Knowledge Base</u>						
۰.	Version 2.6 Built on 3/29/2016						

Figure 6.2. ClockBuilder Pro Wizard

Use the CB Pro Wizard to:

- · Create a new design
- · Review or edit an existing design
- · Create multiple designs, tools are included to merge plans and minimize register writes required to update
- · Export: create in-system programming files
- Calculate rational fractions, using tools
- Optimize frequency output configuration
- · Optimize loop filter and alarms to the application

H	lelp							
b	DUT SPI	I2C	DUT Register Edito	Regulators	All Voltages	GPIO	Status Registers	<ul> <li>Control Registers</li> </ul>
	VDD	1.9	20\/ <b>v</b> On	Voltage	Curre	nt m (	Power	Soft Reset and Calib SOFT_RST_ALL
	VDDA	1.0	On	3.047	203	mA	783 mW Read	SOFT_RST_PLLA
	VDDOO	2.5	50V 🔽 On	2.486 \	16	mA	40 mW Read	SOFT_RST_PLLB
	VDDO1 VDDO2	2.5	50V <b>v</b> On 50V <b>v</b> On	2.483 \	16 16	mA mA	40 mW Read 40 mW Read	SOFT_RST_PLLD
	VDDO3	2.5	50V 🔽 On	2.504 \	17	mA	43 mW Read	Hard Reset, Sync, Power Down
	VDDO4 VDDO5	3.3	50V <b>v</b> On 80V <b>v</b> On	2.482 \ 3.288 \	/ 16 / 7	mA mA	40 mW Read	HARD_RST
	VDDO6	2.5	50V 🔽 On	2.485 \	16	mA	40 mW Read	SYNC
All	Output	Se	lect Voltage	Total	624	mA	1.392 W Read All	
S	upplies 7	Pc	ower On Power	Off C	ompare Desig	gn Estin	ates to Measurements	FINC
								FDEC

Figure 6.3. EVB GUI

Use the EVB GUI to:

- · Download configuration to EVB's DUT (Si5383) by selecting file
- Control the EVB's regulators
- · Monitor voltage, current, and power on the EVB using the "All Voltages" tab
- · Read alarms such as verifying a locked condition, loss of input signal ,etc using the "Status Registers" tab
- · Update individual registers using the "DUT Register Editor"

#### 6.6 Common ClockBuilder Pro Work Flow Scenarios

There are three common workflow scenarios when using CB Pro and the Si5383 EVB. These workflow scenarios are:

- Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration
- · Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration
- Workflow Scenario #3: Creating a User-Generated Device Configuration
- Workflow Scenario #4: Testing a User-Created Device Configuration

Each is described in more detail in the following sections.

#### 6.7 Workflow Scenario #1: Testing a Silicon Labs-Created Default Configuration

The flow for using the EVB GUI to initialize and control a device on the EVB is as follows.

Once the PC and EVB are connected, launch ClockBuilder Pro by clicking on this icon on your PC's desktop.



Figure 6.4. ClockBuilder Pro Desktop Icon

If an EVB is detected, click on the "Open Default Plan" button on the Wizard's main menu. CB Pro automatically detects the EVB and device type.



Figure 6.5. Open Default Plan

Once you open the default plan (based on your EVB model number), a popup will appear.

Cloci	kBuilder Pro v2.6
0	Write Design to EVB? The EVB may be out-of-sync with your design. Would you like to write your design to the EVB?
	Yes No

Figure 6.6. Write Design to EVB Dialog

Select "Yes" to write the default plan to the Si5383 device mounted on your EVB. This ensures the device is completely reconfigured per the Silicon Labs default plan for the DUT type mounted on the EVB.

Si5383 Design Write	
Writing Si5383 Design to EVB	
Address 0x013E	

Figure 6.7. Writing Design Status

After CBPro writes the default plan to the EVB, click on "Open EVB GUI" as shown below.



Figure 6.8. Open EVB GUI

The EVB GUI will appear. Note all power supplies will be set to the nominal values defined in the device's default CB Pro project file created by Silicon Labs, as shown in the example session window below.

Si5383 EVB S/N C	0-00-17-70-46-EF - ClockBu	ilder Pro	_			-		
File Help								
Info DUT SPI	I2C DUT Register Editor	Regulators	All Voltages	GPIO	Status Registers		Ŧ	Control Registers
		Voltage	Current	t	Power			Soft Reset and Calibration
VDC	) 1.80V 🔽 On	1.776 V	257 m	hΑ	456 mW	Read		SOFTRESET_G
VDDA	A On	3.259 V	178 m	۱A	580 mW	Read		DSPLLA_SOFTRESET
VDDO	) 1.80V 🔽 On	1.781 V	14 m	۱A	25 mW	Read		DSPLLB_SOFTRESET
VDDO:	1.80V 🔽 On	1.791 V	14 m	hΑ	25 mW	Read		DSPLLC_SOFTRESET
VDDO2	2 1.80V 🔽 On	1.791 V	14 m	۱A	25 mW	Read		DSPLLD_SOFTRESET
VDDO3	3 1.80V 🔽 On	1.782 V	14 m	hΑ	25 mW	Read		Hard Reset, Sync, &
VDDO4	1.80V 🔽 On	1.786 V	14 m	hΑ	25 mW	Read		Power Down
VDDO:	5 1.80V 🔽 On	1.782 V	6 m	۱A	11 mW	Read		RST_REG
VDDO	5 1.80V 🔽 On	1.778 V	14 m	۱A	25 mW	Read		SYNC_REG
410	- Select Voltage	Total	525 n	nA	1.197 W	Read All		PDN: 0
Supplies	- Power On Power (	Off Co	Compare Design Estimates to Measurements				Frequency Adjust F_INC_REG	
								F_DEC_REG

Figure 6.9. EVB GUI Window

#### 6.7.1 Verify Free-Run Mode Operation

Assuming an OCXO or TCXO output has been applied to the REF/REFb input(s) and no external clocks have been connected to the INPUT CLOCK differential SMA connectors (labeled "INx/INxB"), located around the perimeter of the EVB, the DUT should now be operating in free-run mode. The DUT will be locked to the OCXO/TCXO in this case.

You can run a quick check to determine if the device is powered up and generating output clocks (and consuming power) by clicking on the Read All button highlighted above and then reviewing the voltage, current and power readings for each VDDx supply.

**Note:** Shutting the VDD and VDDA supplies Off and then On will power-down and reset the DUT. Every time you do this, to reload the Silicon Labs-created default plan into the DUT's register space, you must go back to the Wizard's main menu and select "Write Design to EVB":





Failure to do the step above will cause the device to read in a preprogrammed plan from its non-volatile memory (NVM). However, the plan loaded from the NVM may not be the latest plan recommended by Silicon Labs for evaluation.

At this point, you should verify the presence and frequencies of the output clocks (running to free-run modes from the crystal) using appropriate external instrumentation connected to the output clock SMA connectors. To verify the output clocks are toggling at the correct frequency and signal format, click on View Design Report as highlighted below.



Figure 6.11. View Design Report

Your configuration's design report will appear in a new window, as shown below. Compare the observed output clocks to the frequencies and formats noted in your default project's Design Report.

Si5383 Design Report	
esign Report	
Jesign	
I/O Power Supply. VDDA (3 3V)	
1/0 POWEL Supply. (SLSV)	
KA/XB:	
48 MHz (XTAL - Crystal)	
REF:	
12.8 MHz [ 12 + 4/5 MHz ]	
Inputs:	
INU: 25 MHz	
Standard	
DSPLL A,C	
IN1: 25 MHz	
Standard	
DSPLL A,C	
IN2: 156.25 MHz [ 156 + 1/4 MHz ]	
Standard	
DSPLL A,C	
IN3: 1 HZ	
CMOS	
DSPLL D	
DSPLI. D	
Dutputs:	
OUT0: 156.25 MHz [ 156 + 1/4 MHz ]	
Enabled, LVDS 2.5 V	
DSPLL A	
OUT1: 25 MHz	
Enabled, LVDS 2.5 V	
DSPLL A	
OUT2: 156.25 MHz [ 156 + 1/4 MHz ]	
Enabled, LVDS 2.5 V	
DITA: 25 MUT	
Frabled IVES 2.5 V	
DSPLL C	
OUT4: 156.25 MHz [ 156 + 1/4 MHz ]	
Enabled, LVDS 2.5 V	
DSPLL D	
OUT5: 1 Hz	
Enabled, LVDS 2.5 V	
DSPLL D	
OUT6: 25 MHz	
Enabled, LVDS 2.5 V	
DSPLL D	
Frequency Plan	
Copy to Clipboard Save Report	Close

#### Figure 6.12. Design Report Window

# 6.7.2 Verify Locked Mode Operation

Assuming you connect the correct input clocks to the EVB (as noted in the Design Report shown above), the DUT on your EVB will be running in "locked" mode. LED's D7, D8, D18 and D19 will be off when the associated PLL is locked. The EVB GUI "Status Register" page can be selected to also check locked status as well as other alarms.

#### 6.8 Workflow Scenario #2: Modifying the Default Silicon Labs-Created Device Configuration

To modify the "default" configuration using the CB Pro Wizard, click on any of the underlined fields below the header "Edit Configuration with Wizard". You can also pull down on the "Design ID & Notes" menu and select a design step.

Si5383 EVB Default Configuration - ClockBuilder Pro										
ClockBuilder Pro v2.6 🍫 (standard frequency planner) (no	ClockBuilder Pro v2.6 🍫 (standard frequency planner) (no setting overrides) SILICON LABS									
Step 1 of 16 - Design ID & Notes ▼ Configuring Si5383 Rev C										
Default plan for Si5383 EVB has been loaded. You can make edits to t	he EVB's configuration using the interactive Wizard.									
Edit Configuration with Wizard Design ID & Notes • Revision • Host Interface • XAXB & REF • Inputs • Input Clock Select • Outputs • DCO • Output Drivers • DSPLL • LOS • OOF • LOL • INTR	Evaluation Board Detected Si5383 EVB S/N00-00-17-70-22-94 Write Design to EVB Open EVB GUI									
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.									
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> <u>representative</u> to request access to documentation.									
Silicon Labs Cloud Services You can create a custom part number for your design, which can be used to order factory pre-programmed devices. Or request a phase noise report for this design.	Ask for Help Have a question about your design? Click here to get assistance.									
Frequency Plan Valid 🕢 Design OK 🛞 Pd: 1.161 W, Tj: 95 °C	Home Close									

Figure 6.13. Edit Configuration with Wizard

You will now be taken to the Wizard's step-by-step menus to allow you to change any of the default plan's operating configurations. Note, any changes made to any of these menu's will require that a "Write to EVB" be selected.



Figure 6.14. Design ID and Notes

Note you can view the icon on the lower left hand corner of the menu to confirm if your frequency plan is valid. This example shows modifications made to the loop BW, ramp rate and entry into holdover values which can be tailored to the application. After making your desired changes, you can click on "Write to EVB" to update the DUT to reconfigure your device in real time. The Design Write status window will appear each time you make a change.

🗱 Si5383 Design Write	
Writing Si5383 Design to EVB	
Address 0x013E	

Figure 6.15. Si5383 Design Write

#### 6.9 Workflow Scenario #3: Testing a User-Created Device Configuration

To test a previously created user configuration, open the CB Pro Wizard by clicking on the icon on your desktop and then selecting "Open Design Project File".



#### Figure 6.16. Open Design Project File

Locate your CB Pro design file (\*.slabtimeproj or \*.sitproj file) in the Windows file browser.

CB O	pen CB	Pro Project File		_	Accessibility Inc.					23
0	9-	🜗 « Program F	iles	<ul> <li>ClockBuilder Pro</li> </ul>		<b>-</b> ∮	Searc	h ClockBuild	er Pro	٩
Or	ganize	<ul> <li>New folder</li> </ul>								0
	Â	Name	×	Date modified	Туре	Size				
1		퉬 bin		1/18/2016 11:19 AM	File folder					
	) E	퉲 СЦ		1/18/2016 11:19 AM	File folder					
0	2	鷆 Etc		1/18/2016 11:19 AM	File folder					
		퉬 USBXpressDri	iver-ClockBuilder-Program	1/18/2016 11:19 AM	File folder					
		퉬 USBXpressDri	iver-Legacy	1/18/2016 11:19 AM	File folder					
		USBXpressDri	iver-Si538x4x-EVB	1/18/2016 11:19 AM	File folder					
1		Bi5383-RevC-	Project	1/19/2016 10:20 AM	Silicon Labs Timin		11 KB			
6	2									
	-									
	-									
	-									
1										
		File nar	me: Si5383-RevC-Project			•	Silicon	Labs Timing	y Project	-
									Care	
							Up	en	Canci	ei

Figure 6.17. Browse to Project File

Select "Open" to load the selected file and then "Yes" when the WRITE DESIGN to EVB popup appears:



Figure 6.18. Write Design to EVB Dialog

The progress bar will be launched. Once the new design project file has been written to the device, verify the presence and frequencies of your output clocks and other operating configurations using external instrumentation.

# 6.10 Exporting the Register Map File for Device Programming by a Host Processor

You can also export your configuration to a file format suitable for in-system programming by selecting "Export" as shown below:

CB Si5383-RevC-Project - ClockBuilder Pro	
ClockBuilder Pro v2.4.11 🍫 (standard frequency planner)	(no setting overrides) SILICON LABS
Design Dashboard 🔻	Configuring Si5383 Rev C
Loaded Si5383 design from C:\Program Files\Silicon Laboratories	s\ClockBuilder Pro\Si5383-RevC-Project.slabtimeproj.
Edit Configuration with Wizard Design ID & Notes · Revision · XAXB & REF · Inputs · Input Clock Select · Outputs · DCO · Output Drivers · DSPLL · LOS · OOF · LOL · INTR	Evaluation Board Detected Si5383 EVB S/N 00-00-17-70-5B-55 Write Design to EVB Open EVB GUI
Save Design to Project File Your configuration is stored to a project file, which can be opened in ClockBuilder Pro at a later time.	You can export your configuration to a format suitable for in-system programming.
Design Report & Datasheet Addendum You can view a <u>design report (text)</u> or create a <u>draft datasheet addendum (PDF)</u> for your design.	Documentation Technical documentation is currently restricted for this product. Please contact your <u>Silicon Labs sales</u> <u>representative</u> to request access to documentation.
Create Custom Part Number With just a few clicks, you can order factory pre- programmed devices based on your configuration.	Ask for Help Have a question about your design? Click here to get assistance.
▶ Frequency Plan Valid   Design OK   Pd: 1.152 W, Tj: 95 °C	Home Close

# Figure 6.19. Export Register Map File

You can now write your device's complete configuration to file formats suitable for in-system programming.

Fi	irmware Image Register File Settings File Multi-Project Register/Settings Regmap
(	About Register Export
	This export will contain the registers that need to be written (in sequence) to the Si538x/4x device to achieve your design/configuration.
	Please refer to the Si538x/4x Family Reference Manual for information on register addressing and how to write the data contained within this export.
	A command line version of this tool is available. Type <b>CBProProjectRegistersExport</b> help from a command prompt to learn more.
ſ	Options
	Export Type:
	Omma Separated Values (CSV) File Each line in the file is an address,data pair in hexadecimal format. A comma separates the address and data fields.
	C Code Header File The register write sequence is expressed in C code via an array of address,data pairs. This can be used directly in firmware code.
	🗹 Include summary header
	If checked, an informational header will be included at the top of the file. Each line in the header will be prefixed by the # character. The header will contain some basic information about the design, tool, and a timestamp.
	✓ Include pre- and post-write control register writes
	Certain control registers must be written before and after writing the volatile configuration registers. This ensures the device is stable during configuration download and resumes normal operation after the download is complete. You can turn inclusion of this sequence off if your host system is managing this process already.
	I am targeting pre-production samples 🕼
	Preview Export Save to File

Figure 6.20. Export Settings

# 7. Writing a New Frequency Plan or Device Configuration to Non-Volatile Flash Memory (NVM)

Note: Writing a configuration into the EVB from ClockBuilder Pro can be done an unlimited number of times.

# 8. Serial Device Communications (Si5383<->MCU)

# 8.1 On-Board I<sup>2</sup>C Support

The MCU on-board the Si5383-EVB communicates with the Si5383 device through an I2C interface. The MCU is the master and the Si5383 device is the slave. It is recommended to use the Si5383 EVB along with CBPro software and the USB cable supplied as the easiest and quickest method to power up, communicate, and evaluate.

#### 8.2 External I<sup>2</sup>C Support

I2C can be supported if driven from an external I2C controller. The serial interface signals between the MCU and the Si5383 pass through shunts loaded on header J48. These jumper shunts must be installed in J48 for normal EVB operation using I<sup>2</sup>C with CBPro. If testing of I2C operation via external controller is desired, the shunts in J48 can be removed thereby isolating the on-board MCU from the Si5383 device. An external I2C controller connected to the Si5383 side of J48 can then communicate to the Si5383 device. For more information on I2C signal protocol, please refer to the Si5383 reference manual.

The figure below illustrates the J48 header schematic. J48 even-numbered pins (2,4) connect to the Si5383 device and the odd-numbered pins (1, 3) connect to the MCU. Once the jumper shunts have been removed from J48, I2C operation should use J48 pin 2 (DUT\_SDA\_SDIO) as the I2C SDA and J48 pin 4 (DUT\_SCLK) as the I2C SCLK.



Figure 8.1. Serial Communications Header J48

# 9. Si5383-EVB Schematic and Bill of Materials (BOM)

The Si5383 EVB Schematic and Bill of Materials (BOM) can be found online at:http://www.silabs.com/products/clocksoscillators/pages/ si538x-4x-evb.aspx

Note: Please be aware that Si5383-EVB schematic is in Orcad Capture hierarchical format and not in a typical "flat" schematic format.



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