FGM230S Proprietary SiP Module Data Sheet

The FGM230S is a system-in-package (SiP) module for Proprietary wireless connectivities built for the performance, security, and energy demands of Proprietary applications.

Based on the EFR32FG23 SoC, it delivers robust RF performance, long-range, industry-leading security features, low-current consumption, a rich set of MCU peripherals, and ample memory, all in a 6.5 x 6.5 mm package.

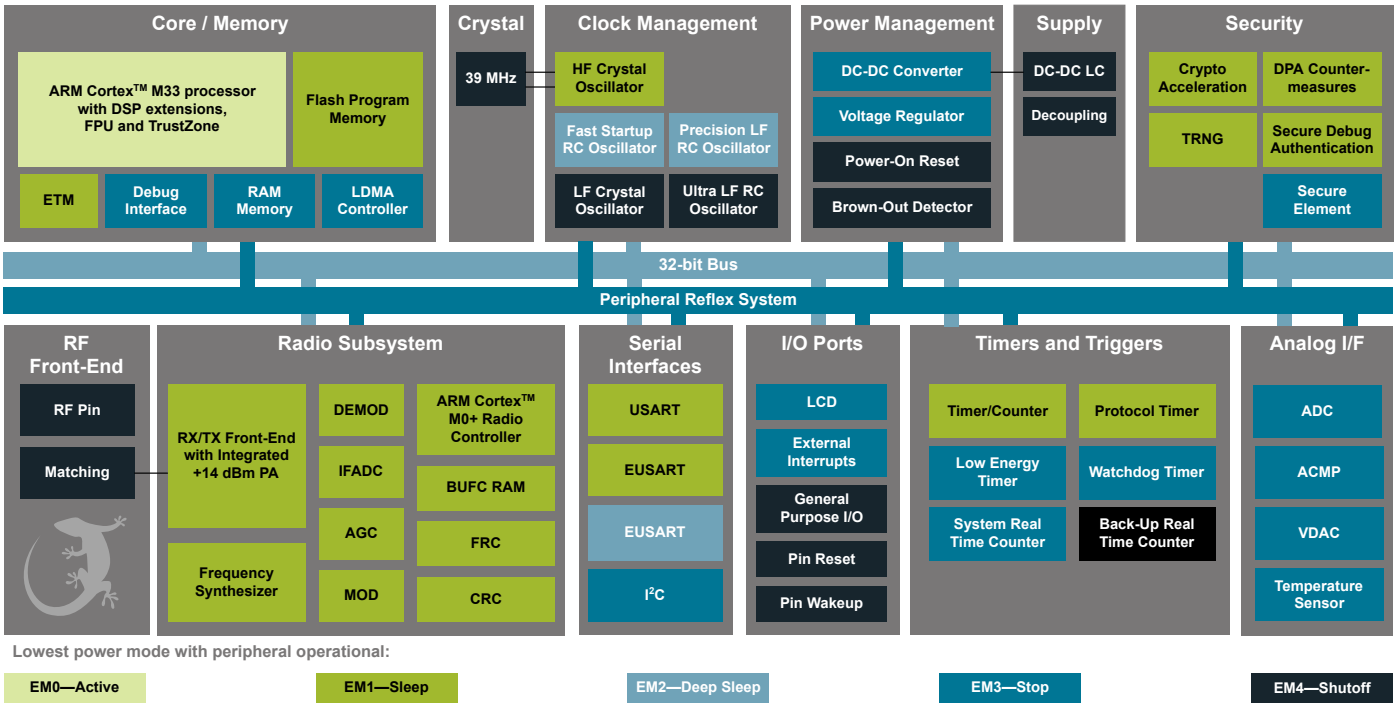
The FGM230S is a complete solution supported by powerful and fully-upgradeable software, advanced development and debugging tools, and documentation that will simplify and minimize the development cycle, certification process, and deployment of your end-product, helping to accelerate its time-to-market significantly.

The FGM230S is targeted for a broad range of applications, including:

- Metering
- Home and Building Automation and Security
- Industrial Automation
- Street Lighting

KEY FEATURES

- Proprietary uncertified connectivity
- RF pin for external antenna
- +14 dBm TX power
- -109.8 dBm RX sensitivity @100 kbps
- 32-bit ARM Cortex-M33 core at 39 MHz
- 512/64 kB of Flash/RAM memory
- Advanced security features
- Rich set of MCU peripherals
- Integrated DC-DC converter
- 34 GPIO pins
- -40 to 85 °C
- 6.5 mm x 6.5 mm



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1. Features

- **Supported Protocols**
  - Proprietary, WM-BUS, Connect
- **Wireless System-on-Chip**
  - 868 MHz and 915 MHz radio
  - TX power up to +14 dBm
  - 32-bit ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 512 kB flash program memory
  - 64 kB RAM data memory
  - Embedded Trace Macrocell (ETM) for advanced debugging
- **Receiver Performance**
  - -109.9 dBm sensitivity at 9.6 kbps FSK, 868.42 MHz
  - -110 dBm sensitivity at 40 kbps FSK, 868.4 MHz
  - -108.6 dBm sensitivity at 100 kbps GFSK, 869.85 MHz
  - -109.3 dBm sensitivity at 9.6 kbps FSK, 908.42 MHz
  - -109.7 dBm sensitivity at 40 kbps FSK, 908.4 MHz
  - -108.1 dBm sensitivity at 100 kbps GFSK, 916 MHz
  - -109.8 dBm sensitivity at 100 kbps O-QPSK, 912 MHz
- **Current Consumption**
  - 4.1 mA RX current at 9.6 kbps FSK, 868.42 MHz
  - 4.1 mA RX current at 100 kbps GFSK, 869.85 MHz
  - 4.1 mA RX current at 9.6 kbps FSK, 908.4 MHz
  - 4.1 mA RX current at 100 kbps GFSK, 916 MHz
  - 4.6 mA RX current at 100 kbps O-QPSK, 912 MHz
  - 10.7 mA TX current at 0 dBm, 916 MHz
  - 20.8 mA TX current at +10 dBm, 916 MHz
  - 30.0 mA TX current at +14 dBm, 916 MHz
  - 26 µA/MHz in Active Mode (EM0) at 39.0 MHz
  - 1.5 µA in Deep Sleep (EM2) at 64 kB RAM retention and RTC running from LFRCO
  - 0.7 µA in Shutoff Mode (EM4)
- **Operating Range**
  - 1.8 to 3.8 V
  - -40 to +85°C
- **Dimensions**
  - 6.5 mm x 6.5 mm
- **Security**
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Boot (Root of Trust Secure Loader)
  - Secure Debug Unlock
  - DPA Countermeasures
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
- **MCU Peripherals**
  - 12-bit 1 Msps or 16-bit 76.9 ksps SAR Analog to Digital Converter (ADC)
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - Low-Energy Sensor Interface (LESENSE)
  - 34 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 2 × Watchdog Timer
  - 3× Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
  - 1× Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
  - 2 × I^2C interface with SMBus support
  - Integrated Low-Energy LCD Controller supporting up to 80 segments
  - Die temperature sensor

2. Ordering Information

Table 2.1. FGM230S Ordering Part Numbers

Ordering Code	TX Power	Freq Band	Antenna	Flash (kB)	RAM (kB)	Security	GPIO	Temp Range	Carrier
FGM230SA27HGN3	+14 dBm	Sub-GHz	RF pin	512	64	Vault-Mid	34	-40 to 85 °C	Tray
FGM230SB27HGN3	+14 dBm	Sub-GHz	RF pin	512	64	Vault-High	34	-40 to 85 °C	Tray

See Section 4.6 Sub-GHz RF Transceiver Characteristics of the Electrical Specifications for maximum TX power figures.

FGM230S modules are not pre-programmed with a bootloader.

Throughout this document, the modules may be referred to by their product family name (FGM230S) or by their full ordering code as seen in the table above.

The evaluation and development radio board **FGM230-RB4328A** (Vault-High) is available for FGM230S. The **FGM230-RB4328B** (Vault-Mid) is NRND.

3. System Overview

3.1 Block Diagram

The FGM230S module is a highly-integrated, high-performance system in a package with all the hardware components needed to enable Sub-GHz wireless connectivity and support robust networking capabilities via proprietary protocols.

Built around the EFR32FG23 Wireless Gecko SoC, the FGM230S includes a 50 Ω RF pin to attach an external antenna, a matching network optimized for transmit power efficiency, supply decoupling and filtering components, an LC tank for DCDC conversion, and a 39 MHz crystal.

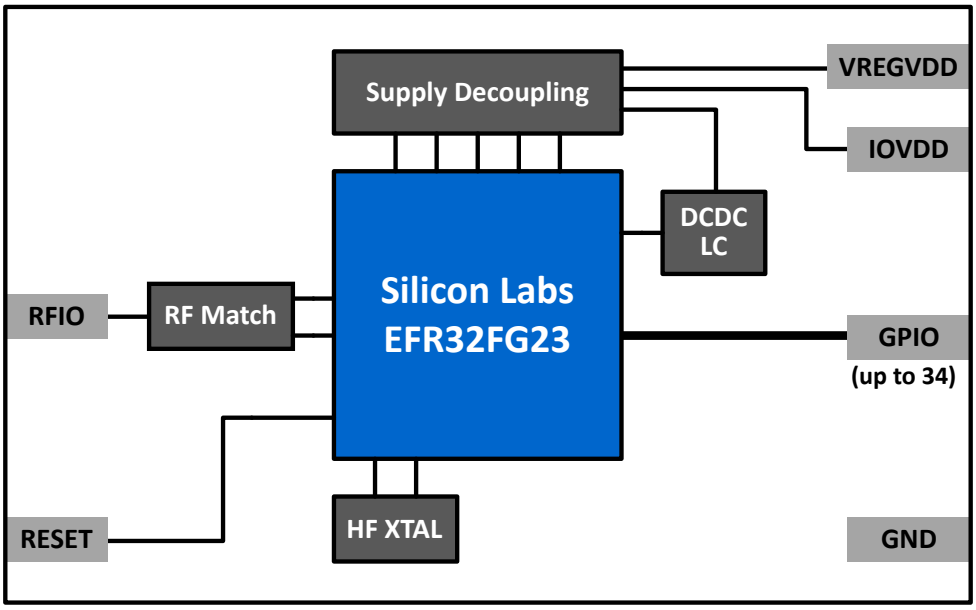


Figure 3.1. FGM230S Block Diagram

3.2 EFR32FG23 SoC

The EFR32FG23 SoC features a 32-bit ARM Cortex M33 core, a Sub-GHz high-performance radio, 512 kB of Flash memory, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. Consult the EFR32xG23 Reference Manual and the EFR32FG23 Data Sheet for details.

3.3 Antenna

The FGM230S modules include a 50 Ω-matched RFIO pin to attach an external antenna to the module.

3.4 Power Supply

The nominal supply level of the FGM230S is 3.3 V, but due to its integrated DCDC converter and built-in LDOs, the device can operate over a supply range of 1.8—3.8 V.

Only a few external decoupling capacitors are required (see Reference Diagrams). Since all smaller caps are integrated in the module, there is no need for fast decoupling externally. L and C for the DCDC converter are integrated in the module as well.

3.5 Security

FGM230S modules support one of two levels in the Security Portfolio offered by Silicon Labs: Secure Vault Mid or Secure Vault High.

Secure Vault is a collection of technologies that deliver state-of-the-art security and upgradability features to protect and future-proof IoT devices against costly threats, attacks and tampering. A dedicated security CPU enables the Secure Vault functions and isolates cryptographic functions and data from the Cortex-M33 core. FGM230SB part numbers support Secure Vault High and FGM230SA part numbers support Secure Vault Mid.

Table 3.1. Security Features and Levels

Feature	Secure Vault Mid	Secure Vault High
Secure Boot with Root of Trust and Secure Loader (RTSL)	X	X
Cryptographic Accelerator	X	X
True Random Number Generator (TRNG)	X	X
Secure Debug with Lock/Unlock	X	X
DPA Countermeasures	X	X
Secure Key Management with PUF		X
Anti-Tamper		X
Secure Attestation		X

3.5.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.5.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations, and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192, P-256, P-384, and P-521 for ECDH (Elliptic Curve Diffie-Hellman) key derivation, and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm) sign and verify operations.

Secure Vault also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling) and PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.5.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.5.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.5.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.5.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.5.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.5.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

3.6 Memory Map

The FGM230S memory map is shown in the figures below.

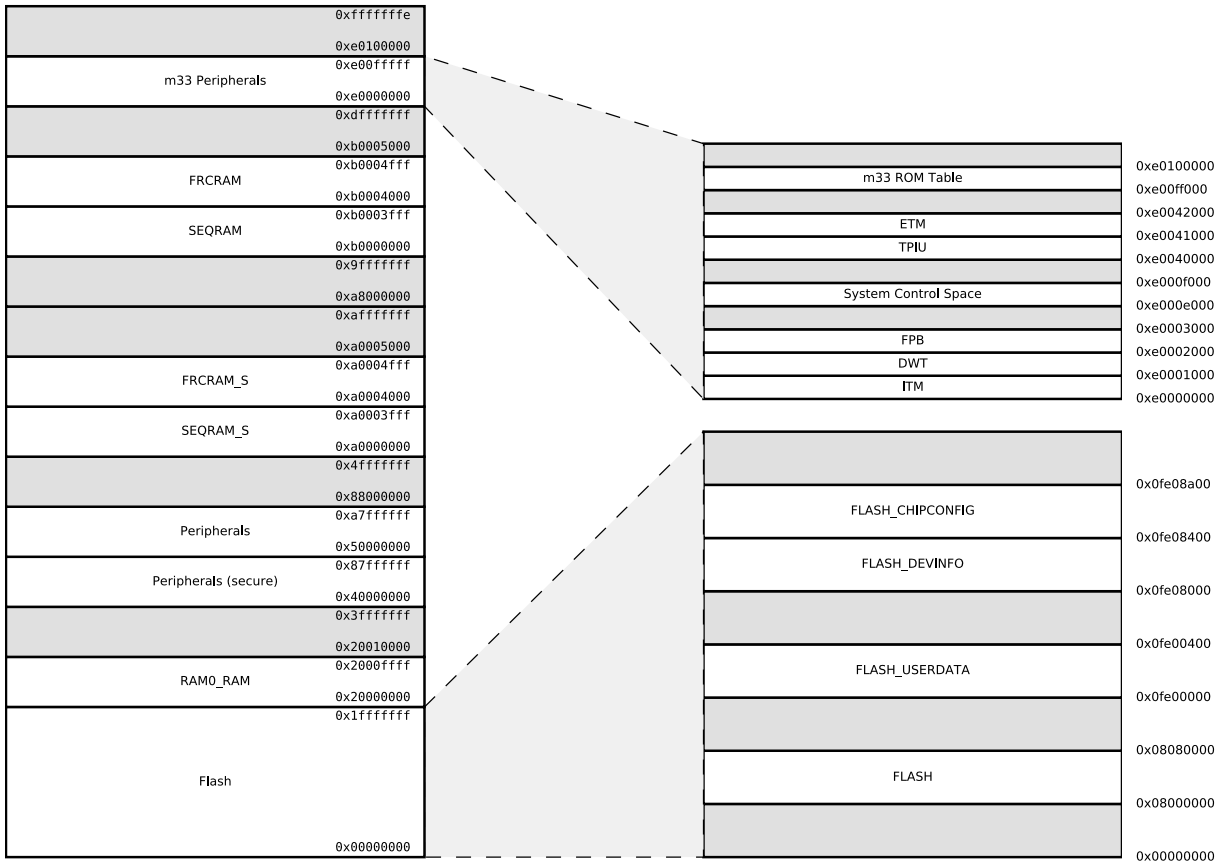


Figure 3.2. FGM230S Memory Map — Core Peripherals and Code Space

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and all supplies at 3.3 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.2 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+105	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin[1]	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
DC voltage on RESETn pin[2]	V_{RESETn}		-0.3	—	3.8	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. When operating as an LCD driver, the output voltage on a GPIO may safely exceed this specification. The pin output voltage may be up to 3.8 V in this case.
2. The RESETn pin has a pull-up device to the internally-regulated DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VREGVDD when DC-DC is inactive. For minimum leakage, it is recommended to not drive RESETn high, and instead rely on the internall pull-up.

4.3 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A		-40	—	+85	°C
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.8	3.3	3.8	V
VREGVDD operating supply voltage	$V_{VREGVDD}$		1.8	3.3	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE1, MODE = WS1	—	—	39	MHz
		VSCALE1, MODE = WS0	—	—	20	MHz
PCLK frequency	f_{PCLK}	VSCALE1	—	—	39	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE1	—	—	39	MHz
HCLK Radio frequency	$f_{HCLKRADIO}$	VSCALE1	—	39.0	—	MHz

4.4 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air (JESD51-2A)/2L board (JESD51-3)	—	126.8	—	°C/W
		Still Air (JESD51-2A)/4L board (JESD51-5, JESD51-7)	—	99.4	—	°C/W
Thermal Resistance, Junction to Board	Ψ_{JB}	Still Air (JESD51-2A)/2L board (JESD51-3)	—	57.1	—	°C/W
		Still Air (JESD51-2A)/4L board (JESD51-5, JESD51-7)	—	57.4	—	°C/W
Thermal Resistance, Junction to Top Center	Ψ_{JT}	Still Air (JESD51-2A)/2L board (JESD51-3)	—	0.92	—	°C/W
		Still Air (JESD51-2A)/4L board (JESD51-5, JESD51-7)	—	1.1	—	°C/W
Thermal Resistance, Junction to Case	Θ_{JC}	Simulation environment per JESD51-14	—	24.1	—	°C/W
Thermal Resistance, Junction to Board	Θ_{JB}	Junction to Board (JESD51-8/4L board (JESD51-5, JESD51-7)	—	42.5	—	°C/W

4.5 Current Consumption

4.5.1 MCU Current Consumption at 3.3 V input

Unless otherwise indicated, typical conditions are: VREGVDD = IOVDD = 3.3V. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. MCU Current Consumption at 3.3 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	39 MHz crystal, CPU running Prime from flash	—	27	—	µA/MHz
		39 MHz crystal, CPU running while loop from flash	—	26	—	µA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	36	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	39 MHz crystal	—	18	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	64 kB RAM and full Radio RAM retention, RTC running from LFXO	—	1.5	—	µA
		64 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	1.5	—	µA
Current consumption in EM4 mode	I_{EM4}	BURTC with LFRCO	—	0.7	—	µA
Current consumption for retained RAM bank in EM2 or EM3	I_{RAM}	Per 16 kB RAM bank	—	0.1	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	0.85	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1]	I_{PD0C_VS}		—	0.13	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1]	I_{PD0D_VS}		—	0.98	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1]	I_{PD0E_VS}		—	0.06	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See the "Power Domains" section in the SoC datasheet for a list of the peripherals in each power domain.

4.5.2 MCU Current Consumption at 1.8 V input

Unless otherwise indicated, typical conditions are: VREGVDD = IOVDD = 1.8 V. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU Current Consumption at 1.8 V input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	39 MHz crystal, CPU running Prime from flash	—	44	—	µA/MHz
		39 MHz crystal, CPU running while loop from flash	—	42	—	µA/MHz
		39 MHz crystal, CPU running CoreMark loop from flash	—	58	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	39 MHz crystal	—	29	—	µA/MHz
Current consumption in EM2 mode, VSCALE0	I_{EM2_VS}	64 kB RAM and full Radio RAM retention, RTC running from LFXO	—	2.2	—	µA
		64 kB RAM and full Radio RAM retention, RTC running from LFRCO	—	2.2	—	µA
Current consumption for retained RAM bank in EM2 or EM3	I_{RAM}	Per 16 kB RAM bank	—	0.15	—	µA
Current consumption in EM4 mode	I_{EM4}	BURTC with LFRCO	—	0.52	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	384	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0B is enabled[1]	I_{PD0B_VS}		—	1.38	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0C is enabled[1]	I_{PD0C_VS}		—	0.21	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0D is enabled[1]	I_{PD0D_VS}		—	1.59	—	µA
Additional current in EM2 or EM3 when any peripheral in PD0E is enabled[1]	I_{PD0E_VS}		—	0.10	—	µA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See the "Power Domains" section in the SoC datasheet for a list of the peripherals in each power domain.

4.5.3 Radio Current Consumption at 3.3 V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = IOVDD = 3.3 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. Radio Current Consumption at 3.3 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P[1]	I_{RX_ACTIVE}	f = 868.4 MHz, 2-FSK, 40 kbps	—	4.1	—	mA
		f = 868.42 MHz, 2-FSK, 9.6 kbps	—	4.1	—	mA
		f = 869.85 MHz, 2-GFSK, 100 kbps	—	4.1	—	mA
		f = 908.42 MHz, 2-FSK, 9.6 kbps	—	4.1	—	mA
		f = 908.4 MHz, 2-FSK, 40 kbps	—	4.1	—	mA
		f = 916 MHz, 2-GFSK, 100 kbps	—	4.1	—	mA
		f = 912 MHz, O-QPSK 100 kbps	—	4.6	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P[1]	I_{RX_LISTEN}	f = 868.4 MHz, 2-FSK, 40 kbps	—	4.2	—	mA
		f = 868.42 MHz, 2-FSK, 9.6 kbps	—	4.2	—	mA
		f = 869.85 MHz, 2-GFSK, 100 kbps	—	4.2	—	mA
		f = 908.42 MHz, 2-FSK, 9.6 kbps	—	4.2	—	mA
		f = 908.4 MHz, 2-FSK, 40 kbps	—	4.2	—	mA
		f = 916 MHz, 2-GFSK, 100 kbps	—	4.2	—	mA
		f = 912 MHz, O-QPSK 100 kbps	—	4.5	—	mA
Current consumption in transmit mode	I_{TX}	f = 868.42 MHz, CW, 0 dBm output power	—	10.5	—	mA
		f = 868.42 MHz, CW, 4 dBm output power	—	13.3	—	mA
		f = 868.42 MHz, CW, 10 dBm output power	—	20.5	—	mA
		f = 868.42 MHz, CW, 14 dBm output power	—	30.1	—	mA
		f = 916 MHz, CW, 0 dBm output power	—	10.7	—	mA
		f = 916 MHz, CW, 4 dBm output power	—	13.5	—	mA
		f = 916 MHz, CW, 10 dBm output power	—	20.8	—	mA
		f = 916 MHz, CW, 14 dBm output power	—	30.0	—	mA

Note:

1. EM1P operation is 0.22 mA lower than EM1 operation

4.5.4 Radio Current Consumption at 1.8 V

RF current consumption measured with MCU in EM1, HCLK = 39.0 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VREGVDD = IOVDD = 1.8 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. Radio Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception, VSCALE1, EM1P[1]	I_{RX_ACTIVE}	f = 868.4 MHz, 2-FSK, 40 kbps	—	6.8	—	mA
		f = 868.42 MHz, 2-FSK, 9.6 kbps	—	6.8	—	mA
		f = 869.85 MHz, 2-GFSK, 100 kbps	—	6.8	—	mA
		f = 908.42 MHz, 2-FSK, 9.6 kbps	—	6.8	—	mA
		f = 908.4 MHz, 2-FSK, 40 kbps	—	6.8	—	mA
		f = 916 MHz, 2-GFSK, 100 kbps	—	6.8	—	mA
		f = 912 MHz, O-QPSK 100 kbps	—	7.5	—	mA
Current consumption in receive mode, listening for packet, VSCALE1, EM1P[1]	I_{RX_LISTEN}	f = 868.4 MHz, 2-FSK, 40 kbps	—	6.9	—	mA
		f = 868.42 MHz, 2-FSK, 9.6 kbps	—	6.9	—	mA
		f = 869.85 MHz, 2-GFSK, 100 kbps	—	6.9	—	mA
		f = 908.42 MHz, 2-FSK, 9.6 kbps	—	6.9	—	mA
		f = 908.4 MHz, 2-FSK, 40 kbps	—	6.9	—	mA
		f = 916 MHz, 2-GFSK, 100 kbps	—	6.9	—	mA
		f = 912 MHz, O-QPSK 100 kbps	—	7.4	—	mA
Current consumption in transmit mode	I_{TX}	f = 868.42 MHz, CW, 0 dBm output power	—	16.4	—	mA
		f = 868.42 MHz, CW, 4 dBm output power	—	20.8	—	mA
		f = 868.42 MHz, CW, 10 dBm output power	—	32	—	mA
		f = 868.42 MHz, CW, 14 dBm output power	—	47	—	mA
		f = 916 MHz, CW, 0 dBm output power	—	16.8	—	mA
		f = 916 MHz, CW, 4 dBm output power	—	21.1	—	mA
		f = 916 MHz, CW, 10 dBm output power	—	32.5	—	mA
		f = 916 MHz, CW, 14 dBm output power	—	46.8	—	mA

Note:

1. EM1P operation is 0.35 mA lower than EM1 operation

4.6 Sub-GHz RF Transceiver Characteristics

4.6.1 RF Transmitter Characteristics

4.6.1.1 868 MHz Band +14 dBm RF Transmitter Characteristics

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = IOVDD = 3.3 V, Crystal frequency= 39.0 MHz. RF center frequency 868.4 MHz.

Table 4.8. 868 MHz Band +14 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		863	—	870	MHz
Maximum TX Power	$POUT_{MAX}$	14 dBm output power[1][2]	13.9	14.3	14.5	dBm
Minimum active TX Power	$POUT_{MIN}$		-24.2	-23.9	—	dBm
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, T = 25 °C	—	0.03	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	T_A = -40 to +85 °C	—	0.3	0.9	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T = 25 °C	—	0.05	0.5	dB
Spurious emissions of harmonics, Conducted measurement, P_{OUT} = +14 dBm, 868.4 MHz	$SPUR_{HARM\_ETSI}$	(frequencies above 1 GHz)[3]	—	-52	—	dBm
Spurious emissions out-of-band, Conducted measurement, P_{OUT} = +14 dBm, 868.4 MHz	$SPUR_{OOB\_ETSI}$	Per ETSI EN 300-220, Section 7.8.2.1 (47-74 MHz, 87.5-118 MHz, 174-230 MHz, and 470-862 MHz)	—	-65	—	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (other frequencies below 1 GHz)	—	-59	—	dBm
		Per ETSI EN 300-220, Section 7.8.2.1 (frequencies above 1 GHz)	—	-59	—	dBm

Note:

1. The output power level can be adjusted to suit specific regulatory requirements for the region in which the device is used.
2. The transmit power for the 863 MHz to 870 Band MHz is normally limited to +14 dBm.
3. Spurious emission limits per EN 300-220-1 v3.1.1 5.9.2

4.6.1.2 915 MHz Band 0 dBm RF Transmitter Characteristics

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = IOVDD = 3.3 V, Crystal frequency= 39.0 MHz. RF center frequency 908.4 MHz.

Table 4.9. 915 MHz Band 0 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Maximum TX Power	$POUT_{MAX}$	0 dBm output power[1][2]	-0.2	0.11	0.54	dBm
Minimum active TX Power	$POUT_{MIN}$		-24.5	-24.2	—	dBm
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, T = 25 °C	—	0.03	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	T_A = -40 to +85 °C	—	1.25	—	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T_A = 25 °C	—	0.02	—	dB
Spurious emissions of harmonics at 0 dBm output power, Conducted measurement, Test Frequency = 908.4 MHz	$SPUR_{HARM\_FCC}$	In non-restricted bands, per FCC 47 CFR §15.231[3]	—	-54	-20	dBc
		In restricted bands, per FCC 47 CFR §15.205 & §15.209[4][5]	—	-54	-41.2	dBm
Spurious emissions out-of-band at 0 dBm output power, Conducted measurement, Test Frequency = 908.4 MHz	$SPUR_{OOB\_FCC}$	In non-restricted bands, per FCC 47 CFR §15.231[3]	—	-61	-20	dBc
		In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[4] [5]	—	-69	-55.2	dBm
		In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5]	—	-69	-51.7	dBm
		In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5]	—	-67	-49.2	dBm
		In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[4] [5]	—	-59	-42	dBm

Note:

1. The transmit power for the 902 MHz to 928 Band MHz is normally limited to +0 dBm when frequency hopping or DSSS is not used.
2. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 0 dBm.
3. FCC Title 47 CFR Part 15 Section 15.231 Periodic operation in the band 40.66-40.70 MHz and above 70 MHz.
4. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
5. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.

4.6.1.3 915 MHz Band +14 dBm RF Transmitter Characteristics

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = IOVDD = 3.3 V, Crystal frequency= 39.0 MHz. RF center frequency 912 MHz.

Table 4.10. 915 MHz Band +14 dBm RF Transmitter Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Maximum TX Power	$POUT_{MAX}$	14 dBm output power[1]	14.7	14.8	14.9	dBm
Minimum active TX Power	$POUT_{MIN}$		-24.5	-24.3	—	dBm
Output power variation vs supply at $POUT_{MAX}$	$POUT_{VAR\_V}$	1.8 V < $V_{VREGVDD}$ < 3.3 V, T = 25 °C	—	0.02	—	dB
Output power variation vs temperature, peak to peak	$POUT_{VAR\_T}$	T_A = -40 to +85 °C	—	0.5	1	dB
Output power variation vs RF frequency	$POUT_{VAR\_F}$	T_A = 25 °C	—	0.1	0.6	dB
Spurious emissions of harmonics at +14 dBm output power, Conducted measurement, Test Frequency = 912 MHz	$SPUR_{HARM\_FCC\_14}$	In restricted bands, per FCC 47 CFR §15.205 & §15.209[23]	—	-52	-51	dBm
		In non-restricted bands, per FCC 47 CFR §15.231[4]	—	-62	-20	dBc
Spurious emissions out-of-band at +14 dB output power, Conducted measurement, Test Frequency = 912 MHz	$SPUR_{OOB\_FCC\_14}$	In non-restricted bands, per FCC 47 CFR §15.231[4]	—	-69	-20	dBc
		In restricted bands (30-88 MHz),per FCC 47 CFR §15.205 & §15.209[2 3]	—	-68.3	-55.2	dBm
		In restricted bands (88-216 MHz), per FCC 47 CFR §15.205 & §15.209[2 3]	—	-68.3	-51.7	dBm
		In restricted bands (216-960 MHz), per FCC 47 CFR §15.205 & §15.209[2 3]	—	-66	-49.2	dBm
		In restricted bands (>960 MHz), per FCC 47 CFR §15.205 & §15.209[2 3]	—	-56.4	-41.2	dBm

Note:

1. The maximum output power can go up to the maximum rating. Emissions are tested with the output power set to 14 dBm.
2. FCC Title 47 CFR Part 15 Section 15.205 Restricted bands of operation.
3. FCC Title 47 CFR Part 15 Section 15.209 Radiated emission limits; general requirements.
4. FCC Title 47 CFR Part 15 Section 15.231 Periodic operation in the band 40.66-40.70 MHz and above 70 MHz.

4.6.2 RF Receiver Characteristics

4.6.2.1 868 MHz Band RF Receiver Characteristics

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = IOVDD = 3.3 V, Crystal frequency= 39.0 MHz. RF center frequency 868.4 MHz.

Table 4.11. 868 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		863	—	870	MHz
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Desired is reference 100 kbps GFSK signal[1]	—	—	10.0	dBm
Sensitivity	SENS	Desired is reference 9.6 kbps 2FSK signal[2], 1% PER, frequency = 868.42 MHz, T ≤ 85 °C	—	-109.9	—	dBm
		Desired is reference 40 kbps 2FSK signal[3], 1% PER, frequency = 868.4 MHz, T ≤ 85 °C	—	-110	—	dBm
		Desired is reference 100 kbps GFSK signal[1], 1% PER, frequency = 869.85 MHz, T ≤ 85 °C	—	-108.6	—	dBm
Image rejection, Interferer is CW at image frequency	IR	Desired is reference 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, 1% PER, frequency = 868.42 MHz	—	49.6	—	dB
		Desired is reference 40 kbps 2FSK signal[3] at 3dB above sensitivity level, 1% PER, frequency = 868.4 MHz	—	49.8	—	dB
		Desired is 100kbps GFSK signal[1] at 3dB above sensitivity level, 1% PER, frequency = 869.85 MHz	—	48.1	—	dB
Blocking selectivity, 1% PER. Desired is 9.6 kbps 2FSK signal[2] at 3 dB above sensitivity level, frequency = 868.42 MHz	$BLOCK_{9p6}$	Interferer CW at Desired ± 1 MHz	—	59.4	—	dB
		Interferer CW at Desired ± 2 MHz	—	64.2	—	dB
		Interferer CW at Desired ± 5 MHz	—	73.7	—	dB
		Interferer CW at Desired ± 10 MHz	—	79.6	—	dB
		Interferer CW at Desired ± 100 MHz	—	83.3	—	dB
Blocking selectivity, 1% PER. Desired is 40 kbps 2FSK signal[3] at 3 dB above sensitivity level, frequency = 868.4 MHz	$BLOCK_{40}$	Interferer CW at Desired ± 1 MHz	—	59.7	—	dB
		Interferer CW at Desired ± 2 MHz	—	64.3	—	dB
		Interferer CW at Desired ± 5 MHz	—	74.0	—	dB
		Interferer CW at Desired ± 10 MHz	—	79.8	—	dB
		Interferer CW at Desired ± 100 MHz	—	83.8	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 1% PER. Desired is 100 kbps GFSK signal[1] at 3 dB above sensitivity level, frequency = 869.85 MHz	$BLOCK_{100}$	Interferer CW at Desired ± 1 MHz	—	48.1	—	dB
		Interferer CW at Desired ± 2 MHz	—	63.4	—	dB
		Interferer CW at Desired ± 5 MHz	—	72.6	—	dB
		Interferer CW at Desired ± 10 MHz	—	78.3	—	dB
		Interferer CW at Desired ± 100 MHz	—	80.6	—	dB
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-90.0	—	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	10	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dB
Max spurious emissions during active receive mode	$SPUR_{RX}$	30 MHz to 1 GHz	—	-81.7	-57	dBm
		1 GHz to 6 GHz	—	-68	-47	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + Δf/2), '1' = Transition from (F_center - Δf/2)
3. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2

4.6.2.2 915 MHz Band RF Receiver Characteristics

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VREGVDD = IOVDD = 3.3 V, Crystal frequency= 39.0 MHz. RF center frequency 916 MHz.

Table 4.12. 915 MHz Band RF Receiver Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF test frequency range	F_{RANGE}		902	—	928	MHz
Rx Max Strong Signal Input Level for 1% PER	RX_{SAT}	Desired is reference 100 kbps GFSK signal[1]	—	—	10.0	dBm
Sensitivity	SENS	Desired is reference 9.6 kbps 2FSK signal[2], 1% PER, frequency = 908.42 MHz, T ≤ 85 °C	—	-109.3	—	dBm
		Desired is reference 40 kbps 2FSK signal[3], 1% PER, frequency = 908.4 MHz, T ≤ 85 °C	—	-109.7	—	dBm
		Desired is reference 100 kbps GFSK signal[1], 1% PER, frequency = 916 MHz, T ≤ 85 °C	—	-108.1	—	dBm
		Desired is reference 100 kbps O-QPSK signal[4], 1% PER, frequency = 912 MHz, T ≤ 85 °C	—	-109.8	—	dBm
Image rejection, Interferer is CW at image frequency	IR	Desired is reference 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, 1% PER, frequency = 908.42 MHz	—	50.7	—	dB
		Desired is reference 40 kbps 2FSK signal[3] at 3dB above sensitivity level, 1% PER, frequency = 908.4 MHz	—	50.9	—	dB
		Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, 1% PER, frequency = 916 MHz	—	49.6	—	dB
		Desired is reference 100 kbps O-QPSK signal[4], 1% PER, frequency = 912 MHz	—	53.3	—	dB
Blocking selectivity, 1% PER. Desired is 9.6 kbps 2FSK signal[2] at 3dB above sensitivity level, frequency = 908.42 MHz	$BLOCK_{9p6}$	Interferer CW at Desired ± 1 MHz	—	58.7	—	dB
		Interferer CW at Desired ± 2 MHz	—	63.5	—	dB
		Interferer CW at Desired ± 5 MHz	—	73.0	—	dB
		Interferer CW at Desired ± 10 MHz	—	79.0	—	dB
		Interferer CW at Desired ± 100 MHz	—	82.5	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Blocking selectivity, 1% PER. Desired is 40 kbps 2FSK signal[3] at 3dB above sensitivity level, frequency = 908.4 MHz	$BLOCK_{40}$	Interferer CW at Desired ± 1 MHz	—	59.3	—	dB
		Interferer CW at Desired ± 2 MHz	—	63.7	—	dB
		Interferer CW at Desired ± 5 MHz	—	73.6	—	dB
		Interferer CW at Desired ± 10 MHz	—	79.4	—	dB
		Interferer CW at Desired ± 100 MHz	—	82.1	—	dB
Blocking selectivity, 1% PER. Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level, frequency = 916 MHz	$BLOCK_{100}$	Interferer CW at Desired ± 1 MHz	—	49.6	—	dB
		Interferer CW at Desired ± 2 MHz	—	63.1	—	dB
		Interferer CW at Desired ± 5 MHz	—	72.3	—	dB
		Interferer CW at Desired ± 10 MHz	—	78.0	—	dB
		Interferer CW at Desired ± 100 MHz	—	80.3	—	dB
Blocking selectivity, 1% PER. Desired is reference 100 kbps O-QPSK signal[4], 1% PER, frequency = 912 MHz, P_in = -89 dBm	$BLOCK_{OQPSK}$	Interferer CW at Desired ± 2 MHz	—	58.4	—	dB
		Interferer CW at Desired ± 5 MHz	—	72.2	—	dB
		Interferer CW at Desired ± 10 MHz	—	78.9	—	dB
		Interferer CW at Desired ± 100 MHz	—	84.3	—	dB
Intermod selectivity, 1% PER. CW interferers at 400 kHz and 800 kHz offsets	IM	Desired is 100 kbps GFSK signal[1] at 3dB above sensitivity level	—	43.4	—	dB
Lower limit of input power range over which RSSI resolution is maintained	$RSSI_{MIN}$		-90.0	—	—	dBm
Upper limit of input power range over which RSSI resolution is maintained	$RSSI_{MAX}$		—	—	10.0	dBm
RSSI resolution	$RSSI_{RES}$	Over $RSSI_{MIN}$ to $RSSI_{MAX}$ range	—	0.25	—	dB
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216-960 MHz	—	-81.7	-49.2	dBm
		Above 960 MHz	—	-78.7	-41.2	dBm

Note:

1. Definition of reference signal is 100 kbps 2GFSK, BT=0.6, Δf = 58 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
2. Definition of reference signal is 9.6 kbps 2FSK, Δf = 40 kHz, Manchester, '0' = Transition from (F_center + Δf/2), '1' = Transition from (F_center - Δf/2)
3. Definition of reference signal is 40 kbps 2FSK, Δf = 40 kHz, NRZ, '0' = F_center + Δf/2, '1' = F_center - Δf/2
4. Definition of reference signal is 100 kbps O-QPSK, 800 kcps chip rate, 8x spreading factor, 32 bit chip length, 4 bits per symbol

4.7 High-Frequency Crystal

Table 4.13. High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	39.0	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-3	—	3	ppm
Aging	$AGING_{HFXTAL}$		-2	—	2	ppm/5 years
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-16	—	16	ppm

4.8 GPIO Pins

Table 4.14. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.8 V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.3 V	—	2.5	—	nA
		MODEx = DISABLED, IOVDD = 3.8 V, T_A = 125 °C, all other GPIO	—	—	200	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * IOVDD	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.3 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.8 V	0.6 * IOVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.3 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.8 V	—	—	0.4 * IOVDD	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.3 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
		IOVDD = 1.8 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	13	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.3 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
		IOVDD = 1.8 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	11.9	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	33	44	55	kΩ
		RESETn pin. Pull-up to DVDD	33	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VREGVDD when DC-DC is inactive.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VREGVDD when DC-DC is inactive.

4.9 Microcontroller Peripherals

The MCU peripherals set available in FGM230S modules includes:

- 12-bit 1 Msps or 16-bit 76.9 ksps SAR Analog to Digital Converter (ADC)
- 2 × Analog Comparator (ACMP)
- 2 × 12-bit 500 ksps Digital to Analog Converter (VDAC)
- Low-Energy Sensor Interface (LESENSE)
- 34 General Purpose I/O pins with output state retention and asynchronous interrupts
- 8 Channel DMA Controller
- 12 Channel Peripheral Reflex System (PRS)
- 4 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
- 1 × 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
- 32-bit Real Time Counter
- 24-bit Low Energy Timer for waveform generation
- 2 × Watchdog Timer
- 2× Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)
- 1× Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S)
- 2 × I^2C interface with SMBus support
- Integrated Low-Energy LCD Controller supporting up to 80 segments
- Die temperature sensor

For details on their electrical performance, see the relevant portions of Section 4 in the EFR32FG23 SoC data sheet.

To learn which GPIO ports provide access to every peripheral, see 6.3 Analog Peripheral Connectivity and 6.4 Digital Peripheral Connectivity.

5. Reference Diagrams

5.1 Standalone Application

If the FGM230S SiP module is going to be used in an application without any host CPU system, e.g., in an end-device application such as a sensor, a light switch/dimmer, or a simple controller application such as a remote control, the typical connections to note are shown in the figure below.

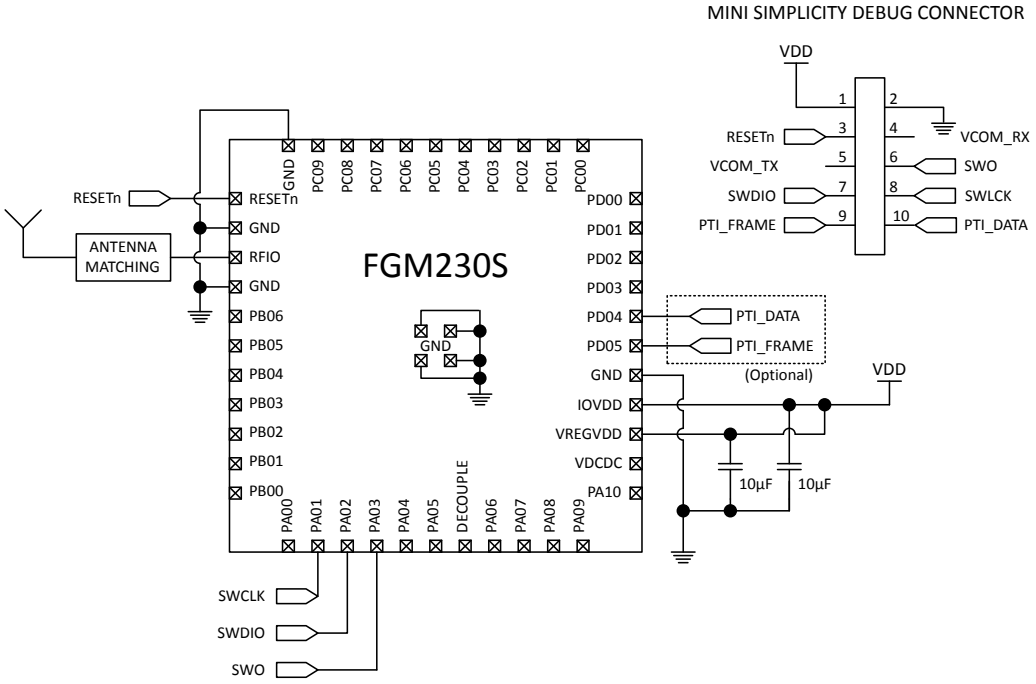


Figure 5.1. Typical Connections for a Standalone Application

Power Supplies: The two power supply pins of the SiP module: IOVDD and VREGVDD, should each be decoupled using a minimum of 10 µF. For applications with quiet GPIO activity, a single 10 µF cap can be used to decouple both IOVDD and VREGVDD. All ground connections on the SiP module should be connected to a common ground plane.

Note: The pins called “DECOUPLE” and “VDCDC” are internal test connections and they must be left “not connected”.

Flash Programming Connections: The application program of the FGM230S can be programmed in two ways:

- *Offline Programming*: Where the flash memory of the SiP modules is programmed by an external programming rig prior of product assembly.
- *Inline Programming*: Where the product is assembled and then the application program is downloaded to the flash program memory of the SiP module.

In the latter case, inline programming, the programming interface: RESETn, SWDIO, SWCLK, SWO and the supply/ground must be made available for the programming rig. This can be implemented as test-pads on the application PCB accessible for a bed-of-nails, or the programming interface can be realized in form of a Mini Simplicity header or the footprint of a Mini Simplicity header.

The Packet Trace Interface, which can be used in RF debugging to analyze received RF packets, can also be made available in the application hardware.

For additional details on programming and debugging interfaces supported by Silicon Labs products, refer to AN958: Debugging and Programming Interfaces for Custom Designs.

RF Interface: The RF interface of the FGM230S SiP module is a 50Ω matched pin, “RFIO,” which must be connected to an antenna for the RF energy to be radiated / received. The antenna can either be a PCB-trace antenna or an external antenna like a whip antenna or a piece of bent wire. If the antenna is naturally matched to 50Ω, no matching circuit is needed, but in the cases where the antenna does not have a 50Ω impedance, a matching circuit must be implemented to ensure impedance matching between the antenna and the RFIO pin of the SiP module. See Section 7. Design Guidelines for more information about where to place the SiP module on the host PCB and to learn how the antenna can be implemented.

5.2 Network Co-Processor (NCP) Application with UART Host

If the FGM230S SiP module is going to be used in an application with a Host CPU, e.g., a smart home gateway, an advanced door lock, etc., the typical connections to note are shown in the figure below.

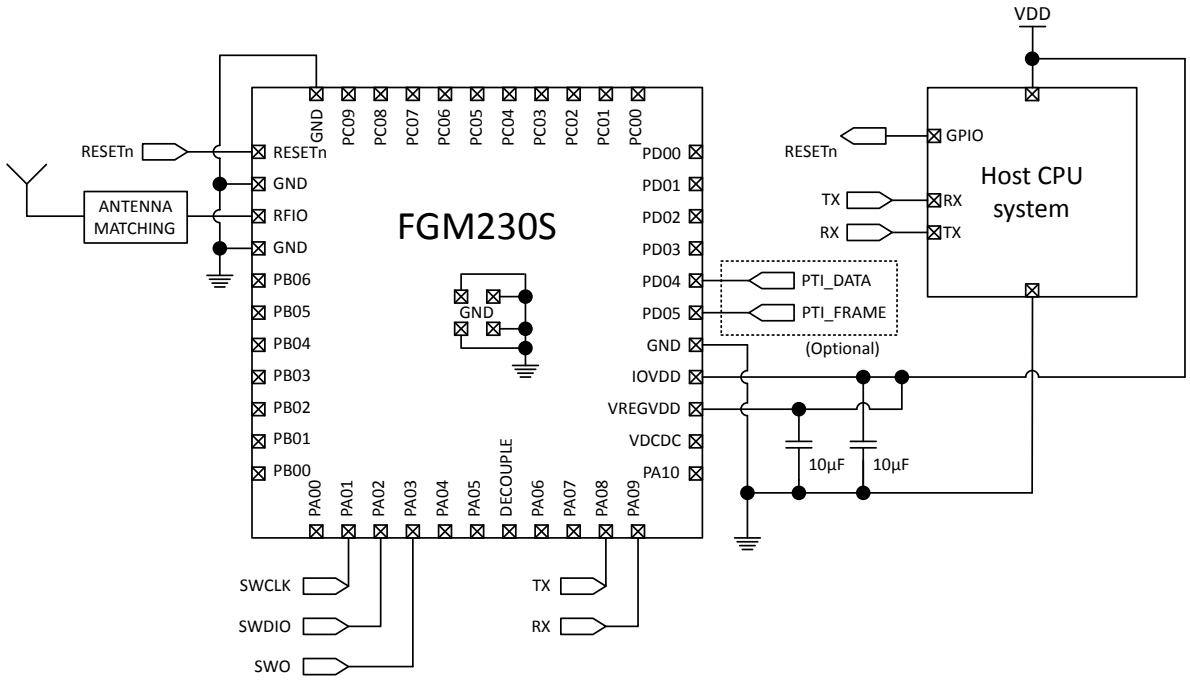


Figure 5.2. Typical FGM230S Host CPU Connections

Communication Lines: In many applications, the UART is the means of communication between the Host CPU and the FGM230S. The location of the UART pins of the FGM230S is software configurable, and if handshake signals are required, this can be enabled too, but in its most simple form, only the RX and TX pins are required for the UART communication.

Power Supplies: The two power supply pins of the SiP module: IOVDD and VREGVDD, should each be decoupled using a minimum of 10 µF, and since the Host CPU system and the FGM230S SiP module share supply lines, care must be taken to avoid supply noise being coupled from the Host CPU system to the FGM230S. It is therefore important that the Host CPU system has adequate supply noise suppression. All ground connections on the SiP module should be connected to a common ground plane shared with the Host CPU.

Note: The pins called “DECOUPLE” and “VDCDC” are internal test connections, and they must be left “not connected”.

Flash Programming Connections: The application program of the FGM230S can be programmed in three ways:

- *Offline Programming*: Where the flash memory of the SiP modules is programmed by an external programming rig prior of product assembly.
- *Inline Programming*: Where the product is assembled and then the application program is downloaded to the flash program memory of the SiP module. For inline programming, the programming interface: RESETn, SWDIO, SWCLK, SWO, and the supply/ground must be made available for the programming rig by some means, e.g., test-pads on the PCB.
- *Host CPU Programming*: Where GPIO’s of the Host CPU are connected to the programming interface of the FGM230S module. This enables in-field upgrade possibilities, where the Host CPU can re-program the flash program memory of the FGM230S.

In the latter case, Host CPU programming, the programming interface: RESETn, SWDIO, SWCLK, and SWO must be connected to GPIOs of the Host CPU.

RF Interface: The RF interface of the FGM230S SiP module is a 50Ω matched pin, “RFIO,” which must be connected to an antenna for the RF energy to be radiated / received. The antenna can either be a PCB-trace antenna or an external antenna like a whip antenna or a piece of bent wire. If the antenna is naturally matched to 50Ω, no matching circuit is needed, but in the cases where the antenna does not have a 50Ω impedance, a matching circuit must be implemented in order to ensure impedance matching between the antenna and the RFIO pin of the SiP module. See Section 7. Design Guidelines for more information about where to place the SiP module on the host PCB and to learn how the antenna can be implemented.

6. Pin Definitions

6.1 Module Pinout

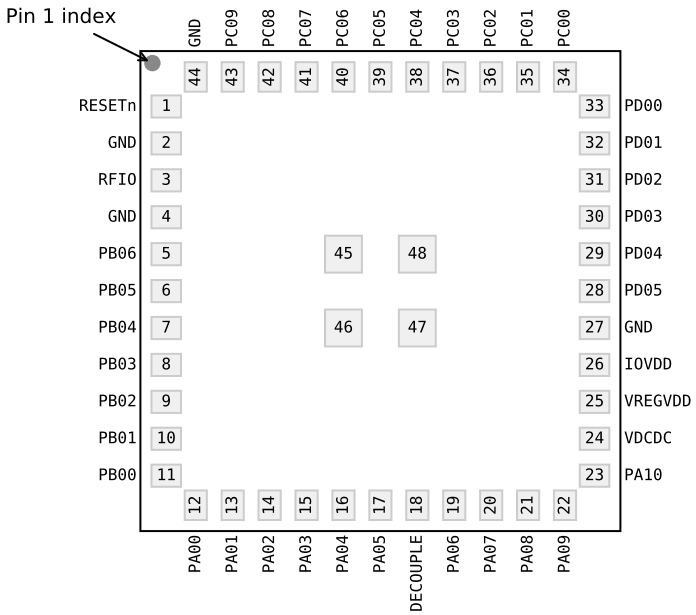


Figure 6.1. FGM230S Module Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.2 Alternate Pin Functions, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity.

Note that GPIO and Peripheral capabilities may differ by part number or be limited by the API or software stack.

Table 6.1. FGM230S SiP Module Pin Definitions

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
RESETn	1	Reset Pin. The RESETn pin is internally pulled up to the DVDD supply on the SoC.	GND	2	Ground
RFIO	3	RF input/output	GND	4	Ground
PB06	5	GPIO	PB05	6	GPIO
PB04	7	GPIO	PB03	8	GPIO
PB02	9	GPIO	PB01	10	GPIO
PB00	11	GPIO	PA00	12	GPIO
PA01	13	GPIO	PA02	14	GPIO
PA03	15	GPIO	PA04	16	GPIO
PA05	17	GPIO	DECOUPLE	18	Do Not Connect

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA06	19	GPIO	PA07	20	GPIO
PA08	21	GPIO	PA09	22	GPIO
PA10	23	GPIO	VDCDC	24	Do Not Connect
VREGVDD	25	Module input power supply.	IOVDD	26	Module I/O pin supply. This pin is internally connected to the SoC IOVDD and AVDD supply lines.
GND	27	Ground	PD05	28	GPIO
PD04	29	GPIO	PD03	30	GPIO
PD02	31	GPIO	PD01	32	GPIO
PD00	33	GPIO	PC00	34	GPIO
PC01	35	GPIO	PC02	36	GPIO
PC03	37	GPIO	PC04	38	GPIO
PC05	39	GPIO	PC06	40	GPIO
PC07	41	GPIO	PC08	42	GPIO
PC09	43	GPIO	GND	44	Ground
GND	45	Ground	GND	46	Ground
GND	47	Ground	GND	48	Ground

6.2 Alternate Pin Functions

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc. The following table shows which module pins have alternate capabilities and the functions they support.

Table 6.2. GPIO Alternate Function Table

GPIO	Alternate Functions			
PB03	GPIO.EM4WU4		LCD.SEG17	
PB02			LCD.SEG16	
PB01	GPIO.EM4WU3	VDAC0.CH1_MAIN_OUT	LCD.SEG15	
PB00		VDAC0.CH0_MAIN_OUT	LCD.SEG14	
PA00		IADC0.VREFP	LCD.SEG8	
PA01	GPIO.SWCLK		LCD.SEG9	
PA02	GPIO.SWDIO			
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0	LESENSE.LESENSE_EN_0		
PA04	GPIO.TDI GPIO.TRACECLK	LESENSE.LESENSE_EN_1	LCD.SEG10	
PA05	GPIO.TRACEDATA1 GPIO.EM4WU0	LESENSE.LESENSE_EN_2	LCD.SEG11	
PA06	GPIO.TRACEDATA2		LCD.LCD_CP	
PA07	GPIO.TRACEDATA3		LCD.SEG12	
PA08			LCD.SEG13	
PD05	GPIO.EM4WU10		LCD.COM3	
PD04			LCD.COM2	
PD03			LCD.COM1	
PD02	GPIO.EM4WU9		LCD.COM0	
PD01		LFXO.LFXTAL_I LFXO.LF_EXTCLK		
PD00		LFXO.LFXTAL_O		
PC00	GPIO.EM4WU6		LCD.SEG0	
PC01			LCD.SEG1	
PC02			LCD.SEG2	
PC03			LCD.SEG3	
PC04			LCD.SEG4	
PC05	GPIO.EM4WU7		LCD.SEG5	
PC06			LCD.SEG6	
PC07	GPIO.EM4WU8		LCD.SEG7	

GPIO	Alternate Functions			
PC08			LCD.SEG18	
PC09	GPIO.THMSW_EN		LCD.SEG19	

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIOs. The table below indicates which peripherals are available on each GPIO port. When a differential connection is used, Positive inputs are restricted to the EVEN pins and Negative inputs are restricted to the ODD pins. When a single ended connection is used, positive input is avaliable on all pins. See the device Reference Manual for more details on the ABUS and analog peripherals.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	CH0_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
EUSART2.CS			Available	Available
EUSART2.CTS			Available	Available
EUSART2.RTS			Available	Available
EUSART2.RX			Available	Available
EUSART2.SCLK			Available	Available
EUSART2.TX			Available	Available
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
I2C1.SDA			Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4	Available	Available	Available	Available
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LESENSE.CH0OUT	Available	Available		
LESENSE.CH10OUT	Available	Available		
LESENSE.CH11OUT	Available	Available		
LESENSE.CH12OUT	Available	Available		
LESENSE.CH13OUT	Available	Available		
LESENSE.CH14OUT	Available	Available		
LESENSE.CH15OUT	Available	Available		
LESENSE.CH1OUT	Available	Available		
LESENSE.CH2OUT	Available	Available		
LESENSE.CH3OUT	Available	Available		
LESENSE.CH4OUT	Available	Available		
LESENSE.CH5OUT	Available	Available		
LESENSE.CH6OUT	Available	Available		
LESENSE.CH7OUT	Available	Available		
LESENSE.CH8OUT	Available	Available		
LESENSE.CH9OUT	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available

7. Design Guidelines

7.1 Layout and Placement

For in-depth information about antenna design and antenna structures, see the below application notes available from http://www.silabs.com:

- AN853: Single-Ended Antenna Matrix Design Guide
- AN768: Antenna Selection Guide for the 868MHz EZRadio and EZRadioPRO Designs
- AN847: 915MHz Single-Ended Antenna Matrix Selection Guide

For general layout consideration and recommendations, see this application note available from http://www.silabs.com:

- AN928.2: EFR32 Series 2 Layout Design Guide

For optimal performance of the FGM230S SiP module, use the following guidelines:

- Place the FGM230S on the host PCB where the antenna of the FGM230S system will have its best possible performance:
  - For an external antenna type, see Figure 7.1 FGM230S Implementation with External Antenna on page 37, the location of the FGM230S and its antenna is fairly flexible, but as described in AN853, the performance of the antenna will depend on the ground plane of the entire application PCB.
  - For a PCB trace antenna type, see Figure 7.2 FGM230S Implementation with PCB Trace Antenna on page 37, the location of the FGM230S and its antenna must be at a edge of the host PCB, with no copper or signal routing underneath the antenna structure and sufficient copper clearance around the antenna structure to ensure a good antenna performance. See AN853, AN768, and AN847 for detailed implementation guidelines and a description of various PCB trace antenna structures.
- Place the FGM230S and all RF traces above a solid ground plane with good via connectivity to a top layer ground plane.
- Locate the FGM230S and the antenna / antenna structure as far away from any electrical noise sources on the host PCB as possible, such as:
  - High-speed memory busses of a host CPU system.
  - High-power switching noise sources like switch mode power supplies, triac circuits, electric motor control circuits etc.
  - Other radio systems.
  - Fast switching circuits.
  - If the antenna is external, avoid placing the antenna above the FGM230S since the SiP module contains both fast switching signals (the crystal oscillator) and high-power switch noise sources (the DCDC circuit).
- As a general rule: Use a 50 Ω transmissions line to route the RF signal, especially if the RF trace is longer than λ/16 of the fundamental frequency, which for 868 MHz is 21.6mm and for 915 MHz is 20.6 mm. The impedance of the RF trace depends on the stack-up of the host PCB, see Figure 7.3 RF Trace Design Example on page 38.
- A U.FL connector or a SMA connector can be used to connect to an external antenna. The use of a U.FL or a SMA connector is also recommended for conductive tests. If there is not room enough for a connector foot-print in the application, ensure that there is as a minimum room enough to attached an RF pig-tail to the application in order to enable conducted measurements on the product.
- Connect all ground pads directly to a solid ground plane.
- Do not place plastic or any other dielectric material in contact with the antenna.
- Do not locate the antenna inside an enclosure made of an electrically conductive material.

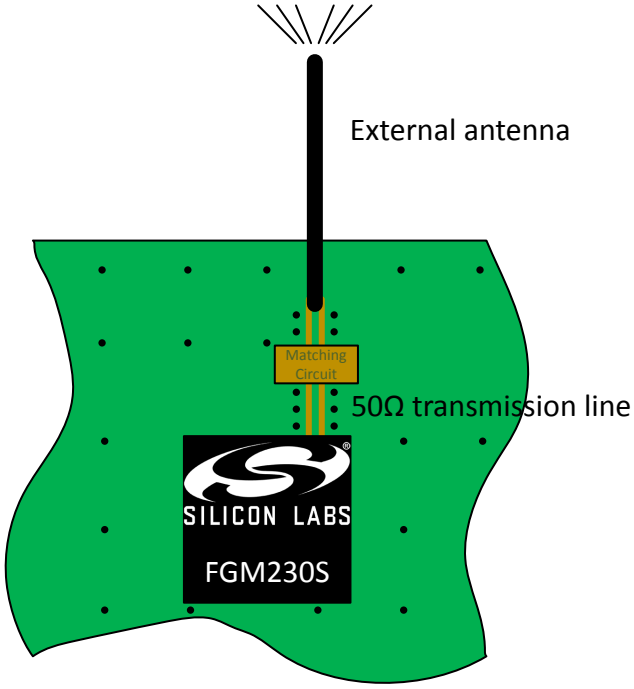


Figure 7.1. FGM230S Implementation with External Antenna

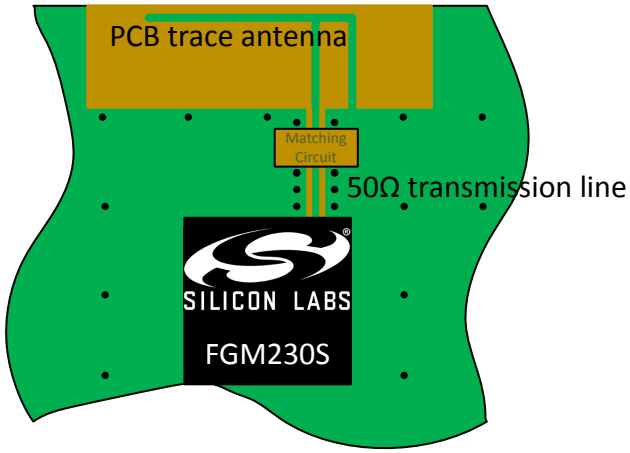
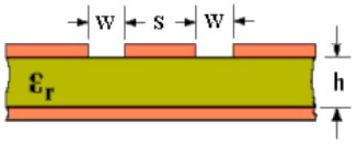


Figure 7.2. FGM230S Implementation with PCB Trace Antenna

Independently of the type of antenna selected, the efficiency of the antenna and the radiation pattern of the antenna depend on the surrounding ground plane. The clearance distances from an antenna structure to the ground-plane and the size of the ground plane is significant and must always be evaluated when the type of antenna to use is to be selected. See AN853: Single-Ended Antenna Matrix Design Guide for detailed information.

The impedance of the RF trace, which is the impedance of a coplanar trace above a ground plane, can be calculated using freely available web calculators:



INPUT DATA

Relative Dielectric Constant (ε_r):	4.6	
Track Width (S):	1.8	mm
Gap Width (W):	0.5	mm
Dielectric Thickness (h):	1.5	mm

RESULTS

Effective Dielectric Constant (ε_{eff}):	3.016	
Characteristic Impedance (Zo):	51.72	Ohms

Figure 7.3. RF Trace Design Example

The impedance of a PCB trace depends on the following:

- The dielectric constant of the PCB material
- The width of the RF trace
- The distance from the RF trace to the top-level ground plane
- The thickness of the PCB core material.

7.2 Proximity to Other Materials

Because this will degrade the performance of the antenna, ideally, an antenna should not be:

- Surrounded by any dielectric or conductive material
- Located in close proximity to dielectric or conductive material

However, for most products with antennas, the antenna will be located inside an enclosure, so the following precautions must be taken:

- Avoid placing plastic or any other dielectric material closer than 5 mm to the antenna. If the dielectric material is too close to the antenna, a retune of the antenna may be required.
- Avoid placing metallic objects in close proximity to the antenna because it will prevent the antenna from radiating freely:
  - The minimum recommended distance for large metallic and/or conductive objects is 50 mm in any direction from the antenna, except in the directions of the application PCB ground planes. If a large metallic object gets close to the antenna, losses of 1-3 dB may be expected, with an increase in loss for closer distances.
  - Metallic objects with a maximum dimension < 10 mm, such as cabinet screws etc., should be located > 10 mm from the antenna in any direction, except in the directions of the applications PCB ground plane

Because of the sensitivity of the antenna to its surroundings, it is advised that one always test the product as an assembled unit. If detuning of the antenna due to enclosure-effects are observed, a retune of the antenna is advised. It is also possible to simulate the entire system in an electro-magnetic field simulator, if such software is available, in order to find the best possible shape or location of the antenna.

7.3 Reset

The FGM230S SiP module can be reset by:

- Pulling the RESETn pin low
- The internal watchdog timer
- A software command

The reset state does not provide any power saving advantages. Therefore, it is not recommended that the device is kept in its reset state to save power.

7.4 Debug

For detailed information about debugging, see AN958: Debugging and Programming Interfaces for Custom Designs.

The FGM230S supports hardware debugging via either a 4-pin JTAG or a 2-pin serial-wire debug (SWD) interface. Expose the debug pins in the application for both programming purposes and debug purposes.

The table below lists the required pins for the JTAG and SWD debug interfacing.

If the JTAG interface is enabled, the module must be power cycled to return to the SWD configuration.

Table 7.1. Debug Pins

Pin Name	Pin Number	JTAG signal	SWD Signal	Comments
PA04	16	TDI	N/A	Pin disabled after reset. Once enabled, pull-up
PA03	15	TDO	N/A	Disabled after reset
PA02	14	TMS	SWDIO	Enabled after reset and has built-in pull-up
PA01	13	TCK	SWCLK	Enabled after reset and has built-in pull-up

7.5 Packet Trace Interface (PTI)

The FGM230S integrates a true PHY-level packet trace interface, which can be used with a network analyzer application to capture and analyze received RF packets non-intrusively and without burdening the embedded processor of the FGM230S SiP module. The PTI generates two output signals: PTI_DATA and PTI_FRAME, and the signals can be accessed through any GPIO on the ports C and D (search for FRC.DOUT and FRC.DFRAME peripheral resources in Table 6.4 DBUS Routing Table on page 32).

8. Package Specifications

8.1 Package Outline

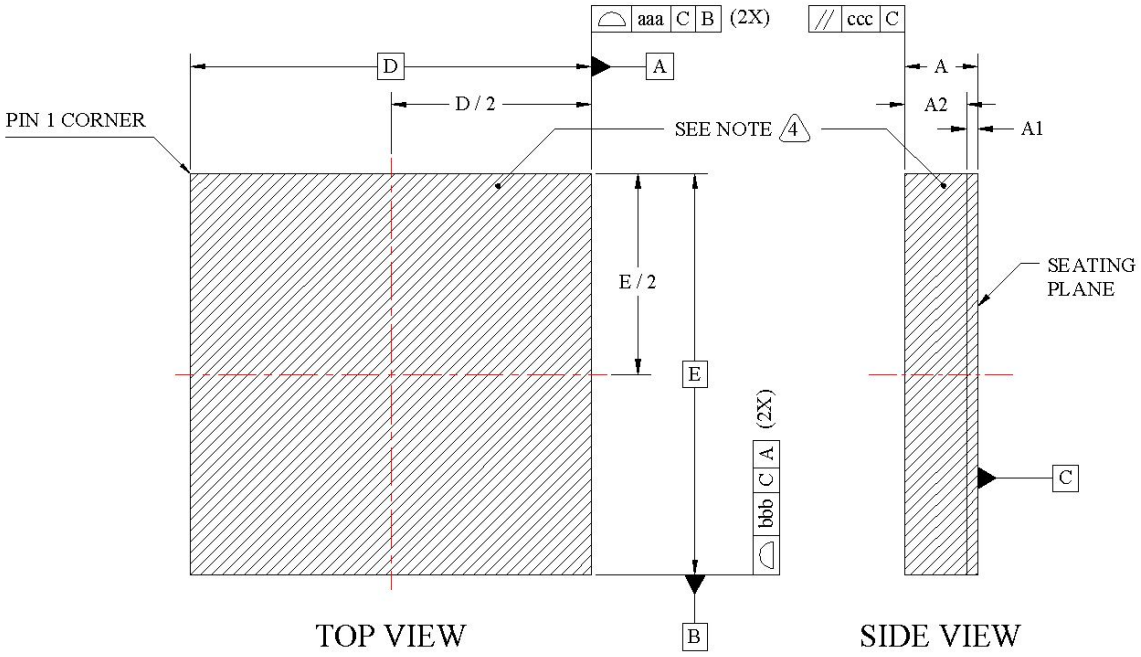


Figure 8.1. Top and Side Views

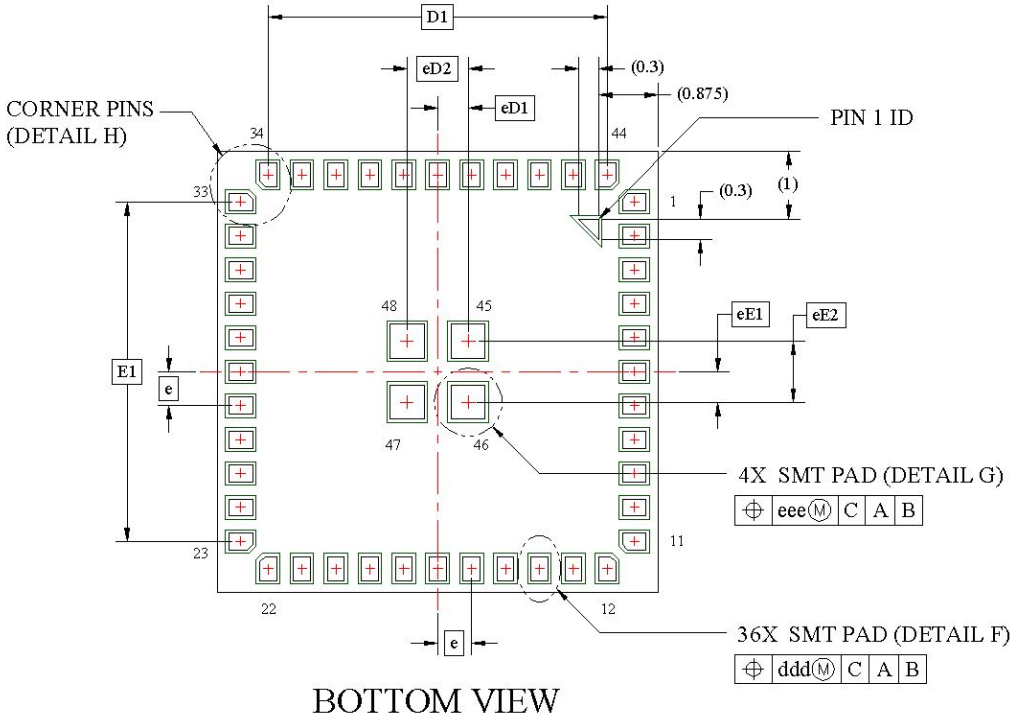


Figure 8.2. Bottom View

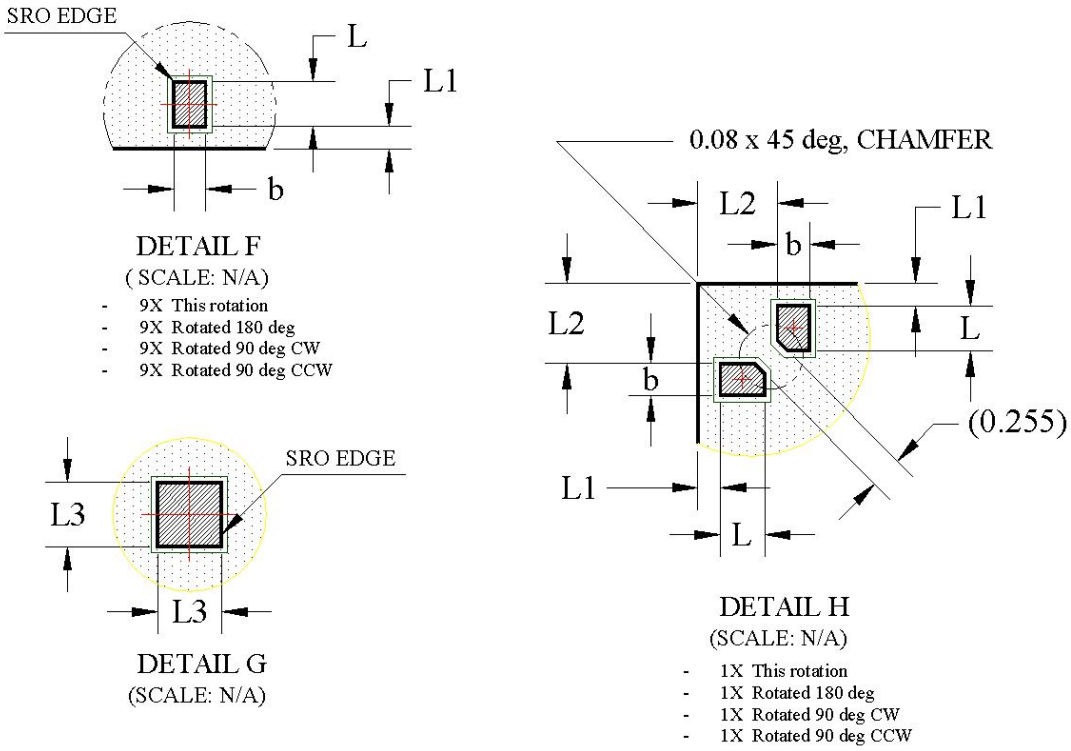


Figure 8.3. Package Edge Detail

Dimension	MIN	NOM	MAX
A	1.080	1.180	1.280
A1	0.140	0.180	0.220
A2	0.950	1.000	1.050
b	0.200	0.250	0.300
D		6.500 BSC	
D1		5.000 BSC	
e		0.500 BSC	
E		6.500 BSC	
E1		5.000 BSC	
L	0.300	0.350	0.400
L1	0.125	0.175	0.225
L2	0.575	0.625	0.675
L3	0.450	0.500	0.550
eD1		0.450 BSC	
eD2		0.900 BSC	
eE1		0.450 BSC	
eE2		0.900 BSC	
aaa		0.100	
bbb		0.100	
ccc		0.100	

Dimension	MIN	NOM	MAX
ddd		0.100	
eee		0.100	

Note:

1. The dimensions in parenthesis are reference.
2. All dimensions in millimeters (mms).
3. Unless otherwise specified tolerances are:
   a. Decimal:
      - X.X = ±0.1
      - X.XX =±0.05
      - X.XXX=±0.003
   b. Angular:
      - ±0.1 (In Deg)
4. Hatching lines means package shielding area.

8.2 PCB Land Pattern

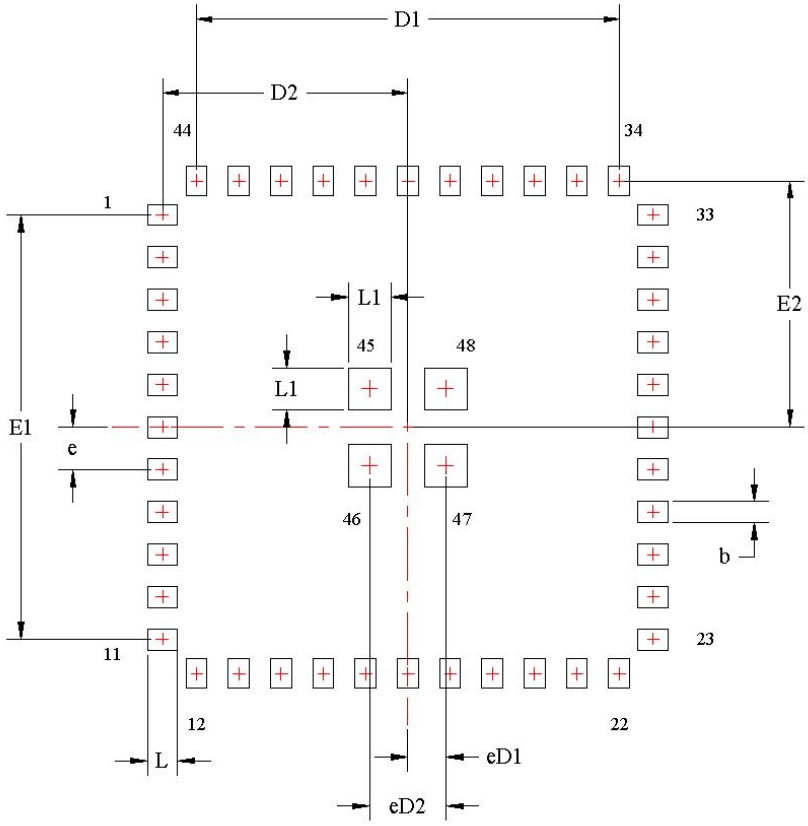


Figure 8.4. Recommended Land Pattern

Dimension	NOM
D1	5.00
D2	2.90
E1	5.00
E2	2.90
eD1	0.45
eD2	0.90
b	0.25
e	0.50
L	0.35
L1	0.50

Dimension	NOM

Note: *

General

1. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.

Stencil

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.100 mm (4 mils).
3. The stencil aperture to land pad size recommendation is 80% paste coverage.

*Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling

8.3 Package Marking

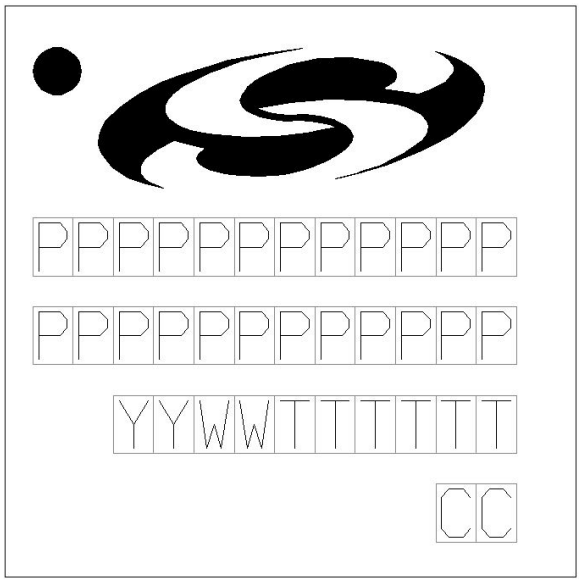


Figure 8.5. FGM230S Top Marking

Mark Description

The package marking consists of:

- PPPPPPPPPPPP - Part number designation
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – A trace or manufacturing code. The first letter is the device revision
- CC - Country of origin

9. Soldering Recommendations

The FGM230S is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven, and particular type of solder paste used.

- See technical documentation of your particular solder paste for profile configurations.
- Avoid using more than two reflow cycles.
- A no-clean, type-3 solder paste is recommended.
- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- Recommended stencil thickness is 0.100 mm (4 mils).
- General SMT application notes are provided in the AN1223: LGA Manufacturing Guidance document.
- See the JEDEC/IPC J-STD-020, IPC-SM-782 and IPC 7351 guidelines for further recommendations.
- The above notes are recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.

10. Tape and Reel

FGM230S modules are delivered to the customer in Tray (260 pcs) or Tape and Reel (2500 pcs) packing with the dimensions below. All dimensions are given in mm unless otherwise indicated.

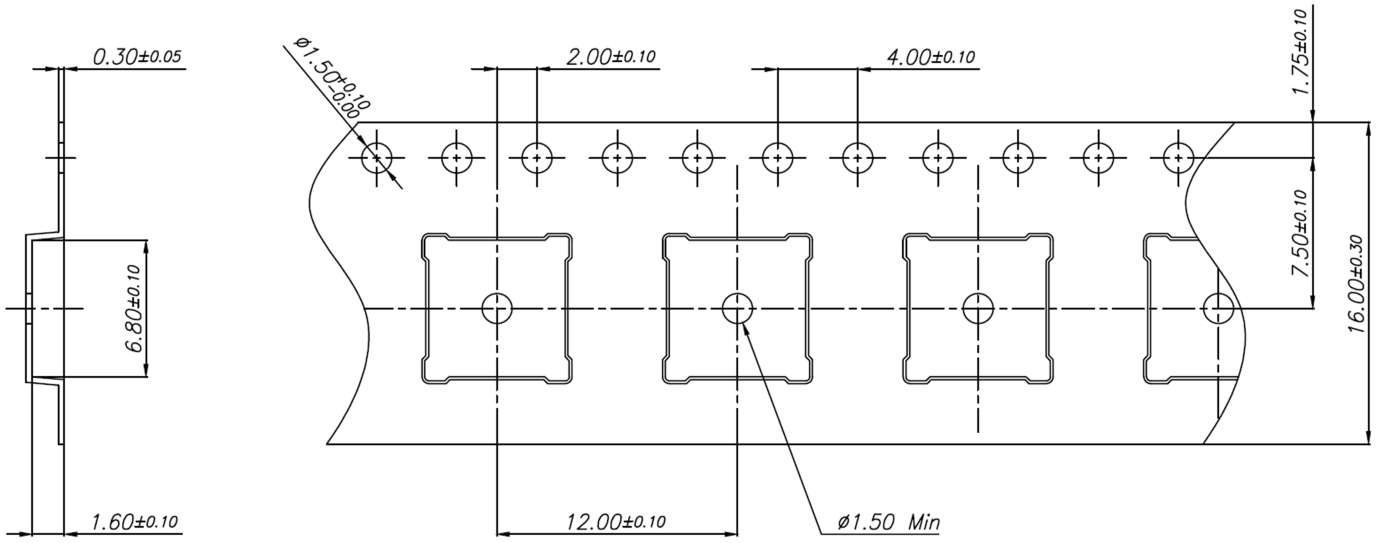


Figure 10.1. Carrier Tape Dimensions

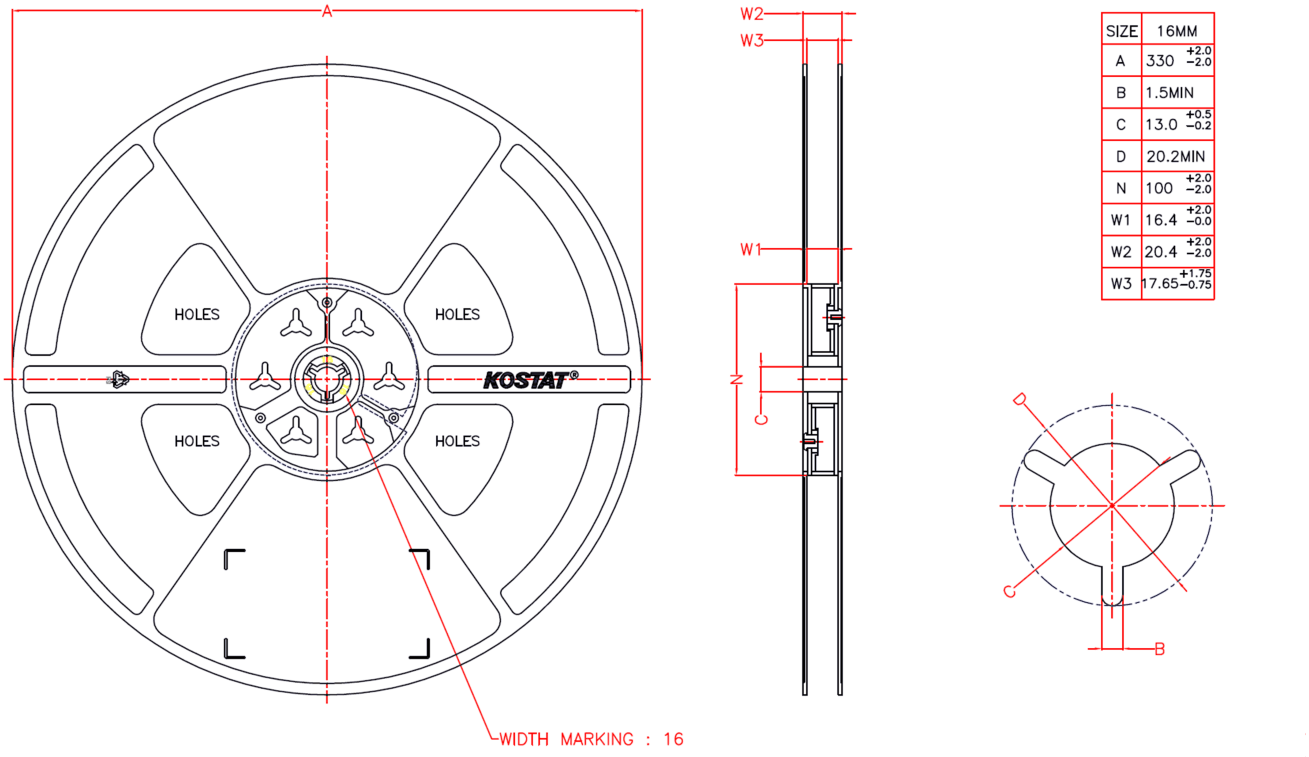


Figure 10.2. Reel Dimensions

11. Certifications

FGM230S is an uncertified module.
The transceiver characteristics, provided in Section 4.5 Current Consumption are corresponding those of ZGM230S, but when using proprietory technology, the user should conduct own tests to demonstrate the compliance to the standards, rules and directives that are applicable for regulatory radio approvals in each region.

12. Revision History

Revision 1.2

November, 2024

- Updated 2. Ordering Information to note that the FGM230-RB4328B (Vault-Mid) board is NRND.

Revision 1.1

April, 2023

- Clarified that Secure Debug is supported for both Secure Vault Mid and High in 3.5.4 Secure Debug with Lock/Unlock section.
- 4.3 General Operating Conditions table changes:
  - Added HCLK and SYSCLK frequency specification for "VSCALE1, WS1" test condition.
  - Corrected HCLK and SYSCLK frequency MAX value for "VSCALE1, WS0" test condition.
- 4.4 Thermal Characteristics table format updated.
- 4.6.2.1 868 MHz Band RF Receiver Characteristics table changes:
  - Updated test condition for $SPUR_{RX}$ from "1 GHz to 12 GHz" to "1 GHz to 6 GHz".

Revision 1.0

November, 2022

Initial release.

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