I²C PROGRAMMABLE, ANY-FREQUENCY 1–200 MHZ, QUAD FREQUENCY 8-OUTPUT CLOCK GENERATOR

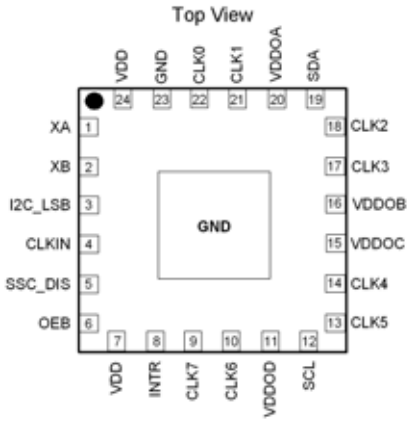
Features

- Generates any frequency from 1 to 200 MHz on each of the 4 output banks
- Eight CMOS clock outputs
- Programmable frequency configuration
- 0 ppm frequency synthesis error for any combination of frequencies
- 19 to 30 MHz xtal or 5–200 MHz input clk
- Easy to use programming software
- Configurable “triple A” spread spectrum: *any* clock, *any* frequency, and with *any* spread amount
- Programmable output phase adjustment with <20 ps error
- Interrupt pin indicates LOS or LOL
- OEB pin disables all outputs or per bank $\overline{OEB}$ control via I²C
- Low jitter: 1.5 ps rms phase jitter
- Excellent PSRR performance eliminates need for external power supply filtering
- Low power: 45 mA (core)
- Core VDD: 1.8, 2.5, or 3.3 V
- Separate VDDO for each bank of outputs: 1.8, 2.5, or 3.3 V
- Small size: 4x4 mm 24-QFN
- Pb-free, RoHS-6 compliant
- Industrial temperature range: –40 to +85 °C

Ordering Information:

See page 25.

Pin Assignments



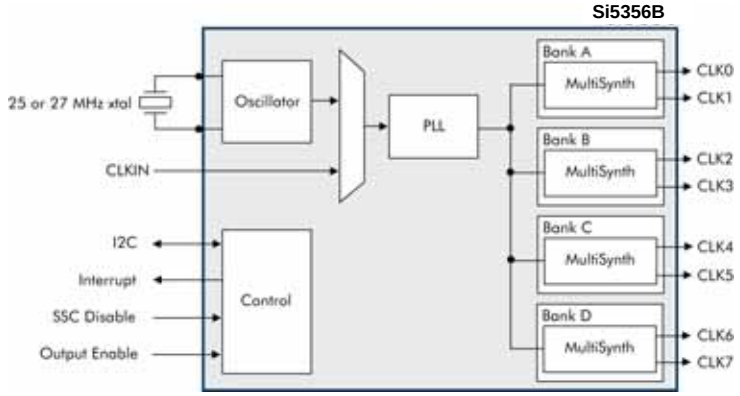
Applications

- Printers
- Audio/video
- Networking
- Communications
- Storage
- Switches/routers
- Computing
- Servers
- OC-3/OC-12 line cards

Description

The Si5356B is a highly flexible, I²C programmable clock generator capable of synthesizing four completely non-integer related frequencies up to 200 MHz. The device has four banks of outputs with each bank supporting two CMOS outputs at the same frequency. Using Silicon Laboratories' patented MultiSynth fractional divider technology, all outputs have 0 ppm frequency synthesis error regardless of configuration, enabling the replacement of multiple clock ICs and crystal oscillators with a single device. Each output bank is independently configurable to support 1.8, 2.5, or 3.3 V. The device is programmable via an I²C/SMBus-compatible serial interface and supports operation from a 1.8, 2.5, or 3.3 V core supply.

Functional Block Diagram



***Refer to Ordering Guide for custom part numbers.**

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Section **Page**

1. Electrical Specifications

Table 1. Recommended Operating Conditions

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	T_A		–40	—	85	°C
Core Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	
			1.71	1.8	1.98	
Output Buffer Supply Voltage	V_{DDO}		1.71	—	3.63	V

Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

Table 2. DC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Current Consumption	I_{DD}	100 MHz on all outputs, 25 MHz refclk	—	45	60	mA
Output Buffer Supply Current	I_{DDOX}	CMOS, 50 MHz 15 pF load[1]	—	6	9	mA
		CMOS, 200 MHz[1,2], 3.3 V	—	13	18	mA
		CMOS, 200 MHz[1,2], 2.5 V	—	10	14	mA
		CMOS, 200 MHz[1,2], 1.8 V	—	7	10	
High Level Input Voltage	V_{IH}	CLKIN, I2C_LSB	0.8 x V_{DD}	—	3.63	V
		SSC_DIS, $\overline{OEB}$	0.85	—	1.2	V
Low Level Input Voltage	V_{IL}	CLKIN, I2C_LSB	–0.2	—	0.2 x V_{DD}	V
		SSC_DIS, $\overline{OEB}$	—	—	0.3	V
Clock Output High Level Output Voltage	V_{OH}	Pins: CLK0-7 I_{OH} = –4 mA	V_{DDO} – 0.3	—	—	V
Clock Output Low Level Output Voltage	V_{OL}	Pins: CLK0-7 I_{OH} = +4 mA	—	—	0.3	V
INTR Low Level Output Voltage	V_{OLINTR}	Pin: LOS I_{OH} = +3 mA	0	—	0.4	V
SSC_DIS, $\overline{OEB}$ Input Resistance	R_{IN}		—	20	—	kΩ

Notes:
1. Single CMOS driver active.
2. Measured into a 5”, 50 Ω trace with a 2 pF load.

Table 3. AC Characteristics

(V_{DD} = 1.8 V –5% to +10%, 2.5 or 3.3 V ±10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Clock						
Clock Input Frequency	F_{IN}		5	—	200	MHz
Clock Input Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}	—	—	2.3	ns
Clock Input Duty Cycle	DC	< 2 ns tr/tf	40	—	60	%
Clock Input Capacitance	C_{IN}		—	2	—	pF
Output Clocks						
Clock Output Frequency	F_O		1	—	200	MHz
Clock Output Frequency Synthesis Resolution	F_{RES}	See "3.3. Input and Output Frequency Configuration" on page 11	—	—	1	ppb
Output Load Capacitance	C_L		—	—	15	pF
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 15 pF	—	—	2.0	ns
Clock Output Rise/Fall Time	T_R/T_F	20 to 80% V_{DD}, C_L = 2 pF	—	0.45	0.85	ns
Clock Output Duty Cycle	DC	Measured at $V_{DD}/2$	45	50	55	%
Powerup Time	T_{PU}	POR to output clock valid	—	—	2	ms
Output Enable Time	T_{OE}		—	—	10	µs
Output-Output Skew	T_{SKEW}	Outputs at same frequency, f_{OUT} > 5 MHz	–150	—	+150	ps
Period Jitter	J_{PPKPK}	10000 cycles	—	50	75	ps pk-pk
Cycle-Cycle Jitter[1]	J_{CCPK}	10000 cycles	—	40	70	ps pk
Phase Jitter	J_{PH}	MultiSynth in integer mode, 5 kHz to 1 MHz	—	1.5[2]	—	ps rms
PLL Loop Bandwidth	F_{BW}		—	1.6	—	MHz
Interrupt Status Timing						
CLKIN Loss of Signal Assert Time	t_{LOS}		—	2.6	5	µs
CLKIN Loss of Signal Deassert Time	t_{LOS_b}		0.01	0.2	1	µs

Notes:
1. Measured in accordance to JEDEC standard 65.
2. Phase Jitter only guaranteed for Multisynth0.

Table 4. Crystal Specifications for 19 to 26 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	19	25	26	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	100	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 5. Crystal Specifications for 26 to 30 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	f_{XTAL}	26	27	30	MHz
Load Capacitance (on-chip differential)	c_L (supported)*	11	12	13	pF
	c_L (recommended)	17	18	19	pF
Crystal Output Capacitance	c_O	—	—	5	pF
Equivalent Series Resistance	r_{ESR}	—	—	75	Ω
Crystal Max Drive Level	d_L	100	—	—	µW

***Note:** See "AN360: Crystal Selection Guide for Si533x and Si5355/56 Devices" for how to adjust the registers to accommodate a 12 pF crystal C_L.

Table 6. I^2C Specifications (SCL,SDA)[1]

Parameter	Symbol	Test Condition	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
LOW Level Input Voltage	V_{ILI2C}		–0.5	0.3 x V_{DDI2C}	–0.5	0.3 x V_{DDI2C}[2]	V
HIGH Level Input Voltage	V_{IHI2C}		0.7 x V_{DDI2C}	3.63	0.7 x V_{DDI2C}[2]	3.63	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		N/A	N/A	0.1	—	V
LOW Level Output Voltage (open drain or open collector) at 3 mA Sink Current	V_{OLI2C}[2]	V_{DDI2C}[2] = 2.5/3.3 V	0	0.4	0	0.4	V
		V_{DDI2C}[2] = 1.8 V	N/A	N/A	0	0.2 x V_{DDI2C}	V
Input Current	I_{II2C}		–10	10	–10	10	µA
Capacitance for each I/O Pin	C_{II2C}	V_{IN} = –0.1 to V_{DDI2C}	—	4	—	4	pF
I^2C Bus Timeout		Timeout Enabled	25	35	25	35	ms
Data rate			100		400		kbps

Notes:

1. Refer to NXP's UM10204 I^2C-bus specification and user manual, Revision 03, for further details: www.nxp.com/acrobat_download/usermanuals/UM10204_3.pdf.
2. Only I^2C pullup voltages (VDDI2C) of 1.71 to 3.63 V are supported. Must write register 27[7] = 1 if the I^2C bus voltage is less than 2.5 V to maintain compatibility with the I^2C bus standard.

Table 7. Thermal Characteristics

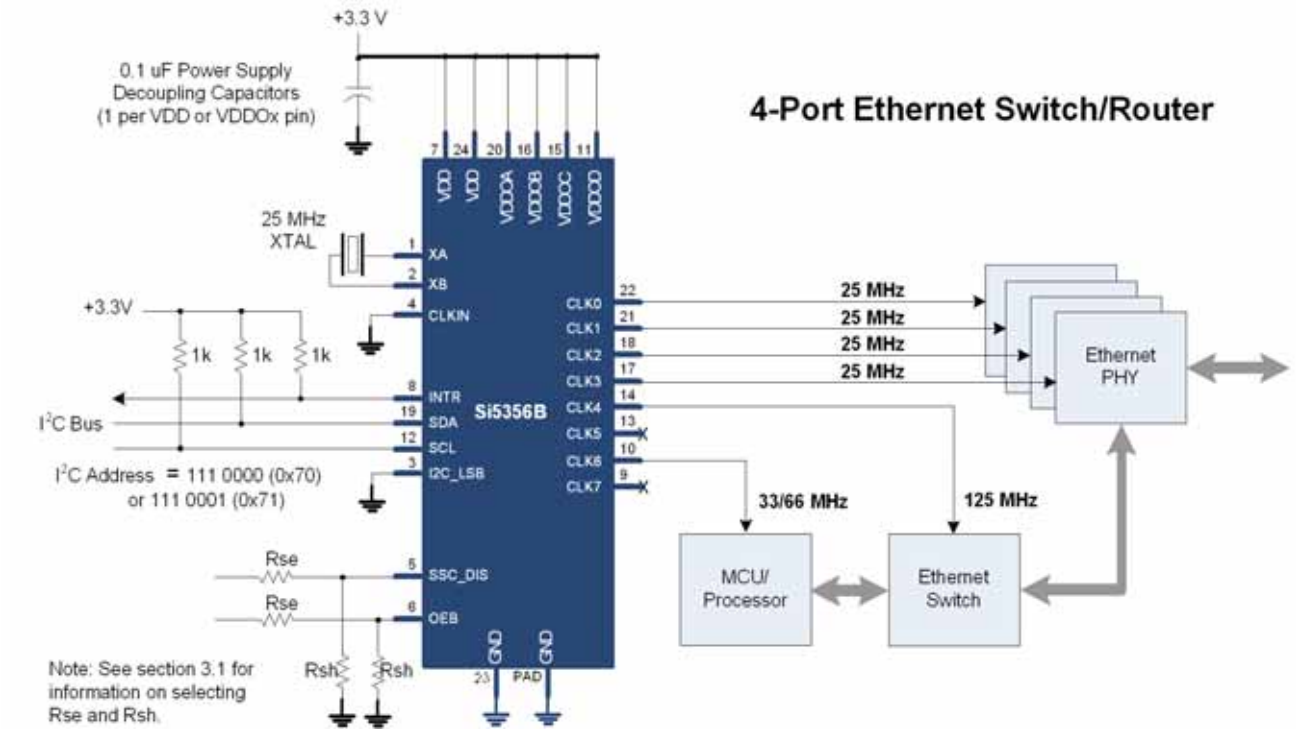
Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	37	°C/W
Thermal Resistance Junction to Case	θ_{JC}	Still Air	25	°C/W

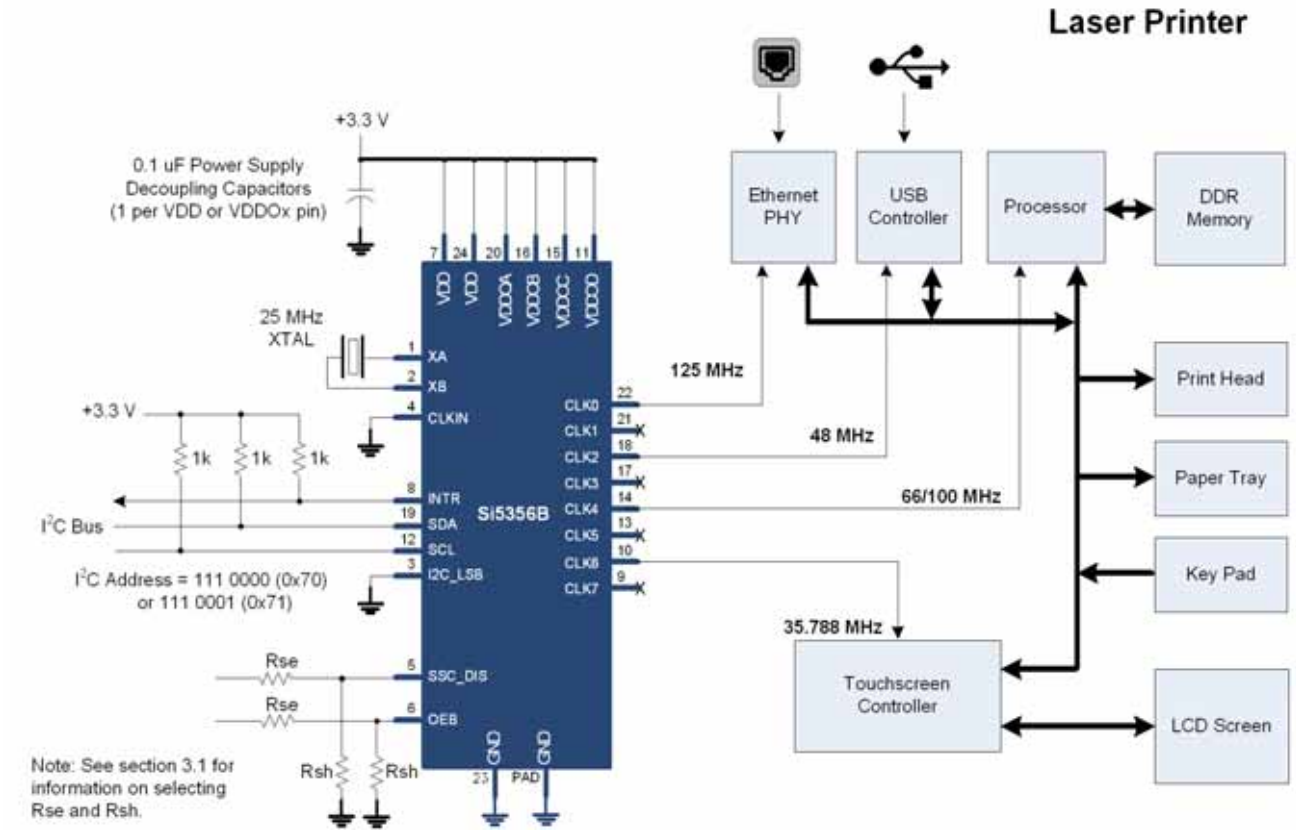
Table 8. Absolute Maximum Ratings[1,2,3,4]

Parameter	Symbol	Rating	Unit
Supply Voltage Range	V_{DD}	–0.5 to +3.8	V
Input Voltage Range (all pins except pins 1,2,5,6)	V_I	–0.5 to 3.8	V
Input Voltage Range (pins 1,2,5,6)	V_{I2}	–0.5 to 1.3	V
Output Voltage Range	V_O	–0.5 to V_{DD} + 0.3	V
Junction Temperature	T_J	–55 to +150	°C
ESD Tolerance	HBM	2.5	kV
	CDM	550	V
	MM	175	V
Latch-up Tolerance	LU	JESD78 Compliant	
Soldering Temperature (Pb-free profile)[4]	T_{PEAK}	260	°C
Soldering Temperature Time at T_{PEAK} (Pb-free profile)[4]	T_P	20–40	sec

Notes:
1. Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. 24-QFN package is RoHS compliant.
3. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.
4. The device is compliant with JEDEC J-STD-020.

2. Typical Application Circuits





3. Functional Description

3.1. Input Configuration

The Si5356B input can be driven from either an external crystal or a reference clock. If the crystal input option is used, the Si5356B operates as a free-running clock generator. In this mode of operation the device requires a low cost fundamental mode crystal connected across XA and XB as shown in Figure 1. The crystal must meet the minimum requirements specified in section “1. Electrical Specifications” . Given the Si5356B’s frequency flexibility, the same crystal can be reused to generate any combination of output frequencies. Custom frequency crystals are not required. The Si5356B integrates the crystal load capacitors on-chip to reduce external component count. The crystal should be placed very close to the device to minimize stray capacitance. To ensure a stable and accurate output frequency, the recommended crystal specifications provided in Table 4 on page 6 must be followed. See AN360 for additional details regarding crystal recommendations.

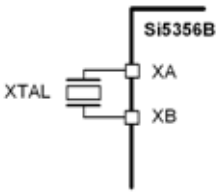


Figure 1. Connecting an XTAL to the Si5356B

For synchronous timing applications, the Si5356B can lock to a 5 to 200 MHz CMOS reference clock. A typical interface circuit is shown in Figure 2. A series termination resistor matching the driver’s output impedance to the impedance of the transmission line is recommended to reduce reflections.

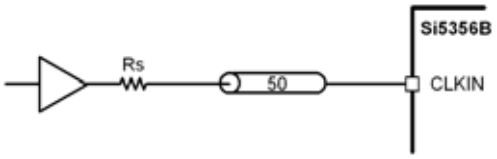


Figure 2. Interfacing CMOS Reference Clocks to the Si5356B

Control input signals to SSC_DIS and OEB cannot exceed 1.2 V yet also need to meet the V_{IH} and V_{IL} specifications outlined in Table 2 on page 4. When these inputs are driven from CMOS sources, a resistive attenuator as shown in the Typical Application Circuits must be used.

Suggested standard 1% resistor values for R_{SE} and R_{SH}, when using a CMOS source, are given below.

CMOS Level	R_{SE} (Ω)	R_{SH} (Ω)
1.8 V	1000	1580
2.5 V	1960	1580
3.3 V	3090	1580

3.2. MultiSynth Technology

Modern timing architectures require a wide range of frequencies which are often non-integer related. Traditional clock architectures address this by using a combination of single PLL ICs, 4-PLL ICs and discrete XOs, often at the expense of BOM complexity and power. The Si5356B uses patented MultiSynth technology to dramatically simplify timing architectures by integrating the frequency synthesis capability of 4 phase-locked loops (PLLs) in a single device, greatly minimizing size and power requirements versus traditional solutions. Based on a fractional-N PLL, the heart of the architecture is a low phase noise, high-frequency VCO. The VCO supplies a high frequency output clock to the MultiSynth block on each of the four independent output paths. Each MultiSynth operates as a high-speed fractional divider with Silicon Laboratories' proprietary phase error correction to divide down the VCO clock to the required output frequency with very low jitter.

The first stage of the MultiSynth architecture is a fractional-N divider which switches seamlessly between the two closest integer divider values to produce the exact output clock frequency with 0 ppm error. To eliminate phase error generated by this process, MultiSynth calculates the relative phase difference between the clock produced by the fractional-N divider and the desired output clock and dynamically adjusts the phase to match the ideal clock waveform. This novel approach makes it possible to generate any output clock frequency without sacrificing jitter performance. Based on this architecture, each clock output can produce any frequency from 1 to 200 MHz.

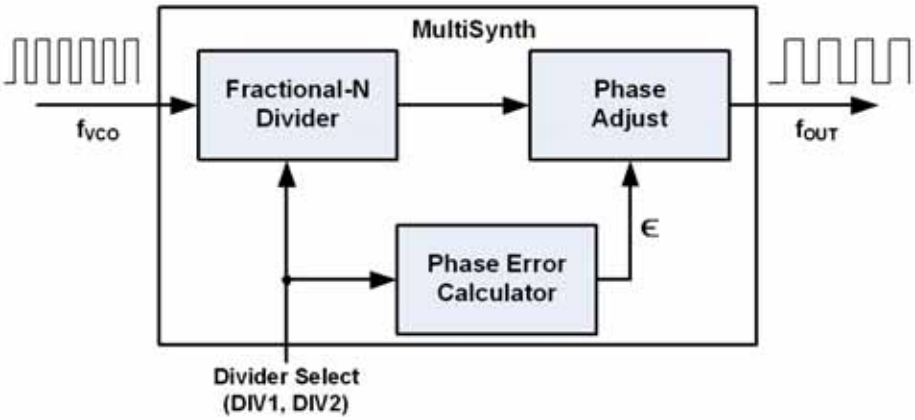


Figure 3. Silicon Labs' MultiSynth Technology

3.3. Input and Output Frequency Configuration

The Si5356B utilizes a single PLL-based architecture, four independent MultiSynth fractional output dividers, and a MultiSynth fractional feedback divider such that a single device provides the clock generation capability of 4 independent PLLs. Unlike competitive multi-PLL solutions, the Si5356B can generate four unique non-integer related output frequencies with 0 ppm frequency error for practically any combination of output frequencies. In addition, any combination of output frequencies can be generated from a single reference frequency without having to change the crystal or reference clock frequency between frequency configurations.

Frequency configurations are fully programmable by writing to device registers using the I^2C interface. Any combination of output frequencies ranging from 1 to 200 MHz can be configured on each of the device outputs.

The following equation governs how the output frequency is calculated.

$$f_{OUT} = \frac{f_{IN} \times N}{P \times M_i}$$

where f_{IN} is the reference frequency, N is the MultiSynth feedback divider value, P is the reference divider value, M_i is the MultiSynth output divider value and f_{OUT} is the resulting output frequency. The MultiSynth output and feedback dividers are fractional dividers expressed in terms of an integer and a fraction. The integer portion has 10-bit resolution and the fractional portion has 30-bit resolution in both the numerator and denominator, meaning that any output frequency can be defined exactly from the input frequency with exact (0 ppm) frequency synthesis error.

3.4. Configuring the Si5356B

Refer to the Si5356B Programming Guidelines for details on how to configure/program the device.

3.5. ClockBuilder™ Desktop Software

To simplify device configuration, Silicon Labs provides ClockBuilder Desktop software, which can operate standalone or in conjunction with an evaluation board (EVB)[1]. When the software is connected to the EVB, ClockBuilder will control both the core and I/O buffer supply voltages to the Si5356B, as well as the entire clock path within the Si5356B. Clockbuilder Desktop can also measure the current delivered by the EVB regulators to each supply voltage of the Si5356B. An Si5356B configuration can be written to a text file to be used by any system to configure the Si5356B via I^2C. ClockBuilder Desktop can be downloaded from www.silabs.com/ClockBuilder and runs on Windows XP, Windows Vista, and Windows 7[2].

Notes:

1. An Si5338-EVB (evaluation board) is used as the hardware platform for the Si5356B device. Contact your local Silicon Labs sales representative to order this evaluation platform for use with the Si5356B devices, or submit a request to www.silabs.com/support/Pages/contacttechnicalsupport.aspx.
2. For Si5356B evaluations, a custom ClockBuilder configuration file must be installed for proper operation of the Si5338-EVB. Contact Silicon Labs for access to the Si5356BClockBuilder configuration file, or submit a request to www.silabs.com/support/Pages/contacttechnicalsupport.aspx.

3.6. Output Phase Adjustment

The Si5356B has a digitally-controlled phase adjustment feature that allows the user to adjust the phase of each output clock in relation to the other output clocks. The phase of each output clock can be adjusted with an error of <20 ps over a range of ±45 ns. This feature is available on any clock output that does not have Spread Spectrum enabled.

3.7. CMOS Output Drivers

The Si5356B has 4 banks of outputs with each bank comprised of 2 clocks for a total of 8 CMOS outputs per device. By default, each bank of CMOS output clocks are in-phase. Alternatively, each output clock can be inverted. This feature enables each output pair to operate as a differential CMOS clock. Each of the output banks can operate from a different VDDO supply (1.8 V, 2.5 V, 3.3 V), simplifying usage in mixed supply applications. All clock outputs between 5 and 200 MHz are in-phase with minimal output-output skew.

The CMOS output driver has a controlled impedance of about 50 Ω, which includes an internal 22 Ω series resistor. An external series resistor is not needed when driving 50 Ω traces. If higher impedance traces are used then a series resistor may be added. A typical configuration is shown in Figure 4.

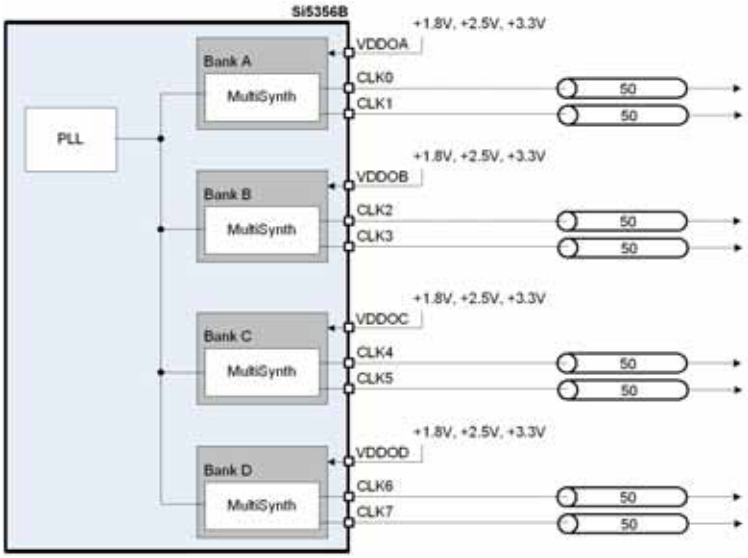


Figure 4. CMOS Output Driver Configuration

3.8. Jitter Performance

The Si5356B provides consistently low jitter for any combination of output frequencies. The device leverages a low phase noise single PLL architecture and Silicon Laboratories' patented MultiSynth fractional output divider technology to deliver excellent jitter performance for any frequency configuration. This level of jitter performance is guaranteed across process, temperature and voltage. The Si5356B provides superior performance to conventional multi-PLL solutions which may suffer from degraded jitter performance depending on frequency plan and the number of active PLLs.

Note: It is highly recommended that VDDO0 = 3.3 V when phase jitter on CLK0 is critical.

3.9. Status Indicators

A logic-high interrupt pin (INTR) is available to indicate a loss of signal (LOS) condition, a PLL loss of lock (PLL_LOL) condition, or that the PLL is in process of acquiring lock (SYS_CAL). PLL_LOL is held high when the input frequency drifts beyond the PLL lock range (approximately 5000 ppm). It is held low during all other times and during a POR or soft reset. SYS_CAL is held high during a POR or SOFT reset so that no chattering occurs during the locking process. As shown in Figure 5, a status register at address 218 is available to help identify the exact event that caused the interrupt pin to become active.

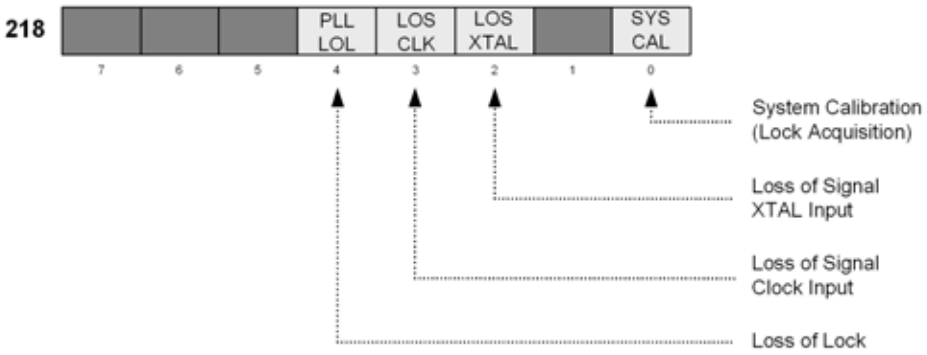


Figure 5. Status Register

Figure 6 shows a typical connection with the required pull-up resistor to VDD.

3.9.1. Using the INTR Pin in Systems with I²C

The INTR output pin is not latched and should not be a polled input to an MCU but an edge-triggered interrupt. An MCU can process an interrupt event by reading the status register at address 218, and it can be cleared by writing zeros to the bits that were set. Individual interrupt bits can be masked by register 6[4:0].

3.9.2. Using the INTR Pin in Systems without I²C

The INTR pin also provides a useful function in systems that require a pin-controlled fault indicator. Pre-setting the interrupt mask register allows the INTR pin to become an indicator for a specific event, such as LOS and/or LOL. Therefore, the INTR pin can be used to indicate a single fault event or even multiple events.

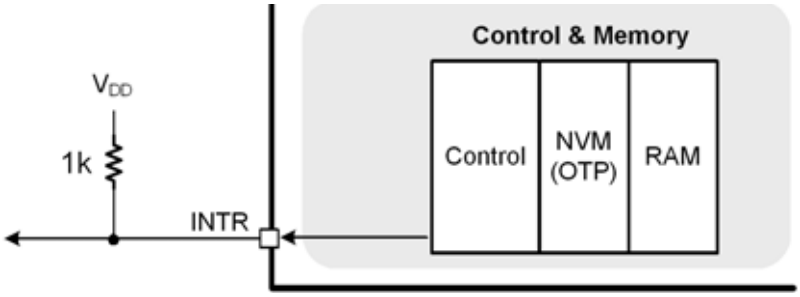


Figure 6. INTR Pin with Required Pull-Up

3.10. Output Enable

There are two methods of enabling and disabling the output drivers: Pin control, and I^2C control.

3.10.1. Enabling Outputs Using Pin Control

The Si5356B device provides an Output Enable pin (OEB) as shown in Figure 7. Pulling this pin high will turn all outputs off. The state of the individual drivers when turned off is controllable. If an individual output is set to always on, then the OEB pin will not have an effect on that driver. Drive state options and always on are explained in "3.10.2. Enabling Outputs through the I^2C Interface" .

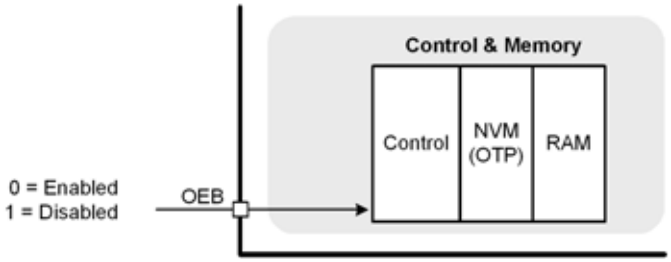


Figure 7. Output Enable Pin

3.10.2. Enabling Outputs through the I^2C Interface

Output enable can be controlled through the I^2C interface. As shown in Figure 8, register 230[3:0] allows control of each individual output driver. Register 230[4] controls all drivers at once. When register 230[4] is set to disable all outputs, the individual output enables will have no effect. Registers 110[7:6], 114[7:6], 118[7:6], and 112[7:6] control the output disabled state as tri-state, low, high, or always on. If always on is set, that output will always be on regardless of any other register or chip state.

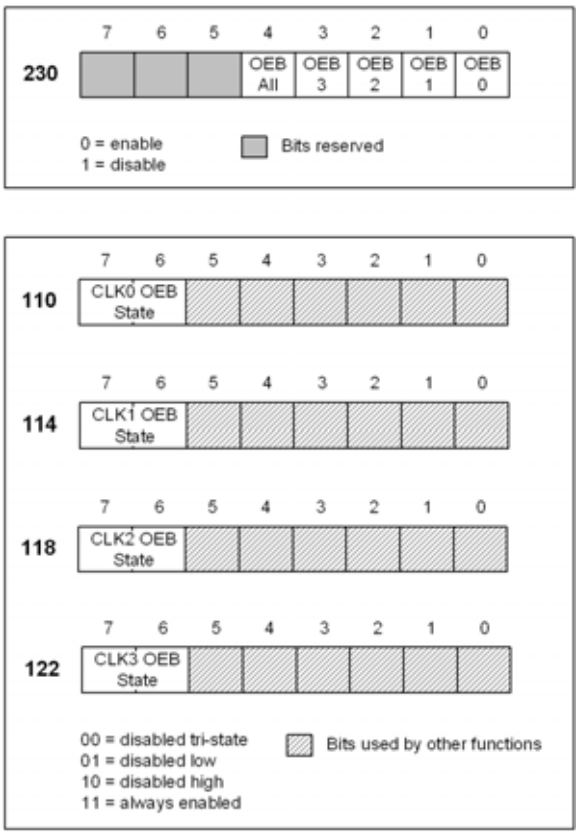


Figure 8. Output Enable Control Registers

3.11. Spread Spectrum

To help reduce electromagnetic interference (EMI), the Si5356B supports spread spectrum modulation. The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI. The Si5356B implements spread spectrum using its patented MultiSynth technology to achieve previously unattainable precision in both modulation rate and spreading magnitude as shown in Figure 9. Through I^2C control, the Spread Spectrum can be applied to any output clock, any clock frequency, and any spread amount from ±0.1% to ±2.5% center spread and –0.1% to –5% down spread.

The spreading rate is limited to 30 to 63 kHz.

The Spread Spectrum is generated digitally in the output MultiSynths which means that the Spread Spectrum parameters are virtually independent of process, voltage and temperature variations. Since the Spread Spectrum is created in the output MultiSynths, through I^2C each output channel can have independent Spread Spectrum parameters. Without the use of I^2C (NVM download only) the only supported Spread Spectrum parameters are for PCI Express compliance composing 100 MHz clock, 31.5 kHz spreading frequency with the choice of the spreading.

Rev A devices provide native support for both down and center spread. Center spread is supported in rev B devices by up-shifting the nominal frequency and using down-spread register parameters.

Note: If you currently use center spread on a Revision A and would like to migrate to a Revision B device, you must generate a new register map using ClockBuilder Desktop. Center spread configurations for Revisions A and B are **not** compatible.

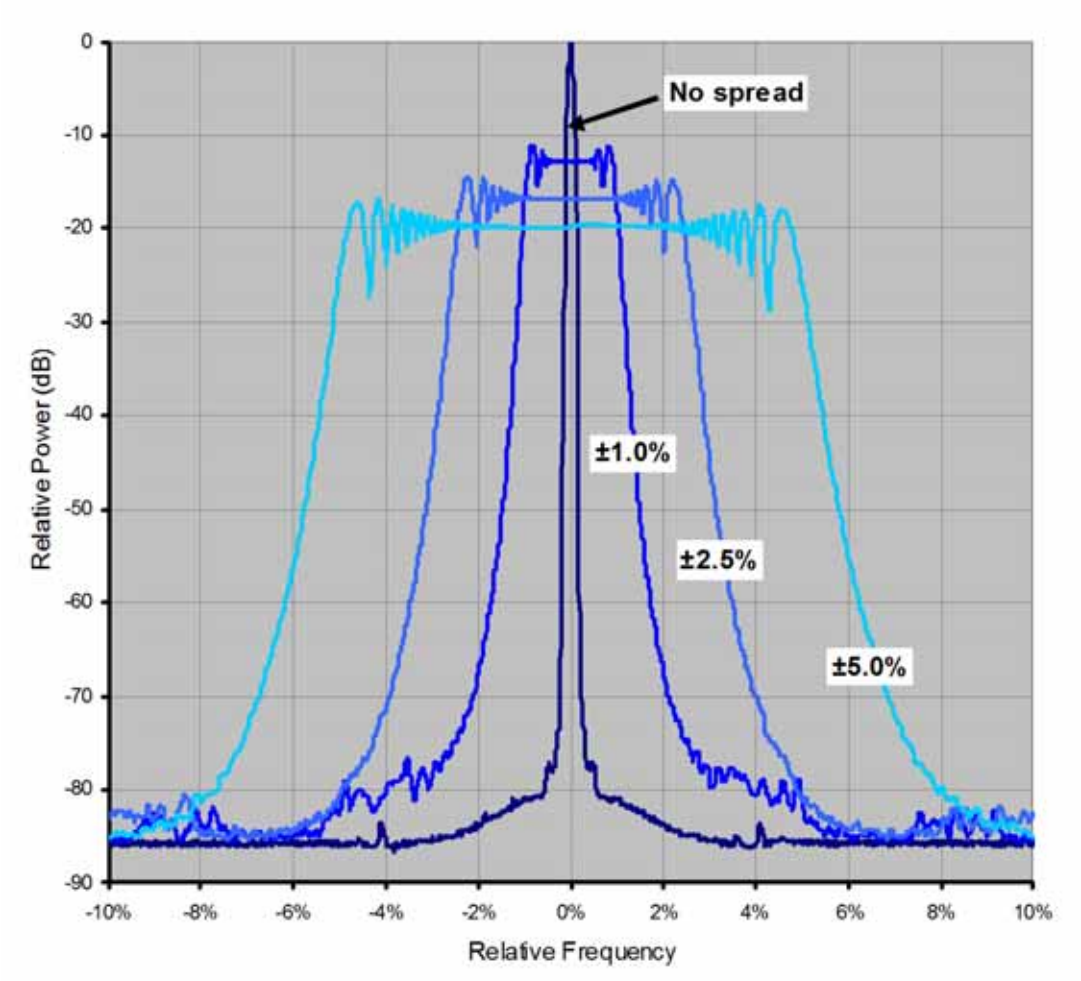


Figure 9. Configurable Spread Spectrum

3.12. Power Supply Considerations

The Si5356B has two core supply voltage pins (V_{DD}) and four clock output bank supply voltage pins (V_{DDOA}–V_{DDOD}), enabling the device to be used in mixed supply applications. The Si5356B does not typically require ferrite beads for power supply filtering. The device has extensive on-chip power supply regulation to minimize the impact of power supply noise on output jitter. Figure 10 shows that the additive phase jitter created when a significant amount of noise is applied to the device power supply is very small.

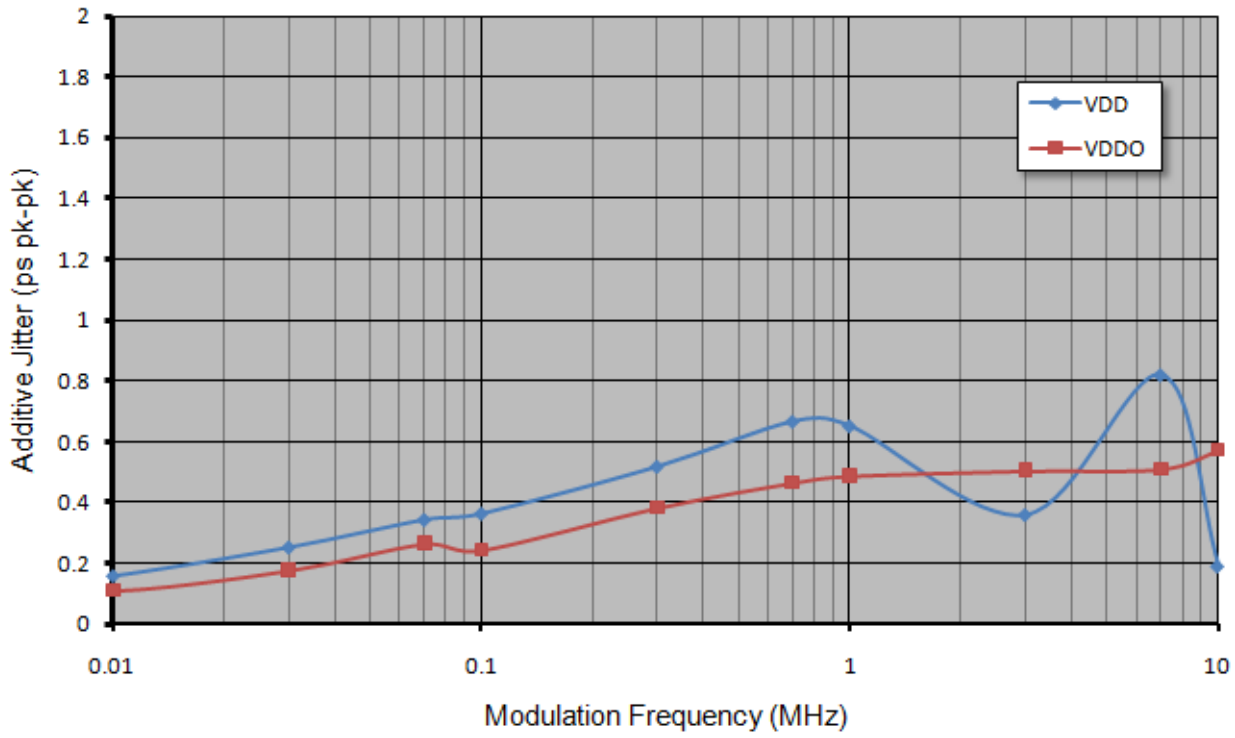


Figure 10. Peak-to-Peak Additive Jitter from 100 mV Sine Wave on Supply

4. I²C Interface

Configuration and operation of the Si5356B is controlled by reading and writing to the RAM space using the I²C interface. The device operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments.

The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in Figure 11. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I²C specification.

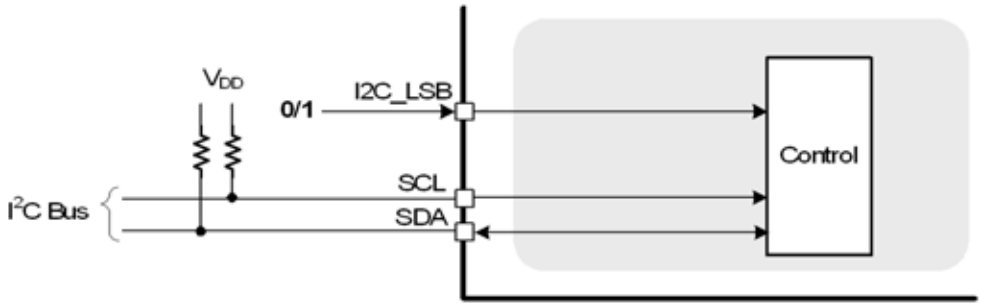


Figure 11. I²C and Control Signals

The 7-bit device (slave) address of the Si5356B consists of a 6-bit fixed address plus a user-selectable LSB bit as shown in Figure 12. The LSB bit is selectable using the optional I2C_LSB pin which is available as an programming option for applications that require more than one Si5356B on a single I²C bus. Devices without the I2C_LSB pin option have a fixed 7-bit address of 70h (111 0000) as shown in Figure 12. Other custom I²C addresses are also possible.

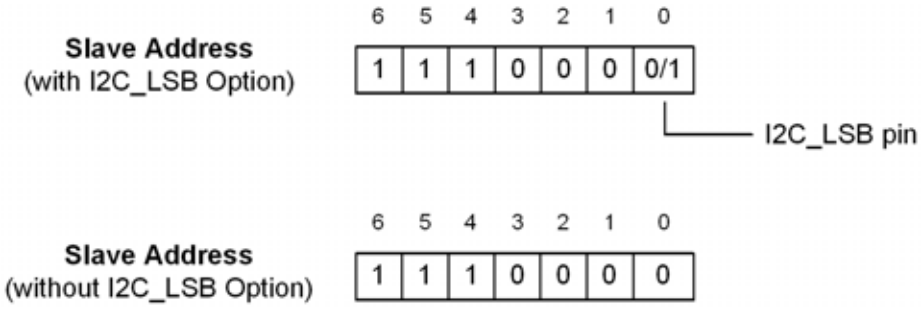


Figure 12. Si5356B I²C Slave Address

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in Figure 13. A write burst operation is also shown where every additional data word is written using an auto-incremented address.

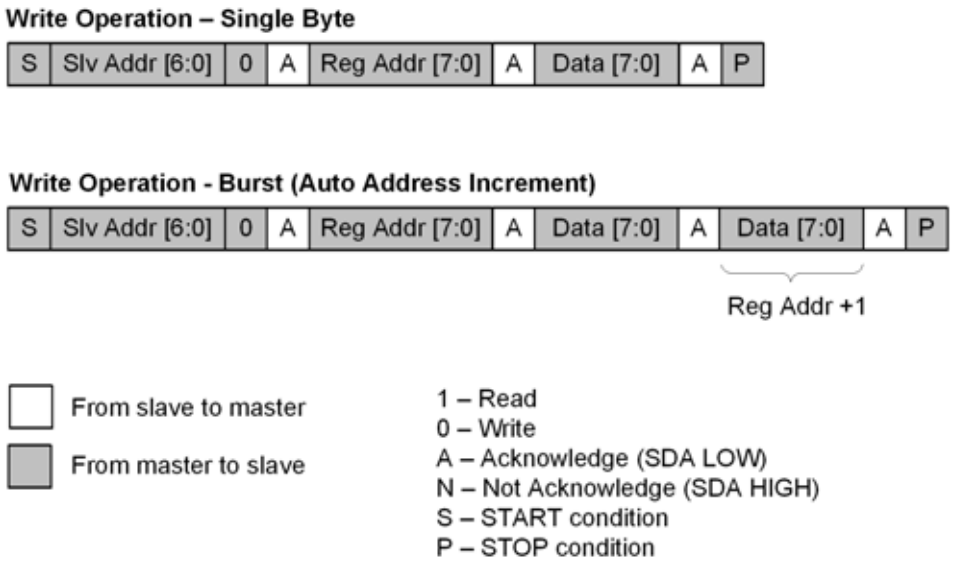


Figure 13. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in Figure 14.

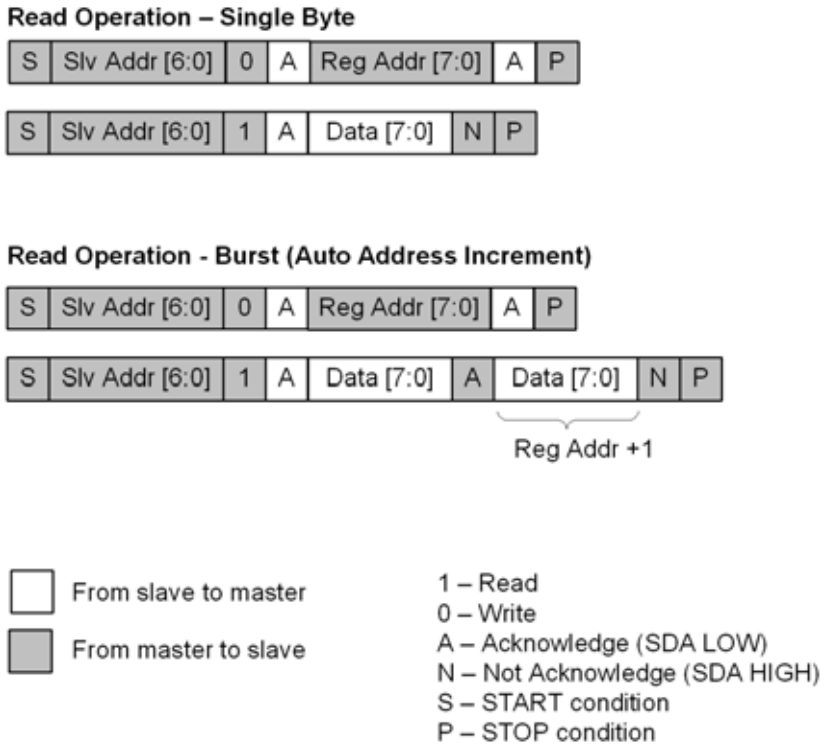


Figure 14. I²C Read Operation

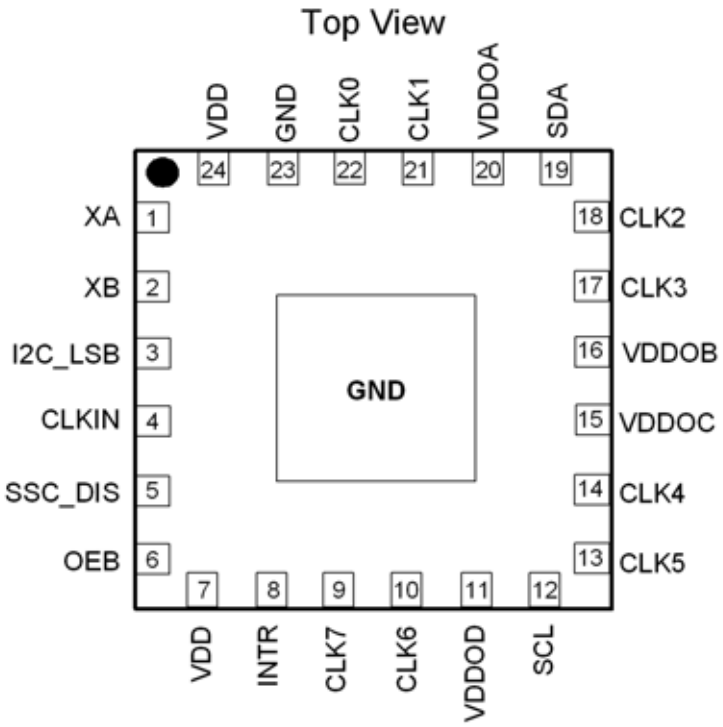
AC and DC electrical specifications for the SCL and SDA pins are shown in Table 6. The timing specifications and timing diagram for the I^2C bus are compatible with the I^2C-Bus Standard. SDA timeout is supported for compatibility with SMBus interfaces.

The I^2C bus can be operated at a bus voltage of 1.71 to 3.63 V and is 3.3 V tolerant. If a bus voltage of less than 2.5 V is used, register 27[7] = 1 must be written to maintain compatibility with the I^2C bus standard.

4.1. Custom Device Configurations

The Si5356B is fully configurable by writing to internal registers through the I^2C interface. After each power cycle the register settings are restored to their factory default values. For applications that require a custom configuration at power-up, the Si5356B is orderable with a custom default register setting. See "8. Ordering Guide" on page 25 more for details.

5. Pin Descriptions



Note: Center pad must be tied to GND for normal operation.

Table 9. Si5356B Pin Descriptions

Pin #	Pin Name	I/O	Description
1	XA	I	**External Crystal.** If a crystal is used as the device frequency reference, connect it across XA and XB. If no input clock is used, this pin should be tied to GND.
2	XB	I	**External Crystal.** If a crystal is used as the device frequency reference, connect it across XA and XB. If no input clock is used, this pin should be tied to GND.
3	I2C_LSB	I	**I^2C LSB Address Bit** This pin is the least significant bit of the Si5356B I^2C address allowing up to two Si5356B devices to occupy the same I^2C bus.
4	CLKIN	I	**Single-Ended Input Clock.** If a single-ended clock is used as the device frequency reference, connect it to this pin. This pin functions as a high-impedance input for CMOS clock signals. The input should be dc coupled. If a crystal is used as the device frequency reference, this pin should be tied to GND.

Table 9. Si5356B Pin Descriptions (Continued)

5	SSC_DIS	I	**Spread Spectrum Disable.** This pin allows disabling of the spread spectrum feature on the output clocks. Connect to 1.2 V to disable spread spectrum on all outputs. Connect to GND to enable spread spectrum. Note that the maximum voltage level on this pin must not exceed 1.2 V. A resistor voltage divider is recommended when controlled by a signal greater than 1.2 V. See the Typical Application Circuit for details.
6	OEB	I	**Output Enable (Active Low)** This pin allows disabling the output clocks. Connect to 1.2 V to disable all outputs. Connect to GND to enable all outputs. Note that the maximum voltage level on this pin must not exceed 1.2 V. A resistor voltage divider is recommended when controlled by a signal greater than 1.2 V. See the Typical Application Circuit for details.
7	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
8	INTR	O	**Interrupt** This pin functions as an maskable interrupt output. 0 = No interrupt 1 = Interrupt present This pin is open drain and requires an external ≥1 kΩ pullup resistor.
9	CLK7	O	**Output Clock 7.** CMOS output clock. If unused, this pin must be left floating.
10	CLK6	O	**Output Clock 6.** CMOS output clock. If unused, this pin must be left floating.
11	VDDOD	VDD	**Clock Output Bank D Supply Voltage.** Power supply for clock outputs 6 and 7. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK6/7 are not used, this pin must be tied to pin 7 and/or pin 24.
12	SCL	I	**I^2C Serial Clock Input.**
13	CLK5	O	**Output Clock 5.** CMOS output clock. If unused, this pin must be left floating.
14	CLK4	O	**Output Clock 4.** CMOS output clock. If unused, this pin must be left floating.
15	VDDOC	VDD	**Clock Output Bank C Supply Voltage.** Power supply for clock outputs 4 and 5. May be operated from a 1.8, 2.5 or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK4/5 are not used, this pin must be tied to pin 7 and/or pin 24.
16	VDDOB	VDD	**Clock Output Bank B Supply Voltage.** Power supply for clock outputs 2 and 3. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK2/3 are not used, this pin must be tied to pin 7 and/or pin 24.
17	CLK3	O	**Output Clock 3.** CMOS output clock. If unused, this pin must be left floating.
18	CLK2	O	**Output Clock 2.** CMOS output clock. If unused, this pin must be left floating.

Table 9. Si5356B Pin Descriptions (Continued)

19	SDA	I/O	**I^2C Serial Data.**
20	VDDOA	VDD	**Clock Output Bank A Supply Voltage.** Power supply for clock outputs 0 and 1. May be operated from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin. If CLK0/1 are not used, this pin must be tied to pin 7 and/or pin 24.
21	CLK1	O	**Output Clock 1.** CMOS output clock. If unused, this pin must be left floating.
22	CLK0	O	**Output Clock 0.** CMOS output clock. If unused, this pin must be left floating.
23	GND	GND	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of the device.
24	VDD	VDD	**Core Supply Voltage.** The device operates from a 1.8, 2.5, or 3.3 V supply. A 0.1 µF bypass capacitor should be located very close to this pin.
GND PAD	GND	GND	**Ground Pad.** This is the large pad in the center of the package. The device will not function unless the ground pad is properly connected to a ground plane on the PCB. See "7. Recommended PCB Land Pattern" on page 24 for the PCB pad sizes and ground via requirements.

6. Package Outline: 24-Lead QFN

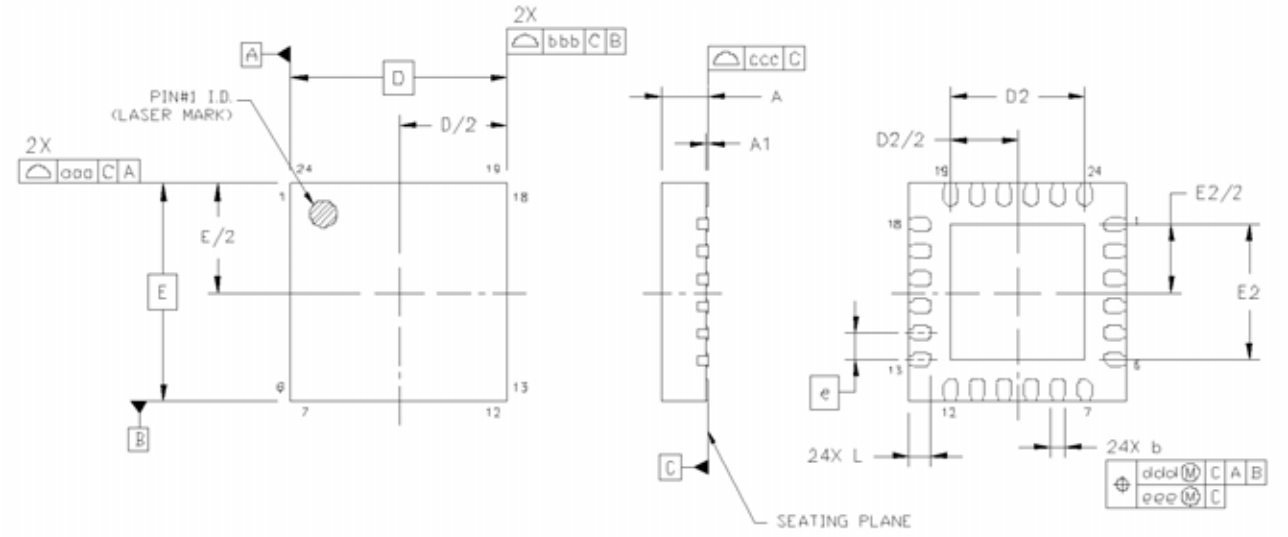


Figure 15. 24-Lead Quad Flat No-Lead (QFN)

Table 10. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		4.00 BSC.	
D2	2.35	2.50	2.65
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.35	2.50	2.65
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Outline MO-220, variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
5. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.

7. Recommended PCB Land Pattern

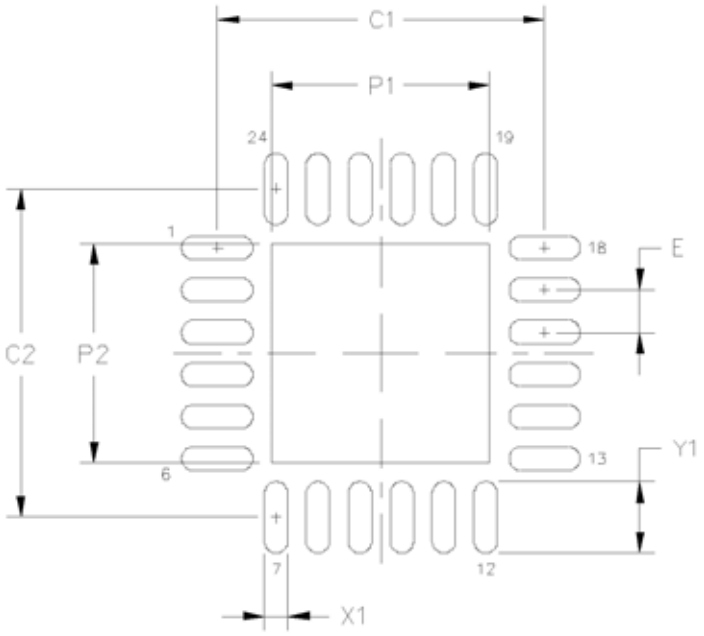


Table 11. PCB Land Pattern

Dimension	Min	Nom	Max
P1	2.50	2.55	2.60
P2	2.50	2.55	2.60
X1	0.20	0.25	0.30
Y1	0.75	0.80	0.85
C1	3.90		
C2	3.90		
E	0.50		

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. Connect the center ground pad to a ground plane with no less than five vias. These 5 vias should have a length of no more than 20 mils to the ground plane. Via drill size should be no smaller than 10 mils. A longer distance to the ground plane is allowed if more vias are used to keep the inductance from increasing.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

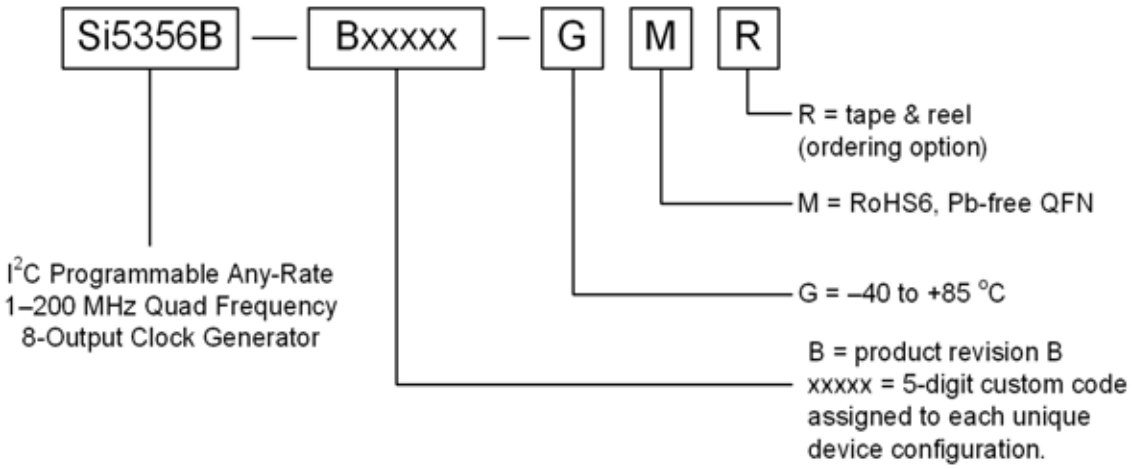
Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.
9. A 2x2 array of 1.0 mm square openings on 1.25 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Ordering Guide



8.1. Custom Part Numbers

The Si5356B includes the following part numbers with start-up configurations as listed inTable 12. Refer to the Si5365B Programming Guidelines document for additional Si5365B part numbers and validated configurations.

Table 12. Customer Part Numbers

Custom Part Number	Input	CLK0	CLK1	CLK2	CLK3	CLK4	CLK5	CLK6	CLK7
Si5356B-B00322-GM	25 MHz	25 MHz	25 MHz	33.333 MHz	Unused	48 MHz	Unused	27.648 MHz	Unused
	XTAL	2.5 V	2.5 V	3.3 V		3.3 V		3.3 V	
	XA/XB	CMOS	CMOS	CMOS		CMOS		CMOS	
Si5356B-B01139-GM	25 MHz	50 MHz	Unused	50 MHz	Unused	48 MHz	Unused	27.648 MHz	Unused
	XTAL	3.3 V		3.3 V		3.3 V		3.3 V	
	XA/XB	CMOS		CMOS		CMOS		CMOS	

9. Top Marking

9.1. Si5356B Top Marking

9.2. Top Marking Explanation

Line	Characters	Description
Line 1	Si5356	Base part number.
Line 2	Bxxxxx	B = 200 MHz, CMOS, I^2C programmable clock generator series. xxxxx = Optional NVM code for custom factory-programmed devices. These 5 characters are not included for standard, factory default configured devices. IBM NVM configuration code #1=00322. See Section “8.1. Custom Part Numbers” for configuration details.
Line 3	RTTTTT	R = Product revision. TTTTT = Manufacturing trace code.
Line 4	Circle with 0.5 mm diameter; left-justified	Pin 1 indicator.
	YYWW	YY = Year. WW = Work week Characters correspond to the year and work week of package assembly.

10. Device Errata

Please visit www.silabs.com to access the device errata document.

Document Change List

Revision 0.1 to Revision 0.2

- Updated crystal specifications to include crystal frequencies of 19 to 30 MHz.
- Updated section “3.4. Configuring the Si5356B” .
- Removed section 3.10 Reset Options.
- Moved section 4.2 Spread Spectrum to section “3.11. Spread Spectrum” .
- Moved section 4.3 Power Supply Considerations to section “3.12. Power Supply Considerations” .
- Added section “9. Top Marking” .

Revision 0.2 to Revision 0.3

- Added Si5356B-A01139-GM to Section 8.1 as a new validated part number conforming to data sheet specifications.
- Corrected CMOS output clock t_R/t_F time (20 to 80%, 15 pF load) from 1.7 ns (max) to 2.0 ns (max) to better reflect characterization data.
- Clarified crystal specifications in Tables 6 and 7 and added reference to AN360.
- Corrected Figure 5. Status Registers to show the correct position of LOS_XTAL and LOS_CLK..
- Removed reference to the Si5338K/L/M in the output enable control section.
- Updated application circuits to make reference to the Si5356B.

Revision 0.3 to Revision 1.0

- Updated Table 2, “DC Characteristics,” on page 4.
  - Corrected I_{DDOX} from "—" (typ) to 6 mA (typ), and 28 mA (max) to 9 mA (max).
  - Corrected R_{IN} from 20 kΩ (min) to 20 kΩ (typ).
- Updated Table 3, “AC Characteristics,” on page 5.
  - Input clock T_R/T_F from 2 ns (max) to 2.3 ns (max).
  - Corrected C_L from 15 pF (typ) to 15 pF (max).
  - Corrected F_{RES} from 0 ppm (max) to 1 ppb (max).
  - Added Interrupt Status Timing.
- Added soldering temperature time T_{PEAK} to Table 8.
- Corrected references to V_{IH} and V_{IL} in Section 3.1.
- Removed output-output skew reference from text of Section 3.7 (see Table 3—AC Characteristics).
- Clarified status alarm register info in Section 3.9.1.
- Removed erroneous reference to ZDB mode.

Revision 1.0 to Revision 1.1

- Removed down spectrum errata that has been corrected in revision B.
- Updated ordering information to refer to revision B silicon.
- Updated top marking explanation in Section 9.1.
- Added further explanation to describe revision-specific behavior of center spread spectrum in Section 3.11.

Revision 1.1 to Revision 1.2

- Added link to errata document.

Revision 1.3 to Revision 1.4

- Removed MSL rating.

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