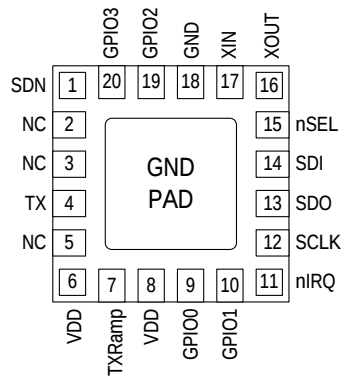
Si4063/60-C

HIGH-PERFORMANCE, LOW-CURRENT TRANSMITTER

Features

- Frequency range = 142–1050 MHz
- Modulation
  - (G)FSK, 4(G)FSK, (G)MSK
  - OOK
- Max output power
  - +20 dBm (Si4063)
  - +13 dBm (Si4060)
- PA support for +27 or +30 dBm
- Ultra low current powerdown modes
  - 30 nA shutdown, 40 nA standby
- Data rate = 100 bps to 1 Mbps
- Fast wake times
- Power supply = 1.8 to 3.8 V
- Highly configurable packet handler
- TX 129 byte FIFO
- Low BOM
- Low battery detector
- Temperature sensor
- 20-Pin QFN package
- IEEE 802.15.4g compliant
- Suitable for FCC Part 90 Mask D, FCC part 15.247, 15,231, 15,249, ARIB T-108, T-96, T-67, China regulatory ETSI EN 300 220

Pin Assignments



Patents pending

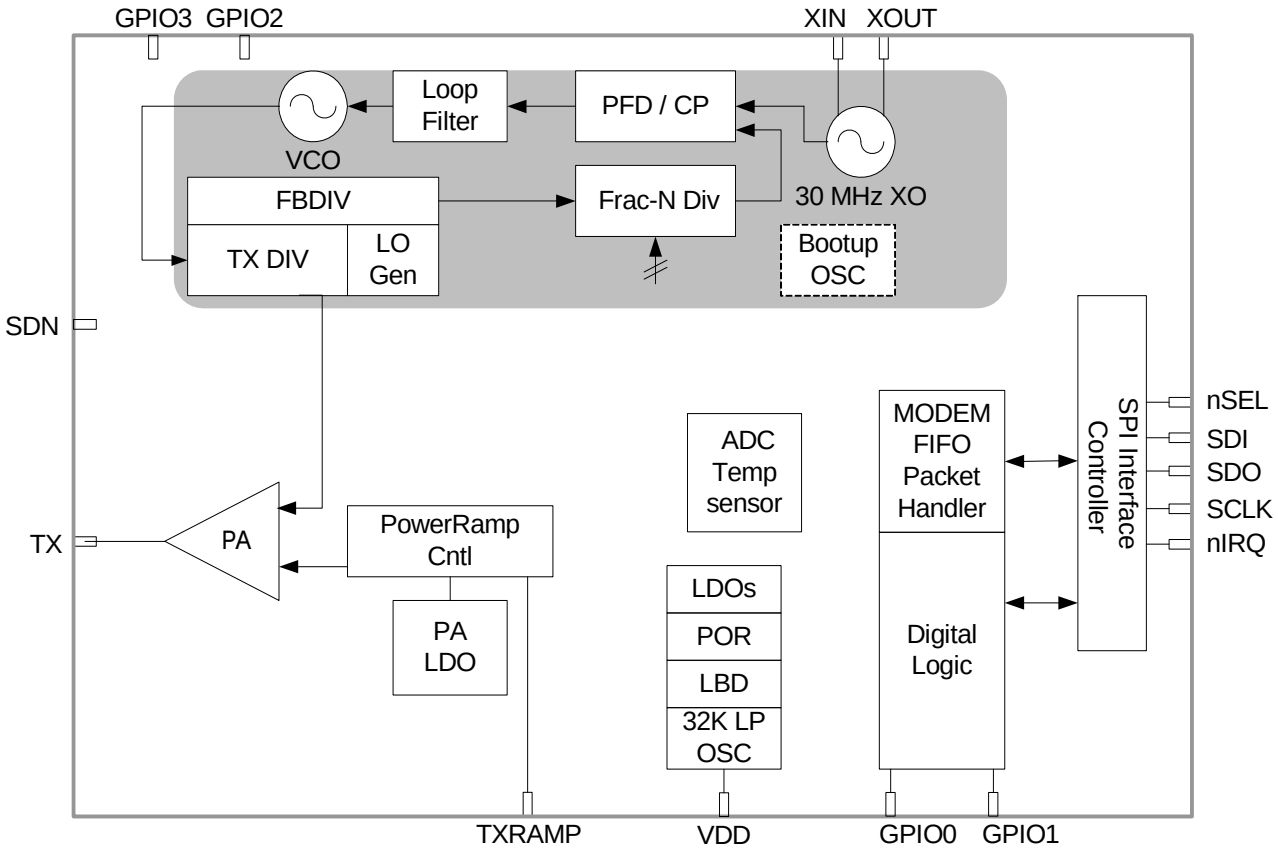
Applications

- Smart metering
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Electronic shelf labels

Description

Silicon Laboratories' Si406x devices are high-performance, low-current transmitters covering the sub-GHz frequency bands from 142 to 1050 MHz. The radios are part of the EZRadioPRO® family, which includes a complete line of transmitters, receivers, and transceivers covering a wide range of applications. All parts offer extremely low active and standby current consumption. The Si406x includes optimal phase noise performance for narrow band applications, such as FCC Part90 and 169 MHz wireless Mbus. The Si4063 offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power allows extended ranges and highly robust communication links. The Si4060 active mode TX current consumption of 18 mA at +10 dBm coupled with extremely low standby current and fast wake times ensure extended battery life in the most demanding applications. The Si4063 can achieve up to +27 dBm output power with built-in ramping control of a low-cost external FET. The devices can meet worldwide regulatory standards: FCC, ETSI, wireless MBus, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards. The devices are highly flexible and can be configured via the Wireless Development Suite (WDS) available at Silicon Labs web site.

Functional Block Diagram



Product	Freq. Range	Max Output Power	TX Current	Narrowband Operation
Si4063	Major bands 142–1050 MHz	+20 dBm	169 MHz: 68.5 mA	✓
Si4060	Major bands 142–1050 MHz	+13 dBm	+10 dBm: 18 mA +13 dBm: 24 mA	✓

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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.8	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	—	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	—	nA
	$I_{SleepRC}$	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF	—	740	—	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal.	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
TUNE Mode Current	I_{Tune_TX}	TX Tune, High Performance Mode	—	7.8	—	mA
TX Mode Current (Si4063)	I_{TX_+20}	+20 dBm output power, class-E match, 915 MHz, 3.3 V	—	88	—	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	68.5	—	mA
TX Mode Current (Si4060)	I_{TX_+10}	+10 dBm output power, Class-E match, 169 MHz, 3.3 V[2]	—	18	—	mA
	I_{TX_+13}	+13 dBm output power, Class-E match, 915/868 MHz, 3.3 V[2]	—	24	—	mA

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. Measured on direct tie RF evaluation board.

Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range (Si4063/60)	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution[2]	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	284–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise	$L\phi(f_M)$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	—	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	—	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	—	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	—	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	—	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	—	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	—	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	—	dBc/Hz

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. Default API setting for modulation deviation resolution is double the typical value specified.

Table 3. Transmitter AC Electrical Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate[2]	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate[2]	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate[2]	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	284–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution[3]	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	284–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Output Power Range (Si4063)[4]	P_{TX63}	Typical range at 3.3 V with Class E match optimized for best PA efficiency	–20	—	+20	dBm
Output Power Range (Si4060)[4]	P_{TX60}	Typical range at 3.3 V with Class E match optimized for best PA efficiency. Efficiency can be traded off for higher Tx output power up to +13 dBm.	–20	—	+12.5	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	—	dB
Output Power Variation (Si4063)		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 3. Transmitter AC Electrical Characteristics[1] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power Variation (Si4060)		At 10 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	9.5	10	10.5	dBm
Output Power Variation (Si4063)		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
Output Power Variation (Si4060)		At 10 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	—	10	—	dBm
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	—	dB
TX RF Output Level Variation vs. Frequency	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.6	—	dB
Transmit Modulation Filtering	B*T	Gaussian Filtering Bandwith Time Product	—	0.5	—	

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Sensor Sensitivity	TS_S		—	4.5	—	ADC Codes/ °C
Low Battery Detector Resolution	LBD_{RES}		—	50	—	mV
Microcontroller Clock Output Frequency Range[2]	F_{MC}	Configurable to Fxtal or Fxtal divided by 2, 3, 7.5, 10, 15, or 30 where Fxtal is the reference XTAL frequency. In addition, 32.768 kHz is also supported.	32.768K	—	Fxtal	Hz
Temperature Sensor Conversion	$TEMP_{CT}$	Programmable setting	—	3	—	ms
XTAL Range[3]	$XTAL_{Range}$		25	—	32	MHz
30 MHz XTAL Start-Up Time	t_{30M}	Using XTAL and board layout in reference design. Start-up time will vary with XTAL type and board layout.	—	300	—	µs
30 MHz XTAL Cap Resolution	$30M_{RES}$		—	70	—	fF
32 kHz XTAL Start-Up Time	t_{32k}		—	2	—	sec
32 kHz Accuracy using Internal RC Oscillator	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	—	6	ms

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. Microcontroller clock frequency tested in production at 1 MHz, 30 MHz, 32 MHz, and 32.768 kHz. Other frequencies tested in bench characterization.
3. XTAL Range tested in production using an external clock source (similar to using a TCXO).

Table 5. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ, SDN)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time[2,3]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time[3,4]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–1	—	1	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	µA
Drive Strength for Output Low Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	1.13	—	mA
Drive Strength for Output High Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.96	—	mA
Drive Strength for Output High Level for GPIO0	I_{OmaxLL}	DRV[1:0] = LL[3]	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	1.7	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. 6.7 ns is typical for GPIO0 rise time.
3. Assuming VDD = 3.3 V, drive strength is specified at Voh (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.
4. 2.4 ns is typical for GPIO0 fall time.

Table 6. Thermal Characteristics

Parameter	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Thermal Impedance Junction to Ambient	θ_{JA}	25	°C/W
Junction Temperature Maximum Value	T_j	+105	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C
Note: Thermal impedance and junction temperature values are based on RF evaluation board measurements.			

Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.8	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Analog Inputs	–0.7, V_{DD} + 0.3	V
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.		

2. Functional Description

The Si406x devices are high-performance, low-current, wireless ISM transmitters that cover the sub-GHz bands. The wide operating voltage range of 1.8–3.8 V and low current consumption make the Si406x an ideal solution for battery powered applications.

A single high precision local oscillator (LO) is used for transmit mode. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 100 bps to 1 Mbps. The Si4063/60 operate in the frequency bands of 142–175, 283–350, 350–525, and 850–1050 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The Si4063/60 contains a power amplifier (PA) that supports output power up to +20 dBm with very high efficiency, consuming only 70 mA at 169 MHz and 85 mA at 915 MHz. The integrated +20 dBm power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The Si4060 is designed to support single coin cell operation with current consumption below 18 mA for +10 dBm output power. Two match topologies are available for the Si4060, Class-E and switched-current. Class-E matching provides optimal current consumption, while switched-current matching demonstrates the best performance over varying battery voltage and temperature with slightly higher current consumption. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The Si406x family supports frequency hopping to extend the link range and improve performance. A highly configurable packet handler allows for autonomous encoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, and 129 byte TX FIFOs, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The Si406x is designed to work with an MCU, crystal, and a few passive components to create a very low-cost system.

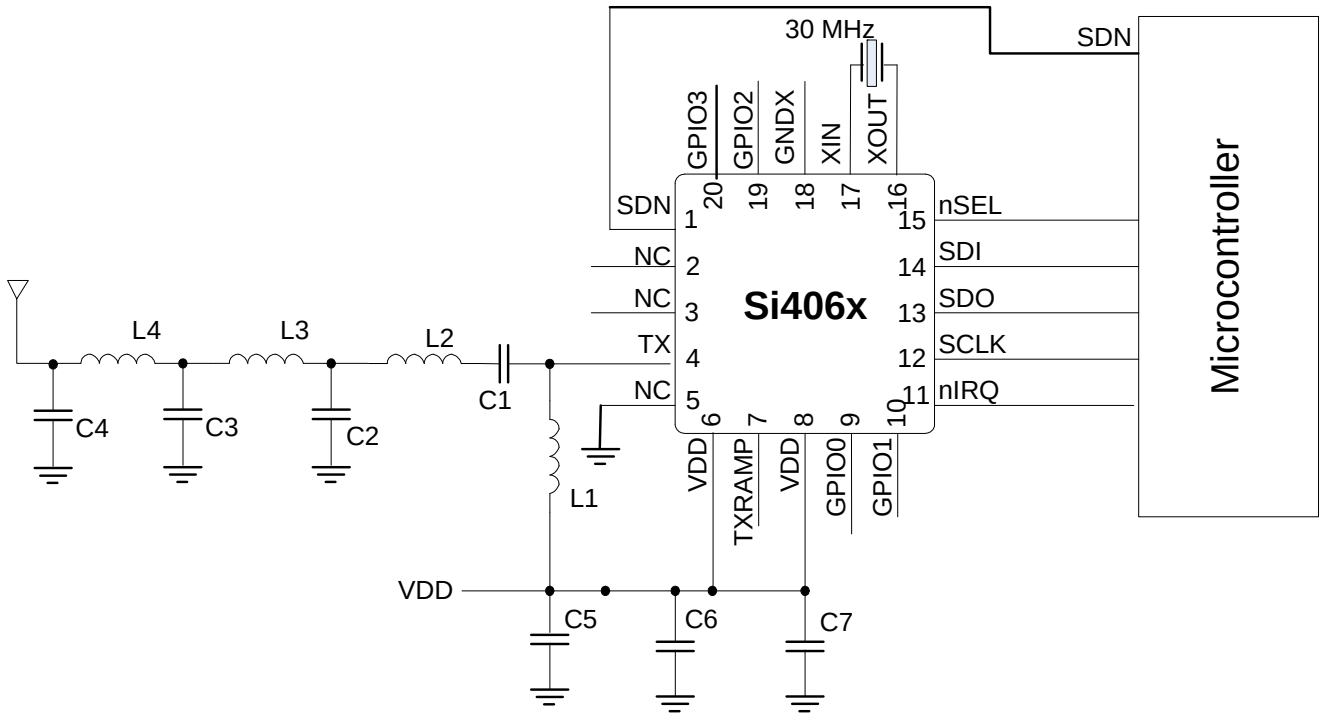


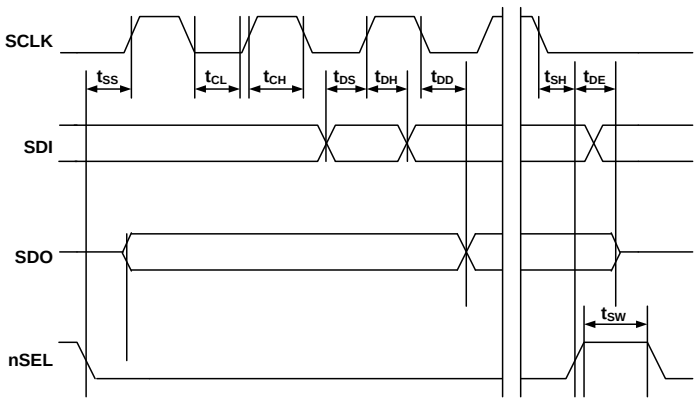
Figure 1. Si406x Application Example

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The Si406x communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI, SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 8. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 2 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 8. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Max (ns)	Diagram
t_{CH}	Clock high time	40		
t_{CL}	Clock low time	40		
t_{DS}	Data setup time	20		
t_{DH}	Data hold time	20		
t_{DD}	Output data delay time		43	
t_{DE}	Output disable time		45	
t_{SS}	Select setup time	20		
t_{SH}	Select hold time	50		
t_{SW}	Select high period	80		

***Note:** CL = 10 pF; VDD = 1.8 V; SDO Drive strength setting = 10.

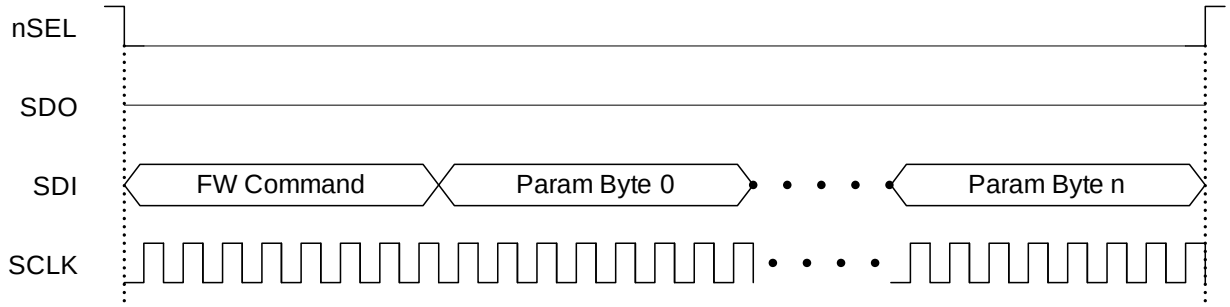
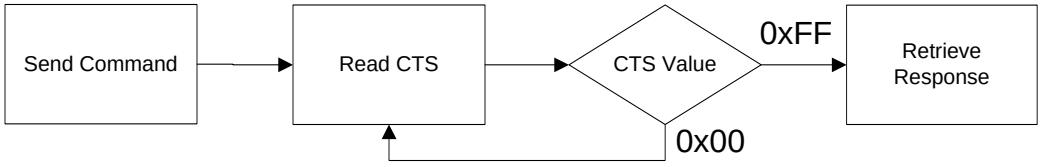


Figure 2. SPI Write Command

The Si406x contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 3 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 4 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

Firmware Flow



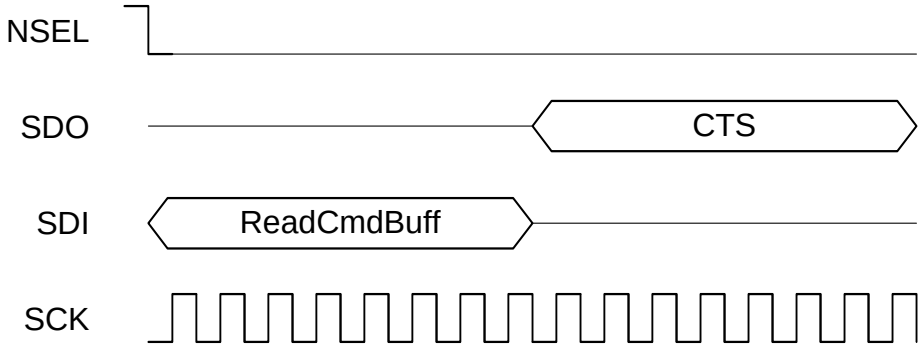


Figure 3. SPI Read Command—Check CTS Value

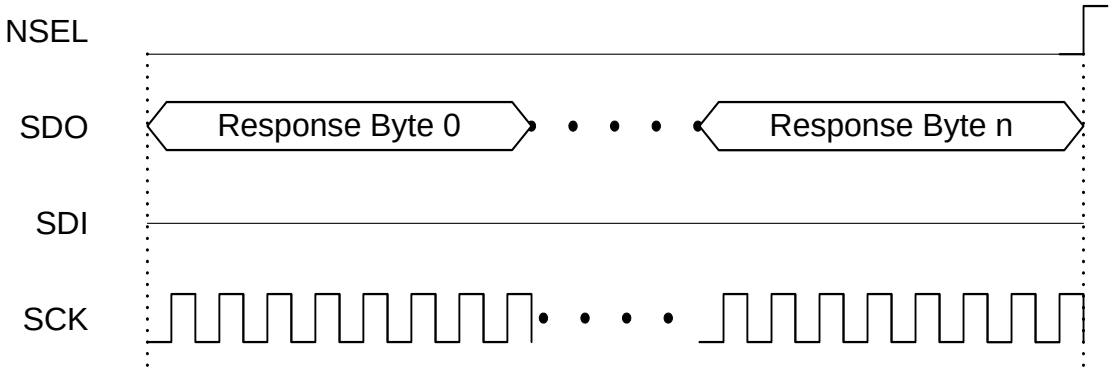


Figure 4. SPI Read Command—Clock Out Read Data

3.2. Fast Response Registers

The fast response registers are registers that can be read immediately without the requirement to monitor and check CTS. There are four fast response registers that can be programmed for a specific function. The fast response registers can be read through API commands, 0x50 for Fast Response A, 0x51 for Fast Response B, 0x53 for Fast Response C, and 0x57 for Fast Response D. The fast response registers can be configured by the “FRR_CTL_X_MODE” properties.

The fast response registers may be read in a burst fashion. After the initial 16 clock cycles, each additional eight clock cycles will clock out the contents of the next fast response register in a circular fashion. The value of the FRRs will not be updated unless NSEL is toggled.

3.3. Operating Modes and Timing

The primary states of the Si406x are shown in Figure 5. The shutdown state completely shuts down the radio to minimize current consumption. Standby/Sleep, SPI Active, Ready, and TX Tune are available to optimize the current consumption and response time to TX for a given application. The API commands, START_TX and CHANGE_STATE, control the operating state with the exception of shutdown which is controlled by SDN, pin 1. Table 9 shows each of the operating modes with the time required to reach TX mode as well as the current consumption of each mode. The times in Table 9 are measured from the rising edge of nSEL until the chip is in the desired state. Note that these times are indicative of state transition timing but are not guaranteed and should only be used as a reference data point. An automatic sequencer will put the chip into TX from any state. It is not necessary to manually step through the states. To simplify the diagram it is not shown but any of the lower power states can be returned to automatically after TX.

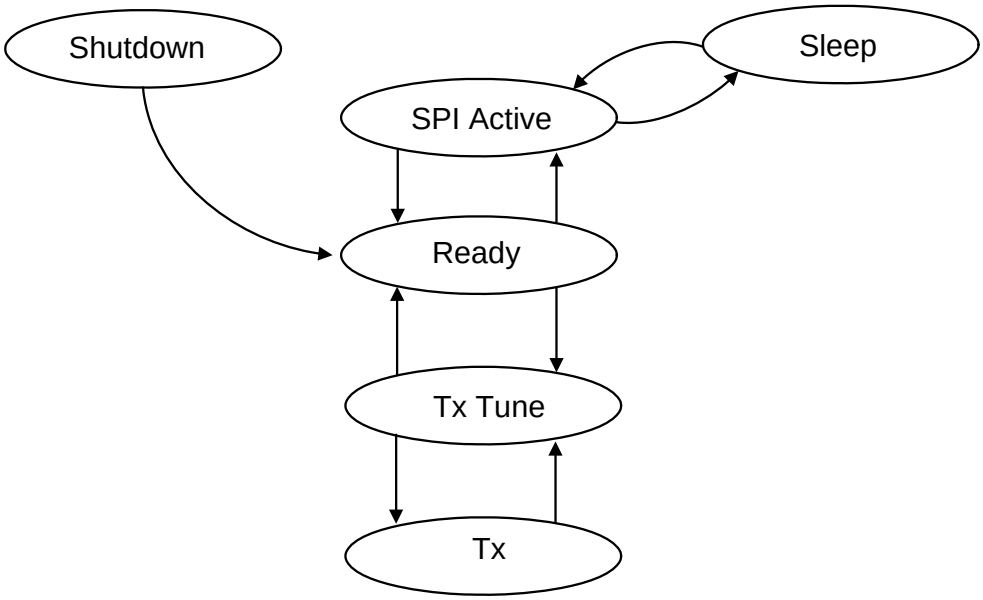


Figure 5. State Machine Diagram

Table 9. Operating State Response Time and Current Consumption*

State/Mode	Response Time to TX	Current in State /Mode
Shutdown State	15 ms	30 nA
Standby State Sleep State SPI Active State Ready State TX Tune State	440 µs 440 µs 340 µs 100 µs 58 µs	40 nA 740 nA 1.35 mA 1.8 mA 7.8 mA
TX State	—	18 mA @ +10 dBm

Figure 6 shows the POR timing and voltage requirements. The power consumption (battery life) depends on the duty cycle of the application or how often the part is in TX state. In most applications the utilization of the standby state will be most advantageous for battery life but for very low duty cycle applications shutdown will have an advantage. For the fastest timing the next state can be selected in the START_TX API commands to minimize SPI transactions and internal MCU processing.

3.3.1. Power on Reset (POR)

A Power On Reset (POR) sequence is used to boot the device up from a fully off or shutdown state. To execute this process, VDD must ramp within 1ms and must remain applied to the device for at least 10ms. If VDD is removed, then it must stay below 0.15V for at least 10ms before being applied again. Please see Figure x and Table x for details.

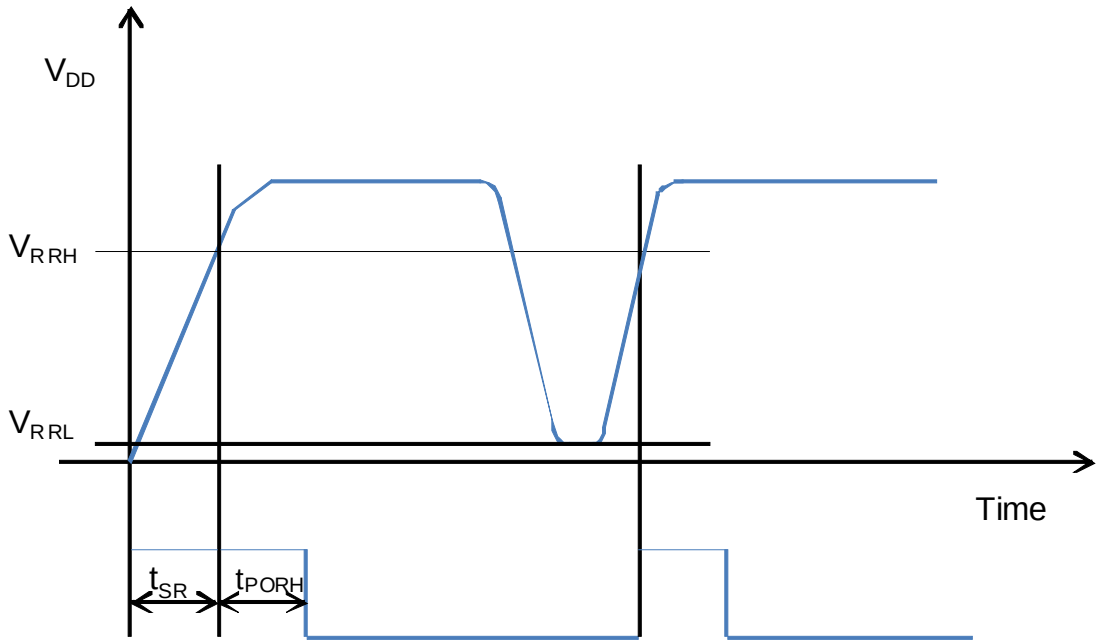


Figure 6. POR Timing Diagram

Table 10. POR Timing

Variable	Description	Min	Typ	Max	Units
t_{PORH}	High time for VDD to fully settle POR circuit.	10			ms
t_{PORL}	Low time for VDD to enable POR.	10			ms
V_{RRH}	Voltage for successful POR	90%*Vdd			V
V_{RRL}	Starting Voltage for successful POR	0		150	mV
t_{SR}	Slew rate of VDD for successful POR			1	ms

3.3.2. Shutdown State

The shutdown state is the lowest current consumption state of the device with nominally less than 30 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 1) high. The SDN pin should be held low in all states except the shutdown state. In the shutdown state, the contents of the registers are lost and there is no SPI access. When coming out of the shutdown state a power on reset (POR) will be initiated along with the internal calibrations. After the POR the POWER_UP command is required to initialize the radio. The SDN pin needs to be held high for at least 10us before driving low again so that internal capacitors can discharge. Not holding the SDN high for this period of time may cause the POR to be missed and the device to boot up incorrectly. If POR timing and voltage requirements cannot be met, it is highly recommended that SDN be controlled using the host processor rather than tying it to GND on the board.

3.3.3. Standby State

Standby state has the lowest current consumption with the exception of shutdown but has much faster response time to TX mode. In most cases standby should be used as the low power state. In this state the register values are maintained with all other blocks disabled. The SPI is accessible during this mode but any SPI event, including FIFO R/W, will enable an internal boot oscillator and automatically move the part to SPI active state. After an SPI event the host will need to re-command the device back to standby through the “Change State” API command to achieve the 40 nA current consumption. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.4. Sleep State

Sleep state is the same as standby state but the wake-up-timer and a 32 kHz clock source are enabled. The source of the 32 kHz clock can either be an internal 32 kHz RC oscillator which is periodically calibrated or a 32 kHz oscillator using an external XTAL.The SPI is accessible during this mode but an SPI event will enable an internal boot oscillator and automatically move the part to SPI active mode. After an SPI event the host will need to re-command the device back to sleep. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption of this mode.

3.3.5. SPI Active State

In SPI active state the SPI and a boot up oscillator are enabled. After SPI transactions during either standby or sleep the device will not automatically return to these states. A “Change State” API command will be required to return to either the standby or sleep modes.

3.3.6. Ready State

Ready state is designed to give a fast transition time to TX state with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX mode by eliminating the crystal start-up time.

3.3.7. TX State

The TX state may be entered from any of the state with the “Start TX” or “Change State” API commands. A built-in sequencer takes care of all the actions required to transition between states from enabling the crystal oscillator to ramping up the PA. The following sequence of events will occur automatically when going from standby to TX state.

1. Enable internal LDOs.
2. Start up crystal oscillator and wait until ready (controlled by an internal timer).
3. Enable PLL.
4. Calibrate VCO/PLL.
5. Wait until PLL settles to required transmit frequency (controlled by an internal timer).
6. Activate power amplifier and wait until power ramping is completed (controlled by an internal timer).
7. Transmit packet.

Steps in this sequence may be eliminated depending on which state the chip is configured to prior to commanding to TX. By default, the VCO and PLL are calibrated every time the PLL is enabled. When the START_TX API command is utilized the next state may be defined to ensure optimal timing and turnaround.

Figure 7 shows an example of the commands and timing for the START_TX command. CTS will go high as soon as the sequencer puts the part into TX state. As the sequencer is stepping through the events listed above, CTS will be low and no new commands or property changes are allowed. If the Fast Response (FRR) or nIRQ is used to monitor the current state there will be slight delay caused by the internal hardware from when the event actually occurs to when the transition occurs on the FRR or nIRQ. The time from entering TX state to when the FRR will update is 5 µs and the time to when the nIRQ will transition is 13 µs. If a GPIO is programmed for TX state or used as control for a transmit/receive switch (TR switch) there is no delay.

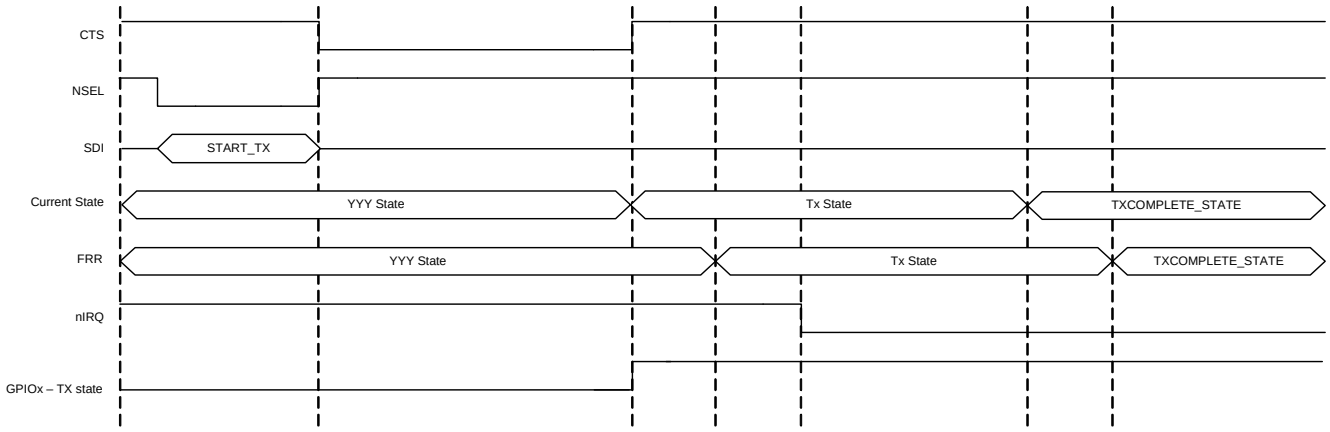


Figure 7. Start_TX Commands and Timing

3.4. Application Programming Interface (API)

An application programming interface (API), which the host MCU will communicate with, is embedded inside the device. The API is divided into two sections, commands and properties. The commands are used to control the chip and retrieve its status. The properties are general configurations which will change infrequently. The API descriptions can be found on the Silicon Labs website.

3.5. Interrupts

The Si406x is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Registers. The nIRQ output signal will then be reset until the next change in status is detected.

The interrupts sources are grouped into three groups: packet handler, chip status, and modem. The individual interrupts in these groups can be enabled/disabled in the interrupt property registers. An interrupt must be enabled for it to trigger an event on the nIRQ pin. The interrupt group must be enabled as well as the individual interrupts in API property as described in the API documentation.

Once an interrupt event occurs and the nIRQ pin is low there are two ways to read and clear the interrupts. All of the interrupts may be read and cleared in the “GET_INT_STATUS” API command. By default all interrupts will be cleared once read. If only specific interrupts want to be read in the fastest possible method the individual interrupt groups (Packet Handler, Chip Status, Modem) may be read and cleared by the “GET_MODEM_STATUS”, “GET_PH_STATUS” (packet handler), and “GET_CHIP_STATUS” API commands.

The instantaneous status of a specific function maybe read if the specific interrupt is enabled or disabled. The status results are provided after the interrupts and can be read with the same commands as the interrupts. The status bits will give the current state of the function whether the interrupt is enabled or not.

The fast response registers can also give information about the interrupt groups but reading the fast response registers will not clear the interrupt and reset the nIRQ pin.

3.6. GPIO

Four general purpose IO pins are available to utilize in the application. The GPIO are configured by the GPIO_PIN_CFG command in address 13h. For a complete list of the GPIO options please see the API guide. GPIO pins 0 and 1 should be used for active signals such as data or clock. GPIO pins 2 and 3 have more susceptibility to generating spurious in the synthesizer than pins 0 and 1. The drive strength of the GPIOs can be adjusted with the GEN_CONFIG parameter in the GPIO_PIN_CFG command. By default the drive strength is set to minimum. The default configuration for the GPIOs and the state during SDN is shown below in Table 11.The state of the IO during shutdown is also shown inTable 11. As indicated previously in Table 5, GPIO 0 has lower drive strength than the other GPIOs.

Table 11. GPIOs

Pin	SDN State	POR Default
GPIO0	0	POR
GPIO1	0	CTS
GPIO2	0	POR
GPIO3	0	POR
nIRQ	resistive VDD pull-up	nIRQ
SDO	resistive VDD pull-up	SDO
SDI	High Z	SDI
SCLK	High Z	SCLK
NSEL	High Z	NSEL

4. Modulation and Hardware Configuration Options

The Si406x supports different modulation options and can be used in various configurations to tailor the device to any specific application or legacy system for drop in replacement. The modulation and configuration options are set in API property, MODEM_MOD_TYPE.

4.1. Modulation Types

The Si406x supports five different modulation options: Gaussian frequency shift keying (GFSK), frequency-shift keying (FSK), four-level GFSK (4GFSK), four-level FSK (4FSK), on-off keying (OOK). Minimum shift keying (MSK) can also be created by using GFSK settings. GFSK is the recommended modulation type as it provides the best performance and cleanest modulation spectrum. The modulation type is set by the “MOD_TYPE[2:0]” registers in the “MODEM_MOD_TYPE” API property. A continuous-wave (CW) carrier may also be selected for RF evaluation purposes. The modulation source may also be selected to be a pseudo-random source for evaluation purposes.

4.2. Hardware Configuration Options

There are different receive demodulator options to optimize the performance and mutually-exclusive options for how the TX data is transferred from the host MCU to the RF device.

4.2.1. TX Data Interface With MCU

There are two different options for transferring the data from the RF device to the host MCU. FIFO mode uses the SPI interface to transfer the data, while direct mode transfers the data in real time over a GPIO pin.

4.2.1.1. FIFO Mode

In FIFO mode, the transmit data is stored in integrated FIFO register memory. The TX FIFO is accessed by writing Command 66h followed directly by the data that the host wants to write into the TX FIFO.

If the packet handler is enabled, the data bytes stored in FIFO memory are “packaged” together with other fields and bytes of information to construct the final transmit packet structure. These other potential fields include the Preamble, Sync word, Header, and CRC checksum. In TX mode, the packet structure may be highly customized by enabling or disabling individual fields; for example, it is possible to disable both the Preamble and Sync Word fields and to load the entire packet structure into FIFO memory. For further information on the configuration of the FIFOs for a specific application or packet size, see "6. Data Handling and Packet Handler" on page 26. The chip will return to the IDLE state programmed in the argument of the “START TX” API command, TXCOMPLETE_STATE[3:0]. For example, the chip may be placed into TX mode by sending the “START TX” command and by writing the 30h to the TXCOMPLETE_STATE[3:0] argument. The chip will transmit all of the contents of the FIFO, and a PACKET_SENT interrupt will occur. When this event occurs, the chip will return to the ready state as defined by TXCOMPLETE_STATE[3:0] = 30h.

4.2.1.2. Automatic TX Packet Repeat

In TX mode, there is an option to send the FIFO contents repeatedly with a user-defined number of times to repeat. This is limited to the FIFO size, and the entire contents of the packet including preamble and sync word need to be loaded into the TX FIFO. This is selectable via the START_TX API, and packets will be sent without any gaps between them.

4.2.1.3. Direct Mode

For legacy systems that perform packet handling within the host MCU or other baseband chip, it may not be desirable to use the FIFO. For this scenario, a Direct mode is provided, which bypasses the FIFOs entirely. In TX Direct mode, the TX modulation data is applied to an input pin of the chip and processed in “real time” (i.e., not stored in a register for transmission at a later time). Any of the GPIOs may be configured for use as the TX Data input function. Furthermore, an additional pin may be required for a TX Clock output function if GFSK modulation is desired (only the TX Data input pin is required for FSK). To achieve direct mode, the GPIO must be configured in the “GPIO_PIN_CFG” API command as well as the “MODEM_MOD_TYPE” API property. For GFSK, “TX_DIRECT_MODE_TYPE” must be set to Synchronous. For 2FSK or OOK, the type can be set to asynchronous or synchronous. The MOD_SOURCE[1:0] should be set to 01h for are all direct mode configurations.

5. Internal Functional Blocks

The following sections provide an overview to the key internal blocks and features.

5.1. Synthesizer

An integrated Sigma Delta (ΣΔ) Fractional-N PLL synthesizer capable of operating over the bands from 142–175, 283–350, 350–525, and 850–1050 MHz for the Si406x. Using a ΣΔ synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing. The transmit modulation is applied directly to the loop in the digital domain through the fractional divider, which results in very precise accuracy and control over the transmit deviation. The frequency resolution in the 850–1050 MHz band is 28.6 Hz with more resolution in the other bands. The nominal reference frequency to the PLL is 30 MHz, but any XTAL frequency from 25 to 32 MHz may be used. The modem configuration calculator in WDS will automatically account for the XTAL frequency being used. The PLL utilizes a differential LC VCO with integrated on-chip inductors. The output of the VCO is followed by a configurable divider, which will divide the signal down to the desired output frequency band.

5.1.1. Synthesizer Frequency Control

The frequency is set by changing the integer and fractional settings to the synthesizer. The WDS calculator will automatically provide these settings, but the synthesizer equation is shown below for convenience. The APIs for setting the frequency are FREQ_CONTROL_INTE, FREQ_CONTROL_FRAC2, FREQ_CONTROL_FRAC1, and FREQ_CONTROL_FRAC0.

$$\text{RF\_channel} = \left(\text{fc\_inte} + \frac{\text{fc\_frac}}{2^{19}}\right) \times \frac{2 \times \text{freq\_xo}}{\text{outdiv}} (\text{Hz})$$

Note: The fc_frac/2^{19} value in the above formula has to be a number between 1 and 2.

Table 12. Output Divider (Outdiv) Values for the Si406x

Outdiv	Lower (MHz)	Upper (MHz)
24	142	175
12	284	350
10	350	420
8	420	525
4	850	1050

5.1.1.1. EZ Frequency Programming

In applications that utilize multiple frequencies or channels, it may not be desirable to write four API registers each time a frequency change is required. EZ frequency programming is provided so that only a single register write (channel number) is required to change frequency. A base frequency is first set by first programming the integer and fractional components of the synthesizer. This base frequency will correspond to channel 0. Next, a channel step size is programmed into the FREQ_CONTROL_CHANNEL_STEP_SIZE_1 and FREQ_CONTROL_CHANNEL_STEP_SIZE_0 API registers. The resulting frequency will be:

$$\text{RF Frequency} = \text{Base Frequency} + \text{Channel} \times \text{Stepsize}$$

The second argument of the START_TX is CHANNEL, which sets the channel number for EZ frequency programming. For example, if the channel step size is set to 1 MHz, the base frequency is set to 900 MHz with the INTE and FRAC API registers, and a CHANNEL number of 5 is programmed during the START_TX command, the resulting frequency will be 905 MHz. If no CHANNEL argument is written as part of the START_TX command, it will default to the previous value. The initial value of CHANNEL is 0; so, if no CHANNEL value is written, it will result in the programmed base frequency.

5.2. Transmitter (TX)

The Si4063 contains an integrated +20 dBm transmitter or power amplifier that is capable of transmitting from –20 to +20 dBm. The output power steps are less than 0.25 dB within 6 dB of max power but become larger and more non-linear close to minimum output power. The Si4063 PA is designed to provide the highest efficiency and lowest current consumption possible. The Si4060 is designed to supply +10 dBm output power for less than 20 mA for applications that require operation from a single coin cell battery. The Si4060 can also operate with either class-E or switched current matching and output up to +13 dBm TX power. All PA options are single-ended to allow for easy antenna matching and low BOM cost. Automatic ramp-up and ramp-down is automatically performed to reduce unwanted spectral spreading.

Chip's TXRAMP pin is disabled by default to save current in cases where on-chip PA will be able to drive the antenna. In cases where on-chip PA will drive the external PA, and the external PA needs a ramping signal, TXRAMP is the signal to use. To enable TXRAMP, set the API Property PA_MODE[7] = 1. TXRAMP will start to ramp up, and ramp down at the SAME time as the internal on-chip PA ramps up/down.

The ramping speed is programmed by TC[3:0] in the PA_RAMP_EX API property, which has the characteristics listed in Table 13.

Table 13. Ramp Times as a Function of TC[3:0] Value

TC	Ramp Time (µs)
0	1.25
1	1.33
2	1.43
3	1.54
4	1.67
5	1.82
6	2.00
7	2.22
8	2.50
9	2.86
10	3.33
11	4.00
12	5.00
13	6.67
14	10.00
15	20.00

The ramping profile is close to a linear ramping profile with smoothed out corner when approaching Vhi and Vlo. The TXRAMP pin can source up to 1 mA without voltage drooping. The TXRAMP pin's sinking capability is equivalent to a 10 kΩ pull-down resistor.

Vhi = 3 V when Vdd > 3.3 V. When Vdd < 3.3 V, the Vhi will be closely following the Vdd, and ramping time will be smaller also.

Vlo = 0 V when NO current needed to be sunk into TXRAMP pin. If 10 µA need to be sunk into the chip, Vlo will be 10 µA x 10k = 100 mV.

Number	Command	Summary
0x2200	PA_MODE	Sets PA type.
0x2201	PA_PWR_LVL	Adjust TX power in fine steps.
0x2202	PA_BIAS_CLKDUTY	Adjust TX power in coarse steps and optimizes for different match configurations.
0x2203	PA_TC	Changes the ramp up/down time of the PA.

5.2.1. Si4063: +20 dBm PA

The +20 dBm configuration utilizes a class-E matching configuration. Typical performance for the 900 MHz band for output power steps, voltage, and temperature are shown in Figures 8–10. The output power is changed in 128 steps through PA_PWR_LVL API. For detailed matching values, BOM, and performance at other frequencies, refer to the PA Matching application note.

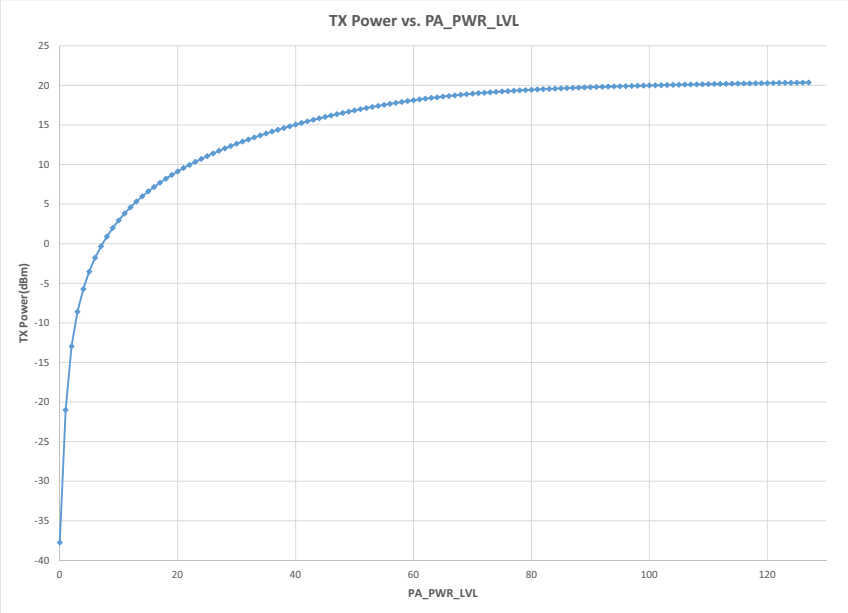


Figure 8. +20 dBm TX Power vs. PA_PWR_LVL

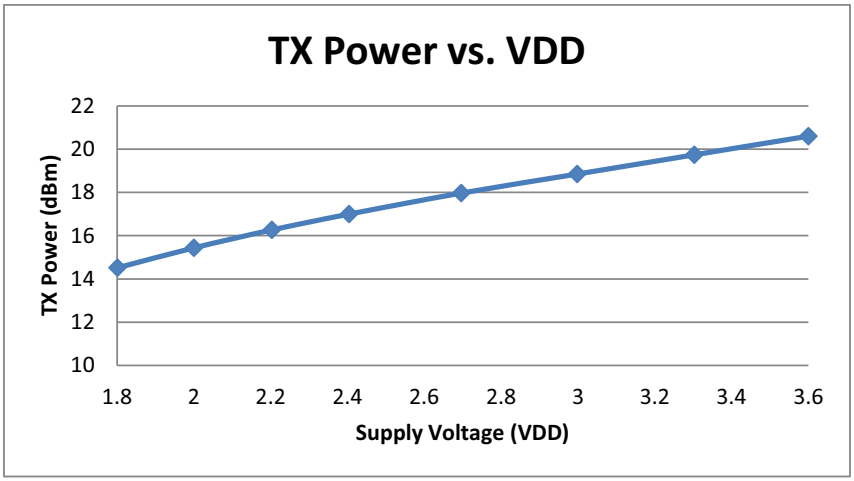


Figure 9. +20 dBm TX Power vs. VDD

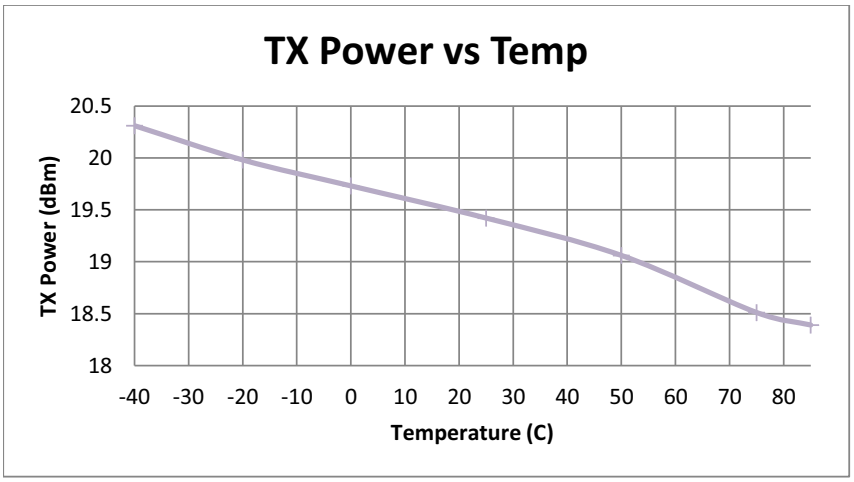


Figure 10. +20 dBm TX Power vs. Temp

5.3. Crystal Oscillator

The Si406x includes an integrated crystal oscillator with a fast start-up time of less than 250 µs. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the crystal. The default crystal is 30 MHz, but the circuit is designed to handle any XTAL from 25 to 32 MHz. If a crystal different than 30 MHz is used, the POWER_UP API boot command must be modified. The WDS calculator crystal frequency field must also be changed to reflect the frequency being used. The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the GLOBAL_XO_TUNE API property. The total internal capacitance is 11 pF and is adjustable in 127 steps (70 fF/step). The crystal frequency adjustment can be used to compensate for crystal production tolerances. The frequency offset characteristics of the capacitor bank are demonstrated in Figure 11.

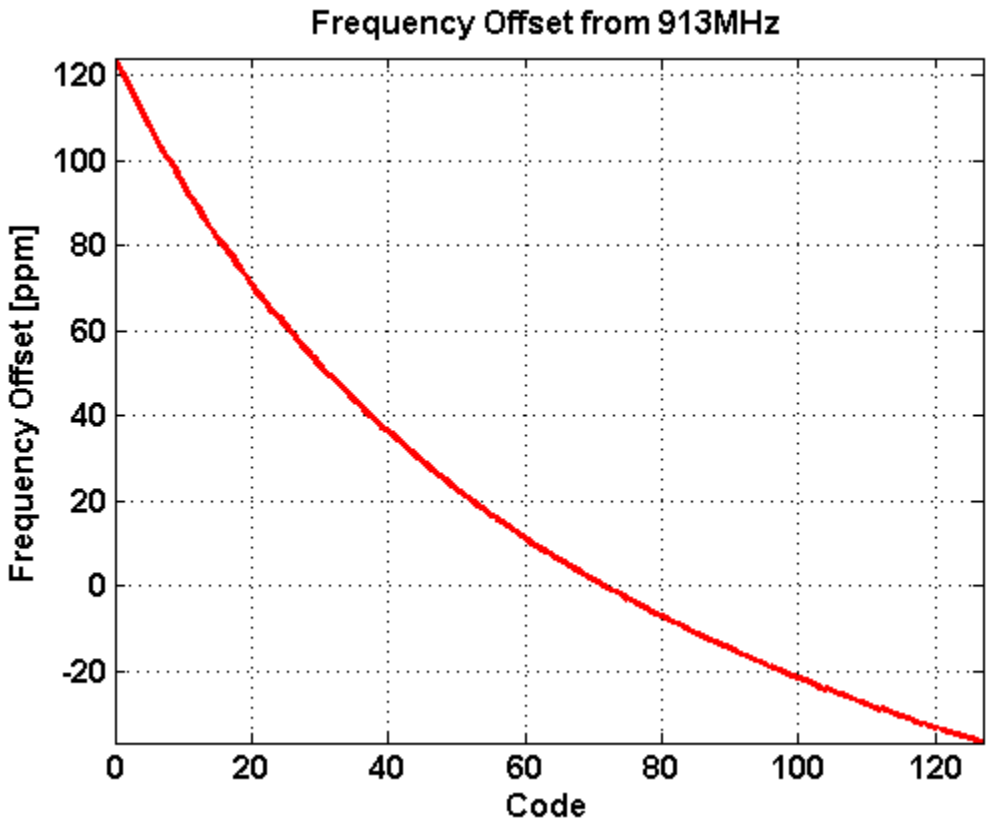


Figure 11. Capacitor Bank Frequency Offset Characteristics

Utilizing the on-chip temperature sensor and suitable control software, the temperature dependency of the crystal can be canceled.

A TCXO or external signal source can easily be used in place of a conventional XTAL and should be connected to the XIN pin. The incoming clock signal is recommended to be peak-to-peak swing in the range of 600 mV to 1.4 V and ac-coupled to the XIN pin. If the peak-to-peak swing of the TCXO exceeds 1.4 V peak-to-peak, then dc coupling to the XIN pin should be used. The maximum allowed swing on XIN is 1.8 V peak-to-peak.

The XO capacitor bank should be set to 0 whenever an external drive is used on the XIN pin. In addition, the POWER_UP command should be invoked with the TCXO option whenever external drive is used.

6. Data Handling and Packet Handler

6.1. TX FIFOs

By default, a 64 byte FIFO is available in the device. This can be increased to support a 129 byte FIFO via API configuration. Writing to command Register 66h loads data into the TX FIFO. The TX FIFO has a threshold for when the FIFO is almost empty, which is set by the “TX_FIFO_EMPTY” property. An interrupt event occurs when the data in the TX FIFO reaches the almost empty threshold. If more data is not loaded into the FIFO, the chip automatically exits the TX state after the PACKET_SENT interrupt occurs. The TX FIFO may be cleared or reset with the “FIFO_RESET” command.

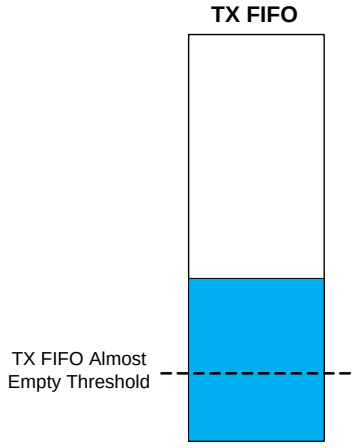


Figure 12. TX FIFO

6.2. Packet Handler

When using the FIFOs, automatic packet handling may be enabled. The usual fields for network communication, such as preamble, synchronization word, headers, packet length, and CRC, can be configured to be automatically added to the data payload. The fields needed for packet generation normally change infrequently and can therefore be stored in registers. Automatically adding these fields to the data payload in TX mode greatly reduces the amount of communication between the microcontroller and Si406x. It also greatly reduces the required computational power of the microcontroller. The general packet structure is shown in Figure 13. Any or all of the fields can be enabled and checked by the internal packet handler.

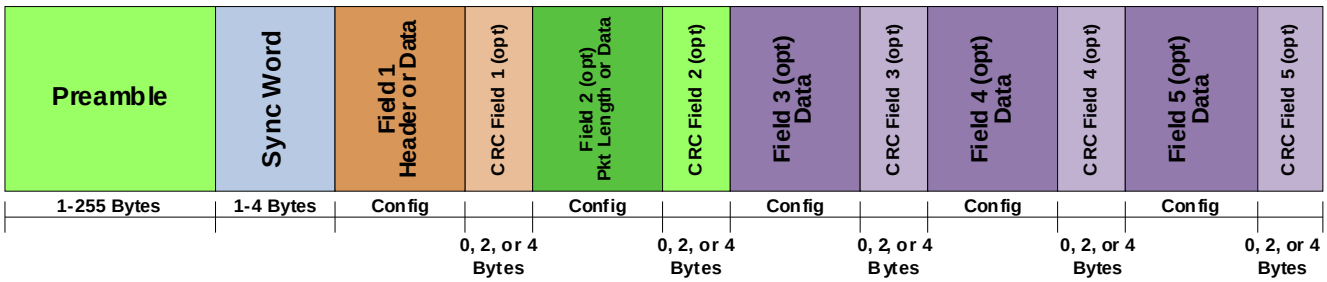


Figure 13. Packet Handler Structure

The fields are highly programmable and can be used to check any kind of pattern in a packet structure. The general functions of the packet handler include the following:

- Construction of Preamble field in TX mode
- Construction of Sync field in TX mode
- Construction of Data Field from FIFO memory in TX mode
- Construction of CRC field (if enabled) in TX mode
- Data whitening and/or Manchester encoding (if enabled) in TX mode

7. Auxiliary Blocks

7.1. Wake-up Timer and 32 kHz Clock Source

The chip contains an integrated wake-up timer that can be used to periodically wake the chip from sleep mode. The wake-up timer runs from either the internal 32 kHz RC Oscillator, or from an external 32 kHz XTAL.

The wake-up timer can be configured to run when in sleep mode. If WUT_EN = 1 in the GLOBAL_WUT_CONFIG property, prior to entering sleep mode, the wake-up timer will count for a time specified defined by the GLOBAL_WUT_R and GLOBAL_WUT_M properties. At the expiration of this period, an interrupt will be generated on the nIRQ pin if this interrupt is enabled in the INT_CTL_CHIP_ENABLE property. The microcontroller will then need to verify the interrupt by reading the chip interrupt status either via GET_INT_STATUS or a fast response register. The formula for calculating the Wake-Up Period is as follows:

$$WUT = WUT\_M \times \frac{4 \times 2^{WUT\_R}}{32.768}[ms]$$

The RC oscillator frequency will change with temperature; so, a periodic recalibration is required. The RC oscillator is automatically calibrated during the POWER_UP command and exits from the Shutdown state. To enable the recalibration feature, CAL_EN must be set in the GLOBAL_WUT_CONFIG property, and the desired calibration period should be selected via WUT_CAL_PERIOD[2:0] in the same API property. During the calibration, the 32 kHz RC oscillator frequency is compared to the 30 MHz XTAL and then adjusted accordingly. The calibration needs to start the 30 MHz XTAL, which increases the average current consumption; so, a longer CAL_PERIOD results in a lower average current consumption. The 32 kHz XTAL accuracy is comprised of both the XTAL parameters and the internal circuit. The XTAL accuracy can be defined as the XTAL initial error + XTAL aging + XTAL temperature drift + detuning from the internal oscillator circuit. The error caused by the internal circuit is typically less than 10 ppm.

7.2. Low Duty Cycle Mode

The low duty cycle (LDC) mode is implemented to automatically wake-up the transmitter to send a packet. It allows low average current polling operation by the Si406x for which the wake-up timer (WUT) is used. TX LDC operation must be set via the GLOBAL_WUT_CONFIG property when setting up the WUT. The LDC wake-up period is determined by the following formula:

$$LDC = WUT\_LDC \times \frac{4 \times 2^{WUT\_R}}{32.768}[ms]$$

where the WUT_LDC parameter can be set by the GLOBAL_WUT_LDC property. The WUT period must be set in conjunction with the LDC mode duration; for the relevant API properties, see the wake-up timer (WUT) section.

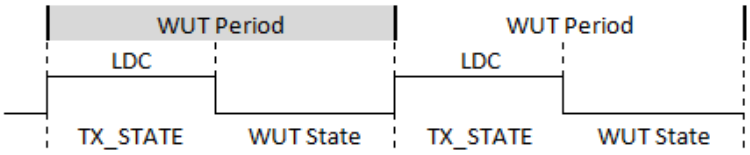


Figure 14. TX LDC Sequences

In TX LDC mode, the transmitter periodically wakes itself up to transmit a packet that is in the data buffer. If a packet has been transmitted, nIRQ goes low if the option is set in the INT_CTL_ENABLE property. After transmitting, the transmitter immediately returns to the WUT state and stays there until the next wake-up time expires.

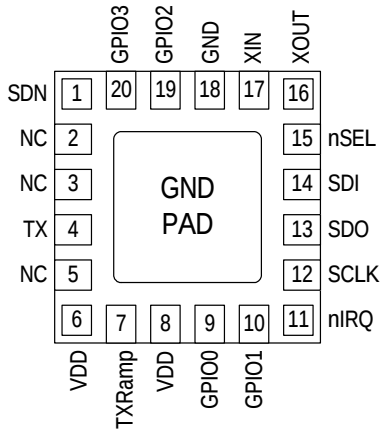
7.3. Temperature, Battery Voltage, and Auxiliary ADC

The Si406x family contains an integrated auxiliary ADC for measuring internal battery voltage, an internal temperature sensor, or an external component over a GPIO. The ADC utilizes a SAR architecture and achieves 11-bit resolution. The Effective Number of Bits (ENOB) is 9 bits. When measuring external components, the input voltage range is 1 V, and the conversion rate is between 300 Hz to 2.44 kHz. The ADC value is read by first sending the GET_ADC_READING command and enabling the inputs that are desired to be read: GPIO, battery, or temp. The temperature sensor accuracy at 25 °C is typically ±2 °C.

7.4. Low Battery Detector

The low battery detector (LBD) is enabled and utilized as part of the wake-up-timer (WUT). The LBD function is not available unless the WUT is enabled, but the host MCU can manually check the battery voltage anytime with the auxiliary ADC. The LBD function is enabled in the GLOBAL_WUT_CONFIG API property. The battery voltage will be compared against the threshold each time the WUT expires. The threshold for the LBD function is set in GLOBAL_LOW_BATT_THRESH. The threshold steps are in increments of 50 mV, ranging from a minimum of 1.5 V up to 3.05 V. The accuracy of the LBD is ±3%. The LBD notification can be configured as an interrupt on the nIRQ pin or enabled as a direct function on one of the GPIOs.

8. Pin Descriptions: Si4063/60



Pin	Pin Name	I/0	Description
1	SDN	I	**Shutdown Input Pin**. 0–VDD V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN = 1, the chip will be completely shut down, and the contents of the registers will be lost. Can be used to reset the chip
2	NC		Leave pin floating.
3	NC		Leave pin floating.
4	TX	O	**Transmit Output Pin.** The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
5	NC		It is recommended to connect this pin to GND per the reference design schematic. Not connected internally to any circuitry.
6	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
7	TXRAMP	O	**Programmable Bias Output with Ramp Capability for External FET PA.** See "5.2. Transmitter (TX)" on page 22.
8	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
9	GPIO0	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, etc.
10	GPIO1	I/O	
11	nIRQ	O	**General Microcontroller Interrupt Status Output.** When the Si406x exhibits any one of the interrupt events, the nIRQ pin will be set low = 0. The Microcontroller can then determine the state of the interrupt by reading the interrupt status. No external resistor pull-up is required, but it may be desirable if multiple interrupt lines are connected.

Pin	Pin Name	I/0	Description
12	SCLK	I	**Serial Clock Input.** 0–VDD V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si406x on positive edge transitions.
13	SDO	O	**0–VDD V Digital Output.** Provides a serial readback function of the internal control registers.
14	SDI	I	**Serial Data Input.** 0–VDD V digital input. This pin provides the serial data stream for the 4-line serial data bus.
15	nSEL	I	**Serial Interface Select Input.** 0–VDD V digital input. This pin provides the Select/Enable function for the 4-line serial data bus.
16	XOUT	O	**Crystal Oscillator Output.** Connect to an external 25 to 32 MHz crystal, or leave floating when driving with an external source on XIN.
17	XIN	I	**Crystal Oscillator Input.** Connect to an external 25 to 32 MHz crystal, or connect to an external source.
18	GND	GND	When using an XTAL, leave floating per the reference design schematic. When using a TCXO, connect to TCXO GND, which should be separate from the board's reference ground plane.
19	GPIO2	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions, including Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect.
20	GPIO3	I/O	
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the Si406x supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the Si406x.

9. Ordering Information

Part Number*	Description	Package Type	Operating Temperature
Si4063-C2A-GM	ISM EZRadioPRO Transmitter	QFN-20 Pb-free	–40 to 85 °C
Si4060-C2A-GM	ISM EZRadioPRO Transmitter	QFN-20 Pb-free	–40 to 85 °C

***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option.

10. Package Outline: Si4063/60

Figure 15 illustrates the package details for the Si406x. Table 14 lists the values for the dimensions shown in the illustration.

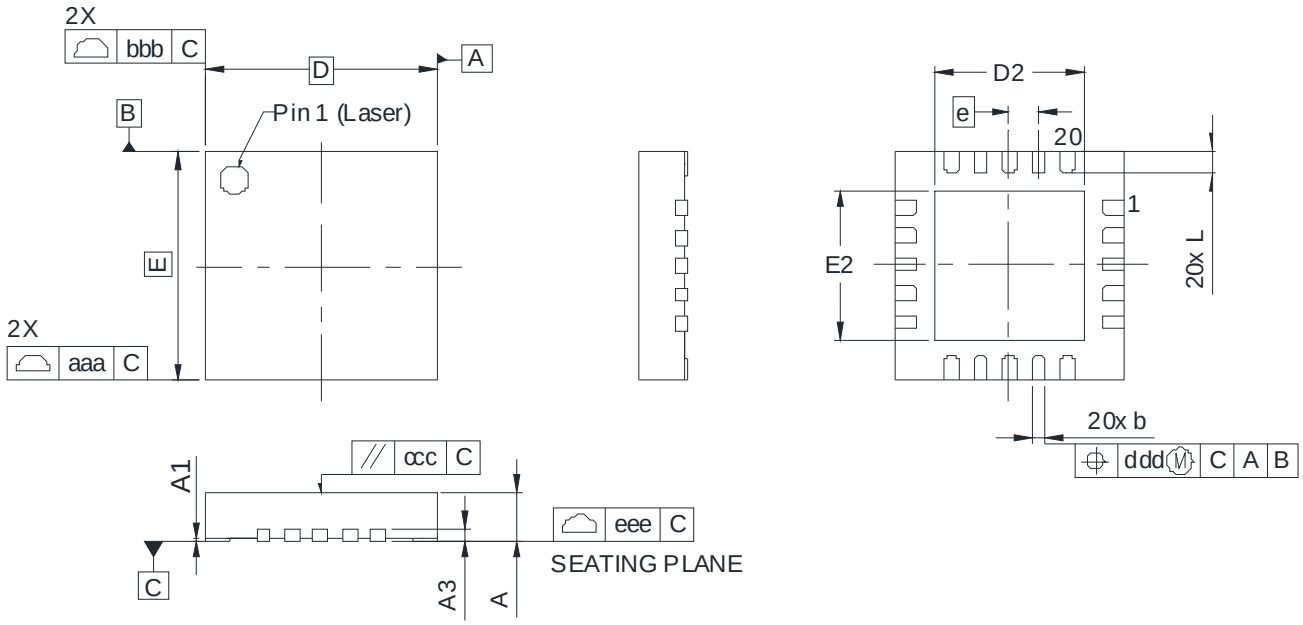


Figure 15. 20-Pin Quad Flat No-Lead (QFN)

Table 14. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D		4.00 BSC	
D2	2.45	2.60	2.75
e		0.50 BSC	
E		4.00 BSC	
E2	2.45	2.60	2.75
L	0.30	0.40	0.50
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.08	

Notes:

1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. PCB Land Pattern: Si4063/60

Figure 16 illustrates the PCB land pattern details for the Si406x. Table 15 lists the values for the dimensions shown in the illustration.

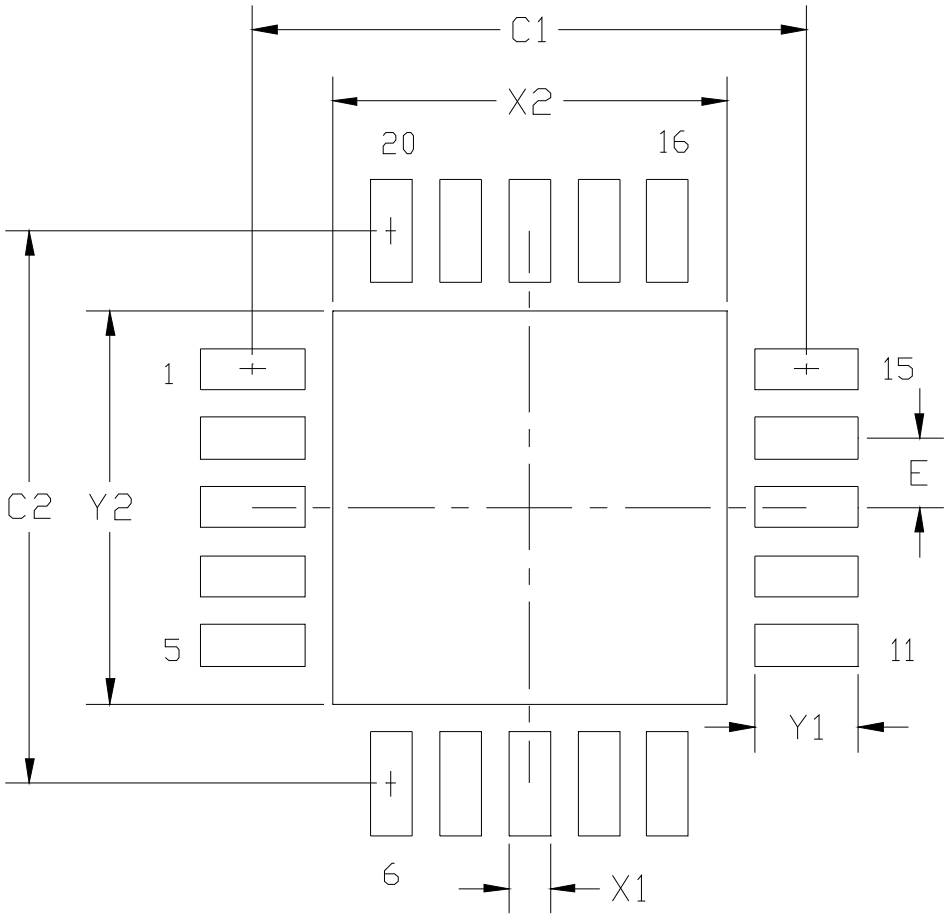


Figure 16. PCB Land Pattern

Table 15. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	Max
C1	3.90	4.00
C2	3.90	4.00
E	0.50 REF	
X1	0.20	0.30
X2	2.55	2.65
Y1	0.65	0.75
Y2	2.55	2.65

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

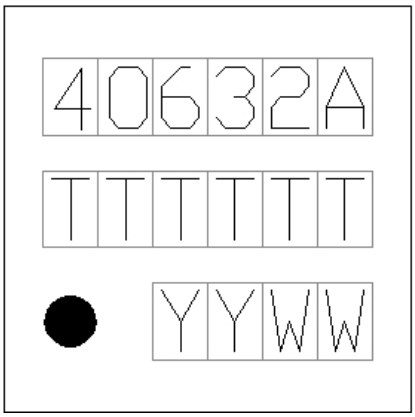
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

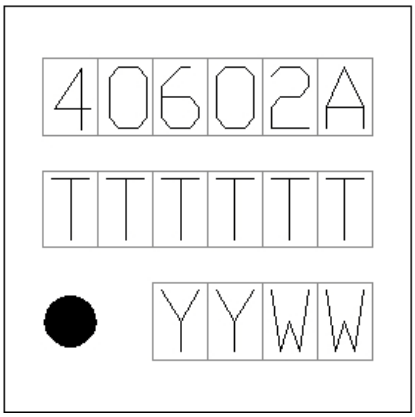
Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

12. Top Marking

12.1. Si4063/60 Top Marking





12.2. Top Marking Explanation

Mark Method	YAG Laser	
Line 1 Marking	Part Number	40632A = Si4063 Rev 2A[1] 40602A = Si4060 Rev 2A[1]
Line 2 Marking	TTTTT = Internal Code	Internal tracking code.[2]
Line 3 Marking	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

Notes:

1. The first letter after the part number is part of the ROM revision. The last letter indicates the firmware revision.
2. The first letter of this line is part of the ROM revision.

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