Si1133 Data Sheet

UV Index/Ambient Light Sensor IC with I²C Interface

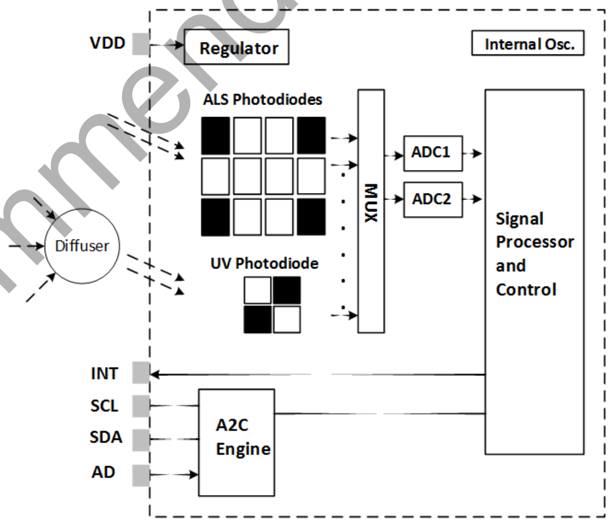
The Si1133 is a UV Index Sensor and Ambient Light Sensor with I²C digital interface and programmable-event interrupt output. This sensor IC includes dual 23-bit analog-to-digital converters, integrated high-sensitivity array of UV, visible and infrared photodiodes, and digital signal processor. The Si1133 is provided in a 10-lead 2x2 mm DFN package and capable of operation from 1.62 to 3.6 V over the –40 to +85 °C temperature range.

Applications

- Wearables
- Handsets
- Display backlighting control
- Consumer electronics

KEY FEATURES

- High accuracy UV index sensor (0 to > 20 uV)
  - Matches erythermal curve
- Ambient light sensor
  - <100 mlx resolution possible, allowing operation under dark glass
  - Up to 128 klx dynamic range possible across two ADC range settings
- Industry's lowest power consumption
  - 1.62 to 3.6 V supply voltage
  - <500 nA standby current
  - Internal and external wake support
  - Built-in voltage supply monitor and power-on reset controller



1. Feature List

- High accuracy UV index sensor
    - Matches erythermal curve
- Ambient light sensor
    - <100 mlx resolution possible, allowing operation under dark glass<100 mlx resolution possible, allowing operation under dark glass
    - Up to 128 klx dynamic range possible across two ADC range settings
- Industry's lowest power consumption
    - 1.62 to 3.6 V supply voltage
    - <500 nA standby current
    - Internal and external wake support
    - Built-in voltage supply monitor and power-on reset controller
- Trimmable internal oscillator with typical 1% accuracy
- I2C Serial communications
    - Up to 3.4 Mbps data rate
    - Slave mode hardware address decoding
- Small package options
    - 10-lead 2 x 2 x 0.65 mm QFN
- Temperature Range: –40 to +85 °C

2. 2 x 2 mm DFN Ordering Guide

Family	DFN OPNs	ALS	UV Index	Proximity (# of LED Drivers)	HRM
Si113x	Si1133-AA00-GMR	Y	Y	—	—

3. Functional Description

The Si1133 is a UV and Ambient Light sensor whose operational state is controlled through registers accessible through the I^2C interface. The host can command the Si1133 to initiate on-demand UV or Ambient Light measurement. The host can also place the Si1133 in an autonomous operational state where it performs measurements at set intervals and interrupts the host either after each measurement is completed or whenever a set threshold has been crossed. This results in an overall system power saving allowing the host controller to operate longer in its sleep state instead of polling the Si1133.

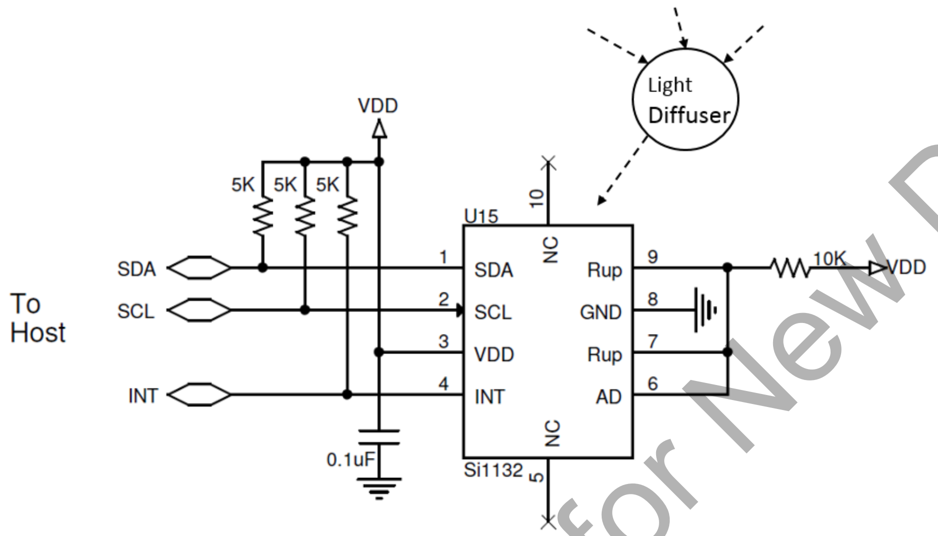


Figure 3.1. Si1133 Basic Application

3.1 Ambient Light Sensing

The Si1133 has photodiodes capable of measuring visible and infrared light. However, the visible photodiode is also influenced by infrared light. The measurement of illuminance requires the same spectral response as the human eye. If an accurate lux measurement is desired, the extra IR response of the visible-light photodiode must be compensated. Therefore, to allow the host to make corrections to the infrared light's influence, the Si1133 reports the infrared light measurement on a separate channel. The separate visible and IR photodiodes lend themselves to a variety of algorithmic solutions. The host can then take these two measurements and run an algorithm to derive an equivalent lux level as perceived by a human eye. Having the IR correction algorithm running in the host allows for the most flexibility in adjusting for system-dependent variables. For example, if the glass used in the system blocks visible light more than infrared light, the IR correction needs to be adjusted.

If the host is not making any infrared corrections, the infrared measurement can be turned off in the CHAN_LIST parameter.

By default, the measurement parameters are optimized for indoor ambient light levels, where it is possible to detect low light levels. For operation under direct sunlight, the ADC can be programmed to operate in a high signal operation so that it is possible to measure direct sunlight without overflowing.

For low-light applications, it is possible to increase the ADC integration time. Normally, the integration time is 24.4 µs. By increasing this integration time, the ADC can detect light levels as low as 100 mlx. The ADC integration time for the Visible Light Ambient measurement can be programmed independently of the ADC integration time of the Infrared Light Ambient measurement. The independent ADC parameters allow operation under glass covers having a higher transmittance to Infrared Light than Visible Light.

When operating in the lower signal range, or when the integration time is increased, it is possible to saturate the ADC when the ambient light suddenly increases. Any overflow condition will have the corresponding data registers report a value of 0xFFddFF for 16-bit mode and 0x7FFFFF for 24-bit mode. The host can adjust the ADC sensitivity to avoid an overflow condition. If the light levels return to a range within the capabilities of the ADC, the corresponding data registers begin to operate normally.

The Si1133 can initiate ALS measurements either when explicitly commanded by the host or periodically through an autonomous process. Refer to Section 4. Operational Modes for additional details.

Two ADCs can be used for simultaneous readings of the visible or UV photodiode and black dark current reference photodiode. When subtracted, these differential measurements remove dark current, reducing noise that enables lower light sensitivity.

3.2 Ultraviolet (UV) Index Sensing

The UV Index is a number linearly related to the intensity of sunlight reaching the earth and is weighted according to the CIE erythema Action Spectrum as shown in Figure 4. This weighting is a standardized measure of human skin's response to different wavelengths of sunlight from UVB to UVA. The UV Index has been standardized by the World Health Organization as shown in the figure below.

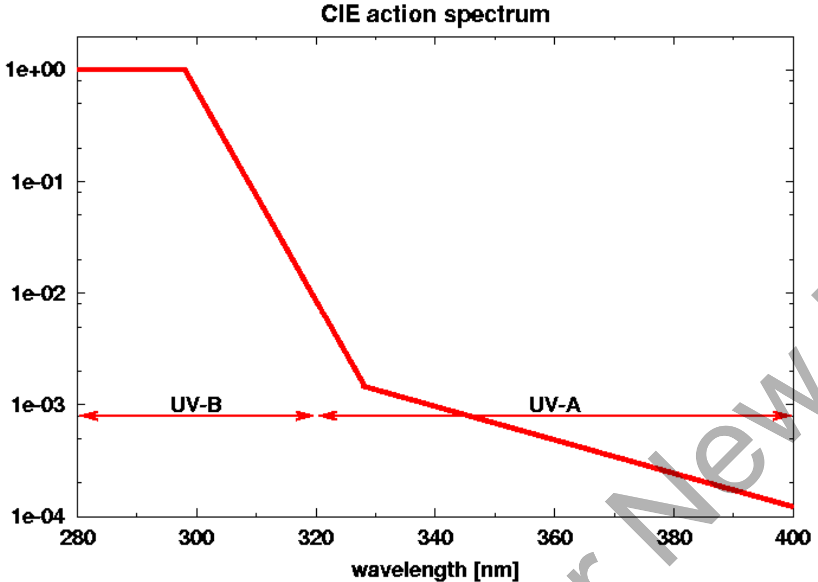


Figure 3.2. CIE Erythemal Action Spectrum

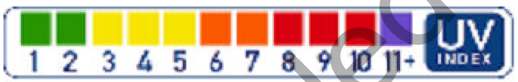


Figure 3.3. UV Index Scale

Isolated UV photodiodes that closely match the erythema curve for accurate UV Index measurements. Matching dark current reference photodiodes are also provided to cancel UV photodiode noise. The typical calibrated UV Index sensor response vs. calculated ideal UV Index is shown below for several cloudy and sunny days and at various angles of the sun/time of day.

Given the possible variation of the overlay materials above the Si1133, it is generally recommended that outgoing factory calibration be performed at the outgoing test to decrease system-to-system variation.

The performance of the Si1133 is best when under a Teflon diffuser while diffuser is within +/- 30 degrees of the sensor view angle. See the plot below.

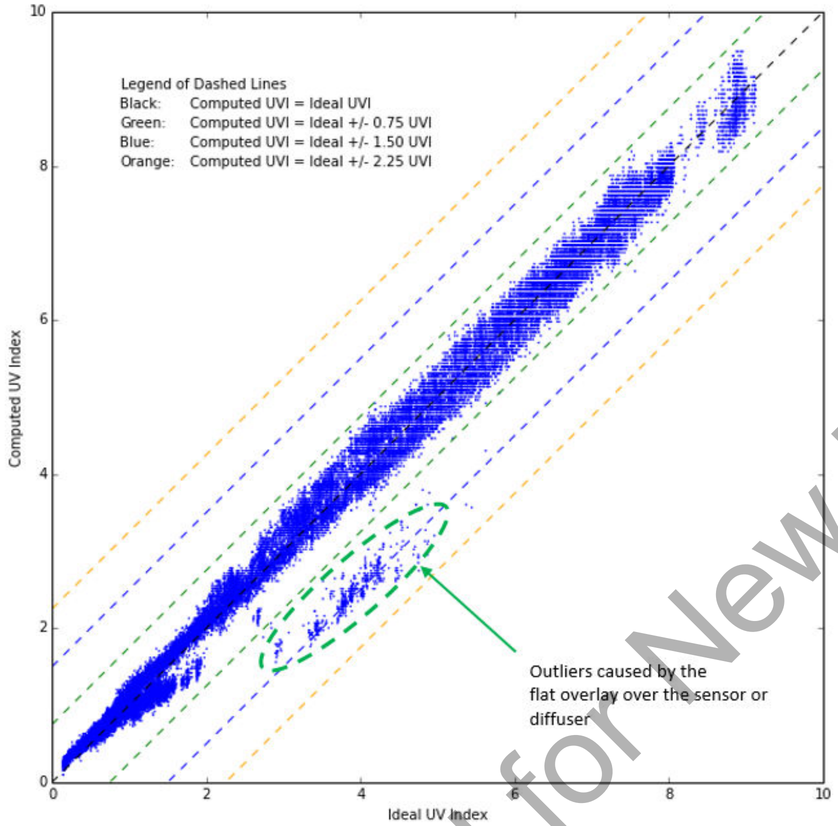


Figure 3.4. Typical UV Index Scatter Plot (+/- 30 º Angular View of a Teflon Diffuser)

The test setup is as follows:

Overlay	Corning Gorilla © Glass (0.7 mm thick)
Diffuser	0.8 mm dia. diffuser, 0.25 mm above QFN package, under glass
ADC Gain	9
Decimation Filter Setting	3
Samples Averaged / Reading	1
Formula	UV index = 0.0187(0.00391 $Input^2$ + Input)

3.3 Power Consumption

The Si1133 alternates between three power consumption states: Active, Suspend, and Sleep. (See the diagram below for an illustratation of each of these states.) The total power consumed by the part depends heavily on the measurement rate, measurement mode, and measurement gain for the various channels enabled. The power levels for the three modes, as well as the Active Power time per reading, are provided in this document. The Suspend time (where the A/D and PD are operating) has two parts. One is determined by the user setup and can be determined by the DECIM_RATE and HW_GAIN setup information, while the other (A/D Startup time) is determined by tadstart, shown in Table 8.2 Performance Characteristics[1] on page 35.

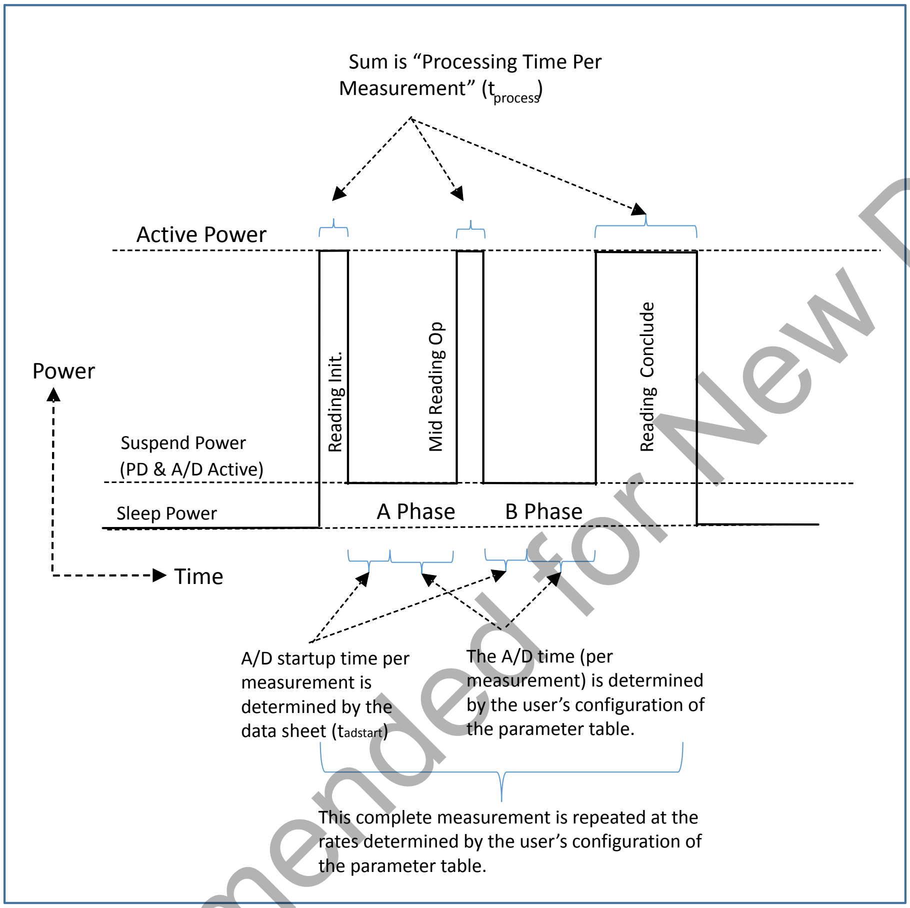


Figure 3.5. Power Consumption States During a Reading

Every A/D conversion has three periods:

155 µs at 4.5 mA	(setup time by internal controller)
48.8 µs at 525 µA	(setup time by A/D)
48.8 µs * (2 ** gain) at 525 µA	(Actual A/D time that will vary with integration time)

3.4 Host Interface

The host interface to the Si1133 consists of three pins:

- SCL
- SDA
- INT

SCL and SDA are standard open-drain pins as required for I2C operation.The Si1133 asserts the INT pin to interrupt the host processor. The INT pin is an open-drain output. A pull-up resistor is needed for proper operation. As an open-drain output, it can be shared with other open-drain interrupt sources in the system.

For proper operation, the Si1133 is expected to fully complete its Initialization Mode prior to any activity on the I2C.

The INT, SCL, and SDA pins are designed so that it is possible for the Si1133 to enter the Off Mode by software command without interfering with normal operation of other I2C devices on the bus.

The I2C interface allows access to the Si1133 internal registers.

An I2C write access always begins with a start (or restart) condition. The first byte after the start condition is the I2C address and a read-write bit. The second byte specifies the starting address of the Si1133 internal register. Subsequent bytes are written to the Si1133 internal register sequentially until a stop condition is encountered. An I2C write access with only two bytes is typically used to set up the Si1133 internal address in preparation for an I2C read.

The I2C read access, like the I2C write access, begins with a start or restart condition. In an I2C read, the I2C master then continues to clock SCK to allow the Si1133 to drive the I2C with the internal register contents.The Si1133 also supports burst reads and burst writes. The burst read is useful in collecting contiguous, sequential registers. The Si1133 register map was designed to optimize for burst reads for interrupt handlers, and the burst writes are designed to facilitate rapid programming of commonly used fields, such as thresholds registers.

The internal register address is a six-bit (bit 5 to bit 0) plus an Auto increment Disable (on bit 6). The Auto increment Disable is turned off by default. Disabling the auto incrementing feature allows the host to poll any single internal register repeatedly without having to keep updating the Si1133 internal address every time the register is read.

It is recommended that the host should read performance measurements (in the I2C Register Map) when the Si1133 asserts INT. Although the host can read any of the Si1133's I2C registers at any time, care must be taken when reading 2-byte measurements outside the context of an interrupt handler. The host could be reading part of the 2-byte measurement when the internal sequencer is updating that same measurement coincidentally. When this happens, the host could be reading a hybrid 2-byte quantity whose high byte and low byte are parts of different samples. If the host must read these 2-byte registers outside the context of an interrupt handler, the host should "double-check" a measurement if the measurement deviates significantly from a previous reading.

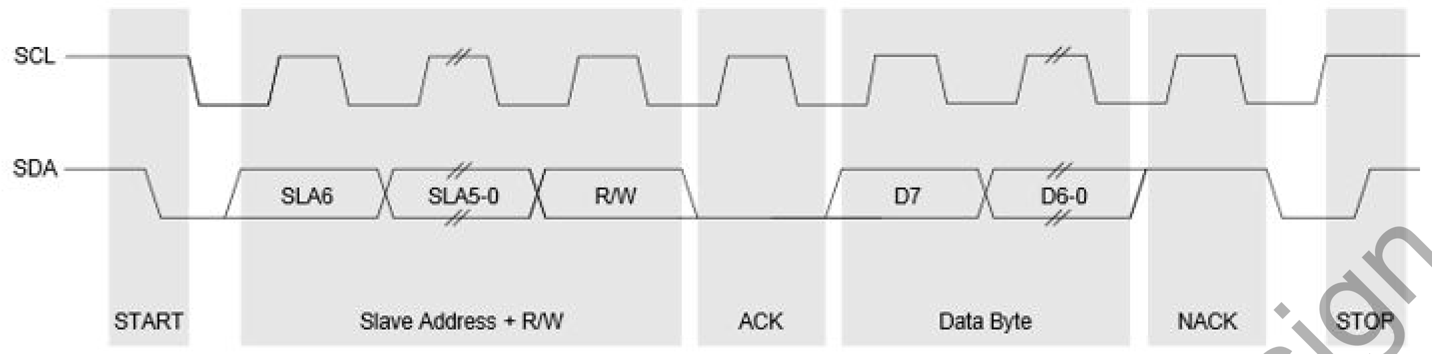


Figure 3.6. I²C Bit Timing Diagram

S	SLAVE ID	0	A	REG ADDRESS	A	DATA	A	P

Figure 3.7. Host Interface Single Write

S	SLAVE ID	1	A	DATA	N	STOP

Figure 3.8. Host Interface Single Read

S	SLAVE ID	0	A	REG ADDRESS	A	DATA	A	DATA	A	DATA	A	P

Figure 3.9. Host Interface Burst Write

S	SLAVE ID	0	A	REG ADDRESS	A	Sr	SLAVE ID	1	A	DATA	A	DATA	A	DATA	N	STOP

Figure 3.10. Host Interface Burst Read

7	6	5:0
0	AI	6 bit address 0x00 to 0x3F

Figure 3.11. Si1133 REG ADDRESS Format

The following notes apply for the figures above:

1. Gray boxes are driven by the host to the Si1133.
2. White boxes are driven by the Si1133.
3. A = ACK or "acknowledge".
4. N = NACK or "no acknowledge".
5. S = START condition.
6. Sr = repeat START condition.
7. P = STOP condition.
8. AI = Disable Auto Increment when set.

4. Operational Modes

The Si1133 can be in one of many operational modes at any time. It is important to consider the operation mode, since the mode has an impact on the overall power consumption of the Si1133. The various modes are:

- Off Mode
- Initialization Mode
- Standby Mode
- Forced Conversion Mode
- Autonomous Mode

4.1 Off Mode

The Si1133 is in the Off Mode when V_{DD} is either not connected to a power supply or if the V_{DD} voltage is below the stated VDD_OFF voltage described in the electrical specifications. As long as the parameters stated in are not violated, no current will flow through the Si1133. In the Off Mode, the Si1133 SCL and SDA pins do not interfere with other I^2C devices on the bus. Keeping V_{DD} less than VDD_OFF is not intended as a method of achieving lowest system current draw. The reason is that the ESD protection devices on the SCL, SDA, and INT pins also draw from a current path through V_{DD}. If V_{DD} is grounded, for example, then current flows from system power to system ground through the SCL, SDA, and INT pull-up resistors and the ESD protection devices. Allowing V_{DD} to be less than VDD_OFF is intended to serve as a hardware method of resetting the Si1133 without a dedicated reset pin.

The Si1133 can also re-enter the Off Mode upon receipt of a software reset sequence. Upon entering Off Mode, the Si1133 proceeds directly from the Off Mode to the Initialization Mode.

4.2 Initialization Mode

When power is applied to V_{DD} and is greater than the minimum V_{DD} Supply Voltage stated in the electrical specification table, the Si1133 enters its Initialization Mode. In the Initialization Mode, the Si1133 performs its initial startup sequence. Since the I^2C may not yet be active, it is recommended that no I^2C activity occur during this brief Initialization Mode period. The “Start-up time” specification in the electrical specification table is the minimum recommended time the host needs to wait before sending any I^2C accesses following a power-up sequence. After Initialization Mode has completed, the Si1133 enters Standby Mode. During the Initialization mode, the I^2C address selection is made according to whether LED2 is pulled up or down.

4.3 Standby Mode

The Si1133 spends most of its time in Standby Mode. After the Si1133 completes the Initialization Mode sequence, it enters Standby Mode. While in Standby Mode, the Si1133 does not perform any Ambient Light or UV measurements. However, the I^2C interface is active and ready to accept reads and writes to the Si1133 registers. The internal Digital Sequence Controller is in its sleep state and does not draw much power. In addition, the INT output retains its state until it is cleared by the host.

I^2C accesses do not necessarily cause the Si1133 to exit the Standby Mode. For example, reading Si1133 registers is accomplished without needing the Digital Sequence Controller to wake from its sleep state.

4.4 Forced Conversion Mode

The Si1133 can operate in Forced Conversion Mode under the specific command of the host processor. The Forced Conversion Mode is entered when the FORCE command is sent. Upon completion of the conversion, the Si1133 can generate an interrupt to the host if the corresponding interrupt is enabled. It is possible to initiate both a UV and ALS measurement.

4.5 Automated Operation Mode

The Si1133 can be placed in the Autonomous Operation Mode where measurements are performed automatically without requiring an explicit host command for every measurement. The START command is used to place the Si1133 in the Autonomous Operation Mode.

The Si1133 updates the I^2C registers for UV and ALS automatically. The host can also choose to be notified when these new measurements are available by enabling interrupts. The conversion frequency for autonomous operation is set up by the host prior to the START command.

The Si1133 can also interrupt the host when the UV or ALS measurement reach a pre-set threshold. To assist in the handling of interrupts the registers are arranged so that the interrupt handler can perform an I^2C burst read operation to read the necessary registers, beginning with the interrupt status register, and cycle through the various output registers.

5. User to Sensor Communication

5.1 Basic I^{2}C Operation

I^{2}C operation is dependent on serial I^{2}C reads and writes to an addressable bank of memory referred to as I^{2}C space. The diagram below outlines the registers used, some functionality and the direction of data flow. The I^{2}C address is initially fixed but can be programmed to a new value. This new value is volatile and reverts to the old value on hardware or software reset. Only 7-bit I^{2}C addressing is supported; 10-bit I^{2}C addressing is not supported. The Si1133 responds to the I^{2}C address of 0x55 or to an alternate address of 0x52.

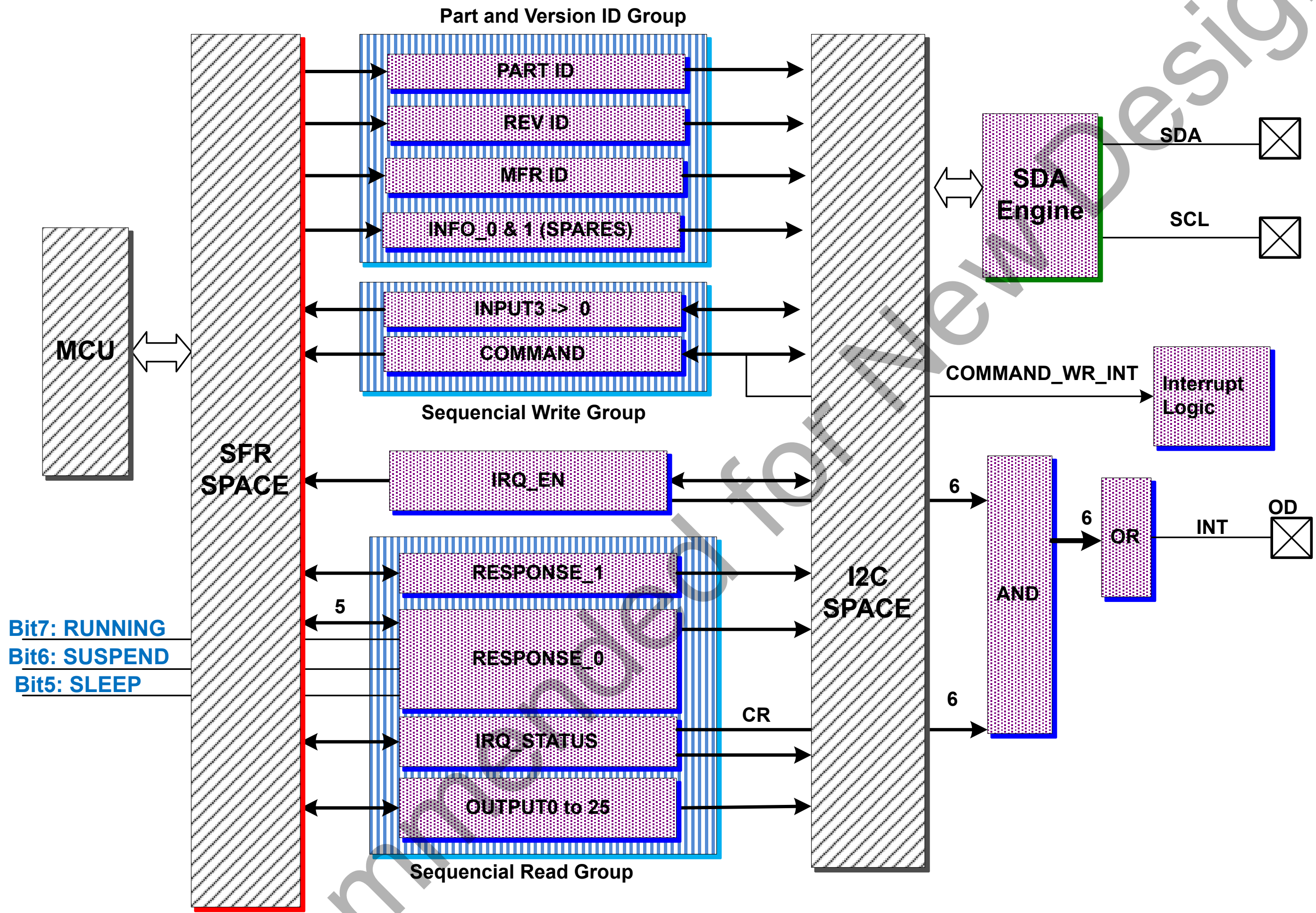


Figure 5.1. I^{2}C Interface Block Diagram

5.2 Relationship Between I2C Registers and Parameter Table

Note that most of the Si1133 configuration is accomplished through 'Parameters'. The Si1133 has an internal MCU with SRAM. The Parameters are stored in the Si1133 Internal MCU SRAM. The I2C Registers can be viewed as mailbox registers that form an interface between the host and the internal MCU. The figure below shows the relationship between some of the key interface registers to the internal Parameters managed by the internal MCU.

- The I2C registers are directly accessible by the host.
- The parameter table is:
  - Accessible indirectly via the command register (and others).
  - Used during setup to fix the operating modes of the Si1133.
  - 0x2C bytes long and is read and written indirectly, one bye at a time, via the command register.

The data stored in the parameter table is volatile and is lost when the part is powered down or software reset command is sent to the part via the I2C part.

I2C Registers Directly Accessible by Host

Register Name	I2C Address	Direction WRT Host
PART_ID	0	IN
REV_ID	1	IN
MFR_ID	2	IN
INFO0	3	IN
INFO1	4	IN
HOSTIN3	7	IN/OUT
HOSTIN2	8	IN/OUT
HOSTIN1	9	IN/OUT
HOSTIN0	0A	IN/OUT
COMMAND	0B	IN/OUT
IRQ_ENABLE	0F	IN/OUT
RESPONSE1	10	IN
RESPONSE0	11	IN
IRQ_STATUS	12	IN
HOSTOUT0	13	IN
HOSTOUT1	14	IN
HOSTOUT2	15	IN
HOSTOUT3	16	IN
HOSTOUT4	17	IN
HOSTOUT5	18	IN
HOSTOUT6	19	IN
HOSTOUT7	1A	IN
HOSTOUT8	1B	IN
HOSTOUT9	1C	IN
HOSTOUT10	1D	IN
HOSTOUT11	1E	IN
HOSTOUT12	1F	IN
HOSTOUT13	20	IN
HOSTOUT14	21	IN
HOSTOUT15	22	IN
HOSTOUT16	23	IN
HOSTOUT17	24	IN
HOSTOUT18	25	IN
HOSTOUT19	26	IN
HOSTOUT20	27	IN
HOSTOUT21	28	IN
HOSTOUT22	29	IN
HOSTOUT23	2A	IN
HOSTOUT24	2B	IN
HOSTOUT25	2C	IN

Fields used to write to Parameter Table

Sensor Parameter Table. Indirectly Accessible by Host

Parameter Address	NAME
0x00	I2C_ADDR
0x01	CHAN_LIST
0x02	ADCCONFIG0
0x03	ADCSENS0
0x04	ADCPOST0
0x05	MEASCONFIG0
0x06	ADCCONFIG1
0x07	ADCSENS1
0x08	ADCPOST1
0x09	MEASCONFIG1
0x0A	ADCCONFIG2
0x0B	ADCSENS2
0x0C	ADCPOST2
0x0D	MEASCONFIG2
0x0E	ADCCONFIG3
0x0F	ADCSENS3
0x10	ADCPOST3
0x11	MEASCONFIG3
0x12	ADCCONFIG4
0x13	ADCSENS4
0x14	ADCPOST4
0x15	MEASCONFIG4
0x16	ADCCONFIG5
0x17	ADCSENS5
0x18	ADCPOST5
0x19	MEASCONFIG5
0x1A	MEASRATE_H
0x1B	MEASRATE_L
0x1C	MEASCOUNT0
0x1D	MEASCOUNT1
0x1E	MEASCOUNT2
0x1F	Unused
0x20	Unused
0x21	Unused
0x22	Unused
0x23	Unused
0x24	Unused
0x25	THRESHOLD0_H
0x26	THRESHOLD0_L
0x27	THRESHOLD1_H
0x28	THRESHOLD1_L
0x29	THRESHOLD2_H
0x2A	THRESHOLD2_L
0x2B	BURST

Figure 5.2. Accessing Parameters through I2C Registers

5.3 I^{2}C Command Register Operation

Writing the codes shown below in the command summary table signals the sensor to undertake one of several complex operations.

These operations take time and all commands should be followed by a read of the RESPONSE0 register to confirm the operation is complete by examining the counter and to check for an error in the error bit. The error bit is set in the RESPONSE0 register's command counter if there is an error in the previous command (e.g., attempt to write to an illegal address beyond the parameter table, or a channel and /or burst configuration that exceeds the size of the output field (26 bytes)). If there is no such error, then the counter portion of the command counter will be incremented.

The RESPONSE_0 register should be read after every command to determine completion and to check for an error. If an error is found, which should not happen except for a host SW bug, the host should clear the error with a RESET command or a RESET_CMD_CTR command.

One operating option is to do a RESET_CMD_CTR command before every command.

Two of the commands imply another I^{2}C register contains an argument.

- STORE_NEW_I2C ADDR command implies a new address has been loaded in the parameter table location I2CID PARAMETER.
- PARAM_SET command implies a byte has been stuffed into INPUT0 register.
- The three CHAN_LIST commands imply the CHAN_LIST location in the parameter table has been configured. A valid CHAN_LIST implies other configuration areas in the parameter table are correctly setup as well.

Two of the commands result in another I^{2}C register containing return arguments (aside from incrementing RESPONSE0).

- PARAM_SET results in the write data being copied in to I2C RESPONSE1 register.
- PARAM_QUERY results in read data in the I2C RESPONSE1 register.

Table 5.1. Command Summary

Command Register Commands	Code	Input to Sensor	Output of Sensor
RESET_CMD_CTR Resets RESPONSE0 CMMND_CTR field to 0.	0x00	-----------	-----------
RESET_SW Forces a Reset, Resets RESPONSE0 CMMND_CTR field to 0xXXX01111.	0x01	-----------	-----------
FORCE Initiates a set of measurements specified in CHAN_LIST parameter. A FORCE command will only execute the measurements which do not have a meas counter index configured in MEAS-CONFIGx.	0x11	-----------	-----------
PAUSE Pauses autonomous measurements specified in CHAN_LIST.	0x12	-----------	-----------
START Starts autonomous measurements specified in CHAN_LIST. A START autonomous command will only start the measurements which has a counter index selected in MEASCONFIGx.	0x13	-----------	-----------
PARAM_QUERY Reads Parameter xxxxxx and store results in RE-SPONSE1.xxxxxx is a 6 bit Address Field (64 bytes).	0b01xxxxxx		RESPONSE1 = result
PARAM_SET Writes INPUT0 to the Parameter xxxxxx.xxxxxx is a 6 bit Address Field (64 bytes).	0b10xxxxxx	INPUT0	RESPONSE1 = INPUT0

Notes:

1. The successful completion of all commands except RESET_CMD_CTR and RESET_SW causes an increment of the CMD_CTR field of the RESPONSE0 register (bits [3:0].
2. Resets RESPONSE0 CMMND_CTR field to 0.
3. Forces a Reset, Resets RESPONSE0 CMMND_CTR field to 0xXXX01111.
4. Uses CHAN_LIST in Parameter Space.
5. "xxxxxx" is a 6-bit Address Field (64 bytes).

5.3.1 Accessing the Parameter Table (PARAM_QUERY & PARAM_SET Commands)

The parameter table is written to by writing the INPUT_0 I2C register and the PARAM_SET command byte to the Command I^2C register. The format of the PARAM_SET word is such that the 6 LSBits contain the location of the target byte in the parameter table.

Example: To transfer 0xA5 to parameter table location 0b010101.

Read RESPONSE0 (address 0x11)	and store the CMMND_CTR field.

Write 0xA5 to INPUT0 (address 0x0A).

Write 0b10010101 to COMMAND (address 0x0B).

Read RESPONSE0 (address 0x11)	and check if the CMMND_CTR field incremented.

If there is no increment or error, repeat the “read the RESPONSE0” step until the CMMND_CTR has incremented. If there is an error send a RESET or a RESET_CMD_CTR command.

The two write commands (to INPUT0 and COMMAND) can be in the same I^2C transaction.

Example: To read data from the parameter table location 0b010101.

Read the RESPONSE0 (address 0x11)	and store the CMMND_CTR field.

Write 0b01010101 to the COMMAND (address 0x0B).

Read RESPONSE0 (address 0x11)	and check if the CMMND_CTR field incremented.

If there is no increment or error, repeat the “read RESPONSE0” step until the CMMND_CTR has incremented.

Read RESPONSE1 (address 0x10)	this gives the read result. If there is an error send RESET or a RESET_CMD_CTR command.

The last two read commands (from RESPONSE0 and RESPONSE1) should not be in the same I^2C transaction.

5.3.2 Sensor Operation Initiation Commands

The FORCE, PAUSE, and START commands make use of the information in CHAN_LIST. Configure CHAN_LIST prior to using any of these commands.

5.3.3 RESET_CMD_CTR Command

Resets RESPONSE0 CMMND_CTR field and does nothing else.

5.3.4 RESET Command

Resets the sensor and puts it into the same state as when powering up. The parameter table and all I^2C registers are reset to their default values.

5.4 I²C Register Summary

The content of the three MSBits of Response0 after reset will depend on the running state (see the Response0 write up).

Table 5.2. I2C Registers

Register Name	I2C Address	Direction WRT Host	Function	Value after Reset (Hard or Soft)	Direction WRT Sensor
PART_ID	0x00	IN	Returns DEVID (0x33 for the Si1133).	PART_ID	OUT
HW_ID	0x01	IN	Returns Hardware ID.	HW_ID	OUT
REV_ID	0x02	IN	Hardware Rev (0xMN).	REV_ID	OUT
HOSTIN0	0x0A	IN/OUT	Data for parameter table on PARAM_SET write to COMMAND register.	0x00	IN
COMMAND	0x0B	IN/OUT	Initiated action in Sensor when specific codes written here.	0x00	IN
RESET	0x0F	IN/OUT	The six least significant bits enable Interrupt Operation.	0x00	IN
RESPONSE1	0x10	IN	Contains the readback value from a param query or a param set command.	0x00	IN/OUT
RESPONSE0	0x11	IN	The 5th MSB of the counter is an error indicator, with the 4 LSBits indicating the error code when the MSB is set.	0xXXXX1111	IN/OUT
IRQ_STATUS	0x12	IN	The six least significant bits show the interrupt status.	0x00	IN/OUT
HOSTOUT0 to HOSTOUT25	0x13 to 0x2C	IN	Captured Sensor Data.	0x00	IN/OUT

5.4.1 PART_ID

I2C Address = 0x00;

Contains Part ID, e.g., 0x33 for Si1133.

5.4.2 HW_ID

I2C Address = 0x01;

Contains the Hardware information.

BITS4:0 = Implementation Code

BITS7:5 = Silicon HW rev (Steps with silicon mask change)

Part Number	Features	BITS4:0 code
Si1133-AA00	UV and ALS Sensor	0x03

5.4.3 REV_ID

I2C Address = 0x02;

Contains the product revision, in a 0xMN format where “M” is the major rev and “N” the minor rev.

5.4.4 INFO0

I2C Address = 3;

Contains 0 after a hard reset or a RESET Command.

5.4.5 INFO1

I2C Address = 4;

Contains 0 after a hard reset or a RESET Command.

5.4.6 HOSTIN0

Name	I2C Address
HOSTIN0	0x0A

Bit	7	6	5	4	3	2	1	0
Name	HOSTIN0							
Type	R/W							
Reset	0							

Bit	Name	Function
7:0	HOSTIN0	This Register is the Input to the Sensor and Output of the Host.

Contain 0 after a hard reset or a RESET Command.

5.4.7 COMMAND

I2C Address = 0x0B;

Contains 0 after a hard reset or a RESET Command.

5.4.8 IRQENABLE

I2C Address = 0x0F;

Contains 0 after a hard reset or a RESET Command.

5.4.9 RESPONSE1

I2C Address = 0x10;

Bit	7	6	5	4	3	2	1	0
Name	RESPONSE1[7:0]							
Type	R							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	RESPONSE1[7:0]	The sensor mirrors the data byte written to the parameter table here for the user to verify the write was successful. A parameter read command results in the byte read being available here for the host.

5.4.10 RESPONSE0

I2C Address = 0x11;

Bit	7	6	5	4	3	2	1	0
Name	RUNNING	SUSPEND	SLEEP	CMD_ERR	CMD_CTR[4:0]			
Type	R	R	R	R	R	R	R	R
Reset	N/A	N/A	N/A	0	1	1	1	1

<table>
<tr><th>Bit</th><th>Name</th><th colspan="3">Function</th></tr>
<tr><td>7</td><td>RUNNING</td><td colspan="3">Indicator of MCU state.</td></tr>
<tr><td>6</td><td>SUSPEND</td><td colspan="3">Indicator of MCU state.</td></tr>
<tr><td>5</td><td>SLEEP</td><td colspan="3">Indicator of MCU state.</td></tr>
<tr><td>4</td><td>CMD_ERR</td><td colspan="3">It is cleared by a hardware reset (power up) or a RESET command or a RESET_CMD_CTR.

It is set by a bad command. E.g., an attempt to write beyond the parameter table.

If it is set, the CMMND_CTR field is the error code.</td></tr>
<tr><td rowspan="6">3:0</td><td rowspan="6">CMMND_CTR</td><td>IF CMD_ERR = 0</td><td colspan="2">A counter that increments on every GOOD command (successful I2C Command Register write and sensor execution of the command).

It is reset to 0 by the RESET_CMD_CTR command.

It is set to 0b1111 on Power Up or a RESET command. This is how a user can detect a fresh SW reset or a power up event.</td></tr>
<tr><td rowspan="5">IF CMD_ERR = 1</td><td>Code</td><td>Meaning</td></tr>
<tr><td>0x10</td><td>Invalid command.</td></tr>
<tr><td>0x11</td><td>Parameter access to an invalid location.</td></tr>
<tr><td>0x12</td><td>Saturation of the ADC or overflow of accumulation.</td></tr>
<tr><td>0x13</td><td>Output buffer overflow—this can happen when Burst mode is enabled and configured for greater than 26 bytes of output.</td></tr>
</table>

The RESPONSE0 register will show “RUNNING” immediately after reset and then “SLEEP” after initialization is complete.

5.4.11 IRQ_STATUS

I2C Address = 0x12;

Bit	7	6	5	4	3	2	1	0
Name	—		IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
Type	RSVD		CR	CR	CR	CR	CR	CR
Reset			0	0	0	0	0	0

Bit	Name	Function
7:6	UNUSED	Unused. Read = 00b; Write = Don't Care.
5	IRQ5	Enables an IRQ for channel 5 result being ready.
4	IRQ4	Enables an IRQ for channel 4 result being ready.
3	IRQ3	Enables an IRQ for channel 3 result being ready.
2	IRQ2	Enables an IRQ for channel 2 result being ready.
1	IRQ1	Enables an IRQ for channel 1 result being ready
0	IRQ0	Enables an IRQ for channel 0 result being ready.

5.4.12 HOSTOUTx

This section covers the twenty-six I2C Host Output Registers. These registers are the output of the sensor and input to the host.

Name	I2C Address
HOSTOUT0 to HOSTOUT25	0x13 to 0x2C

Bit	7	6	5	4	3	2	1	0
Name	HOSTOUTx							
Type	R							
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function
7:0	HOSTOUTx	These registers are the output of the MCU and input to the host. The results of the CHAN_LIST enabled "active channel" readings are located sequentially in this table. Each channel may use 2 or 3 bytes depending on the setup. The validity of the various channel outputs located in this table is determined by other factors. Data is valid when an IRQ status says that it is and remains valid until another reading happens. This is why it is imperative to service the interrupt before the next measurement cycle begins (Autonomous Mode), unless forced mode is used.

6. Measurement: Principle of Operation

Operation is based on the concept of channels. Channels are essentially tasks that have been setup by the user.

To setup these channels, the channel specific areas of the parameter table need to be loaded with the correct information as well as the global area of this table.

The channels' specific areas are described below, including:

- ADC gain
- The photodiode selected
- The counter selected to time
- How often to make a measurement
- The format of the output (16 vs. 24 bits)
- And other areas

The global area includes global information that affect all tasks, such as:

- The list of channels that are enabled.
- The setup of the two counters that can be used by the channels.
- The three light thresholds that can be selected from by the channels.

The list of channels, CHAN_LIST, in the global area determines what operations are run and how the results are packed in the output fields.

The packing of the result data in the output fields is totally determined by the enabled channels as they are packed sequentially from the lowest enabled channel to the highest in the output field (I2C space- HOSTOUT0 to HOSTOUT25). The amount of space used by each channel is determined by the 16 vs. 24 bit selection made in the channel setup.

Although space in the output buffer is reserved by the CHAN_LIST, the data validity is determined by the IRQ_STATUS register in Autonomous Mode and by elapsed time in Forced Mode. In Burst Mode, a subset of Autonomous Mode, all the expected data is valid.

6.1 Output Field Utilization

In all modes, the CHAN_LIST configuration determines how the data is stacked in the 26 byte output field. It is done on a first-come first-served basis, with the enabled lower channels taking up the lower addresses. When burst is enabled, the channel arrangement is just repeated to higher and higher addresses. See the example below.

Global Section of Parameter Table			Channel Specific Section of Parameter Table
CHAN_LIST			Output mode
0	Bit 0	Chan 0	16
1	Bit 1	Chan 1	24
0	Bit 2	Chan 2	16
1	Bit 3	Chan 3	16
1	Bit 4	Chan 4	24
1	Bit 5	Chan 5	16
X	Bit 6	X	X
X	Bit 7	X	X

I2C Register	I2C Addresss	Content
HOSTOUT0	13	Channel 1 Result: Most Signoficant Byte
HOSTOUT1	14	Channel 1 Result: Middle Signoficant Byte
HOSTOUT2	15	Channel 1 Result Least Signoficant Byte
HOSTOUT3	16	Channel 3 Result: Most Signoficant Byte
HOSTOUT4	17	Channel 3 Result Least Signoficant Byte
HOSTOUT5	13	Channel 4 Result: Most Signoficant Byte
HOSTOUT6	14	Channel 4 Result: Middle Signoficant Byte
HOSTOUT7	1A	Channel 4 Result Least Signoficant Byte
HOSTOUT8	1B	Channel 5 Result: Most Signoficant Byte
HOSTOUT9	1C	Channel 5 Result Least Signoficant Byte
HOSTOUT10	1D	Unused
HOSTOUT11	1E	Unused
HOSTOUT12	1F	Unused
HOSTOUT13	20	Unused
HOSTOUT14	21	Unused
HOSTOUT15	22	Unused
HOSTOUT16	23	Unused
HOSTOUT17	24	Unused
HOSTOUT18	25	Unused
HOSTOUT19	26	Unused
HOSTOUT20	27	Unused
HOSTOUT21	28	Unused
HOSTOUT22	29	Unused
HOSTOUT23	2A	Unused
HOSTOUT24	2B	Unused
HOSTOUT25	2C	Unused

Packing of of these four channels in the output table is determined by the four enabled channels in the CHANNEL list above. This is independent of the IRQ_ENABLE and IRQ_STATUS

Figure 6.1. Output Table Data Packing

6.2 Autonomous and Forced Modes

In Autonomous Mode, the user uses the timer fields in both the global and channels specific areas in order to set up the timing for repeated measurements. The user then sends the command to start these autonomous measurements repeatedly. When each channel's timer is tripped, the measurement for that channel is started. When the channel measurement completes, it is signaled by the IRQ_STATUS bits and by an interrupt (if the interrupt is enabled). After that signal, the sensor restarts the channel timer and waits for it to trip and signal the next measurement. The host must read the data before the next reading is generated, or risk losing the reading or getting garbage data to sample smearing (reading data in the midst of it changing).

In Forced Mode, all measurements enabled in the CHAN_LIST start as a result of a FORCE command and are only done once. If there are multiple channels enabled, then the measurements are done back-to-back starting with the lower number channel.The completion signaling is the same as for autonomous, the IRQ_STATUS and interrupt if it is enabled. The logical difference is that all the enabled channels are always shown as simultaneously ready in the IRQ_STATUS, whereas in Autonomous Mode this is not true. FORCE command only works on measurements which do not have a measurement counter selected in MEASCONFIGx.

Global Section of Parameter Table			Channel Specific Section of Parameter Table
CHAN_LIST			Output mode
0	Bit 0	Chan 0	16
1	Bit 1	Chan 1	24
0	Bit 2	Chan 2	16
1	Bit 3	Chan 3	16
1	Bit 4	Chan 4	24
1	Bit 5	Chan 5	16
X	Bit 6	X	X
X	Bit 7	X	X

I2C SPACE		
IRQ_STATUS		
Value	Bit	Meaning
0	Bit 0	Chan 0
0	Bit 1	Chan 1
0	Bit 2	Chan 2
1	Bit 3	Chan 3
0	Bit 4	Chan 4
1	Bit 5	Chan 5
X	Bit 6	X
X	Bit 7	X

I2C Register	I2C Addresss	Content
HOSTOUT0	13	Channel 1 Result: Most Signoficant Byte
HOSTOUT1	14	Channel 1 Result: Middle Signoficant Byte
HOSTOUT2	15	Channel1 Result: Least Signoficant Byte
HOSTOUT3	16	Channel 3 Result: Most Signoficant Byte
HOSTOUT4	17	Channel3 Result: Least Signoficant Byte
HOSTOUT5	13	Channel 4 Result: Most Signoficant Byte
HOSTOUT6	14	Channel 4 Result: Middle Signoficant Byte
HOSTOUT7	1A	Channel4 Result: Least Signoficant Byte
HOSTOUT8	1B	Channel 5 Result: Most Signoficant Byte
HOSTOUT9	1C	Channel5 Result: Least Signoficant Byte
HOSTOUT10	1D	Unused
HOSTOUT11	1E	Unused
HOSTOUT12	1F	Unused
HOSTOUT13	20	Unused
HOSTOUT14	21	Unused
HOSTOUT15	22	Unused
HOSTOUT16	23	Unused
HOSTOUT17	24	Unused
HOSTOUT18	25	Unused
HOSTOUT19	26	Unused
HOSTOUT20	27	Unused
HOSTOUT21	28	Unused
HOSTOUT22	29	Unused
HOSTOUT23	2A	Unused
HOSTOUT24	2B	Unused
HOSTOUT25	2C	Unused

The IRQ_STATUS bits signal which of the possible fields are updated with new information. All other fields should be considered invalid and possibly containing wrong transitory information.

This is despite the reserved space in the output table for the readings that have not yet happened.

Figure 6.2. IRQ_STATUS Shows Which Output Fields Have Valid Data

6.3 Burst Mode

Burst Mode is always used in Autonomous Mode.

The Burst Mode is enabled by the BURST register's bit 7. The burst register is in the global area of the parameter table. Bits 6:0 of the register define the number of readings to be made.

All channels set up in the CHAN_LIST operate in this mode and they operate in unison governed by the MEASRATE register in the parameter table. The individual channel MEASCONFIGx.COUNTER_INDEX [1:0] value is ignored.

The burst is started by the START command and may be paused by the PAUSE command. All measurements enabled in the CHAN_LIST are done as a quick set then repeated after the delay determined by the MEASRATE register. The number of repeats are set by the BURST register.

The measurements called for by the enabled channels are done without an intervening delay, starting with the lower number channel and ending with the highest channel number.

The burst will proceed until it is complete or until the output buffer is full, after which an interrupt may be generated if enabled and the IRQ_STATUS bit(s) associated with all the channels in the CHAN_LIST will be set. The user has the time period until the next set of reads are finished to read back the data in the output field.

The output data will be stacked in the 26 bytes output data field and will be sequential. For example, if the CHAN_LIST enables channels X, Y, and Z, then the data will be found in the output buffer as multiple sets: X1, Y1, Z1, X2, Y2, Z2... The fields X, Y, and Z are packed efficiently and are not necessarily the same length since they can be a mix of 16 and 24 bit values.

I2C SPACE		
IRQ_STATUS When Done		
Value	Bit	Meaning
0	Bit 0	Chan 0
1	Bit 1	Chan 1
0	Bit 2	Chan 2
1	Bit 3	Chan 3
1	Bit 4	Chan 4
1	Bit 5	Chan 5
X	Bit 6	X
X	Bit 7	X

Global Section of Parameter Table			Channel Specific Section of Parameter Table
CHAN_LIST			Output mode
0	Bit 0	Chan 0	16
1	Bit 1	Chan 1	24
0	Bit 2	Chan 2	16
1	Bit 3	Chan 3	16
1	Bit 4	Chan 4	24
1	Bit 5	Chan 5	16
X	Bit 6	X	X
X	Bit 7	X	X

Since The CHAN_LIST shows 4 active channels we see two sets of readings stacked one after another.

I2C Register	I2C Addresss	Content
HOSTOUT0	13	Channel 1 Result: Most Signoficant Byte
HOSTOUT1	14	Channel 1 Result: Middle Signoficant Byte
HOSTOUT2	15	Channel 1 Result: Least Signoficant Byte
HOSTOUT3	16	Channel 3 Result: Most Signoficant Byte
HOSTOUT4	17	Channel 3 Result: Least Signoficant Byte
HOSTOUT5	13	Channel 4 Result: Most Signoficant Byte
HOSTOUT6	14	Channel 4 Result: Middle Signoficant Byte
HOSTOUT7	1A	Channel 4 Result: Least Signoficant Byte
HOSTOUT8	1B	Channel 5 Result: Most Signoficant Byte
HOSTOUT9	1C	Channel 5 Result: Least Signoficant Byte
HOSTOUT10	1D	Channel 1 Result: Most Signoficant Byte
HOSTOUT11	1E	Channel 1 Result: Middle Signoficant Byte
HOSTOUT12	1F	Channel 1 Result: Least Signoficant Byte
HOSTOUT13	20	Channel 3 Result: Most Signoficant Byte
HOSTOUT14	21	Channel 3 Result: Least Signoficant Byte
HOSTOUT15	22	Channel 4 Result: Most Signoficant Byte
HOSTOUT16	23	Channel 4 Result: Middle Signoficant Byte
HOSTOUT17	24	Channel 4 Result: Least Signoficant Byte
HOSTOUT18	25	Channel 5 Result: Most Signoficant Byte
HOSTOUT19	26	Channel 5 Result: Least Signoficant Byte
HOSTOUT20	27	Unused
HOSTOUT21	28	Unused
HOSTOUT22	29	Unused
HOSTOUT23	2A	Unused
HOSTOUT24	2B	Unused
HOSTOUT25	2C	Unused

Reading Set 1 (HOSTOUT0–HOSTOUT9)

Reading Set 1 (HOSTOUT10–HOSTOUT19)

In burst mode the I2C HOSTOUT locations are updated simultaneously when the burst is done. Only then will the IRQ_STATUS field be updates and an int generated (if the correct IRQ_ENABLE bit(s) is set).

Figure 6.3. Burst Mode Example of Two Sets of Readings

6.4 Interrupt Operation

The INT output pin is asserted by the sensor when an enabled channel in the CHAN_LIST (which has the corresponding bit in the RESET register) has finished. In Burst Mode, the interrupt is delayed until the number of readings is reached or the buffer is full.

When the host reads the IRQ_STATUS register to learn which source generated the interrupt, the IRQ_STATUS register is cleared automatically.

The most efficient method of extracting measurements from the Si1133 is an I^2C Burst Read beginning at the IRQ_STATUS register.

6.5 Timing of Channel Measurements

The timing of measurements has two aspects:

1. The length of time to take a measurement.
2. How frequently the measurement is taken.

The amount of time to take the measurement is controlled by factors like HW_GAIN (which is really the integration time), SW_GAIN, and the decimation rate setting.

Note: Each measurement is composed of two measurement times.

In an ALS measurement, two measurements are always taken and added together.

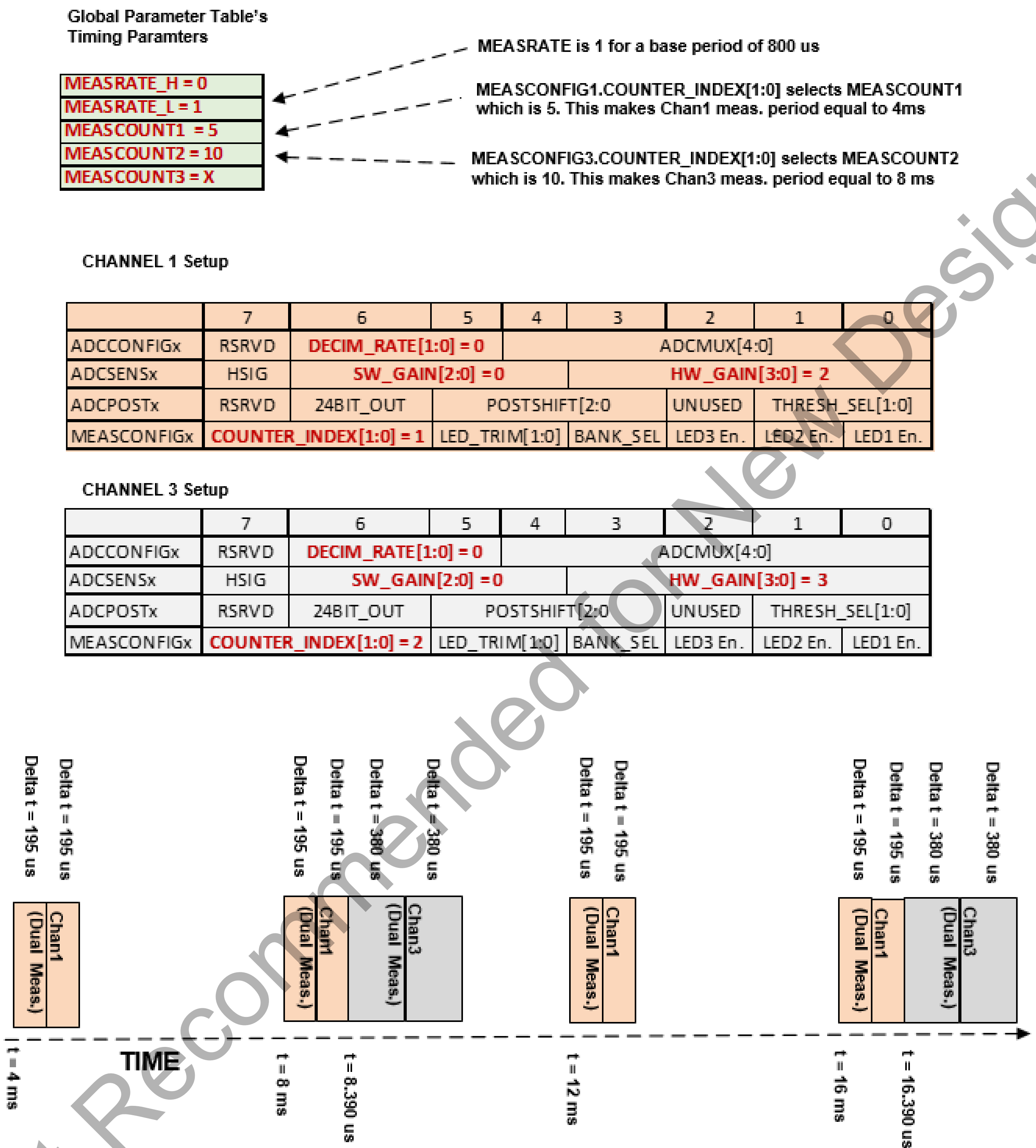


Figure 6.4. Example of Measurement Timing

7. Parameter Table

Table 7.1. Parameter Table

Address	Name	Description	
0x00	I2C_ADDR	I2C Address (Temp)	Global Area: Affects all Channels
0x01	CHAN_LIST	Channel List	
0x02	ADCCONFIG0	Channel 0 Setup	Channel Areas: Specific Channel Setup
0x03	ADCSENS0		
0x04	ADCPOST0		
0x05	MEASCONFIG0		
0x06	ADCCONFIG1	Channel 1 Setup	
0x07	ADCSENS1		
0x08	ADCPOST1		
0x09	MEASCONFIG1		
0x0A	ADCCONFIG2	Channel 2 Setup	
0x0B	ADCSENS2		
0x0C	ADCPOST2		
0x0D	MEASCONFIG2		
0x0E	ADCCONFIG3	Channel 3 Setup	
0x0F	ADCSENS3		
0x10	ADCPOST3		
0x11	MEASCONFIG3		
0x12	ADCCONFIG4	Channel 4 Setup	
0x13	ADCSENS4		
0x14	ADCPOST4		
0x15	MEASCONFIG4		
0x16	ADCCONFIG5	Channel 5 Setup	
0x17	ADCSENS5		
0x18	ADCPOST5		
0x19	MEASCONFIG5		

Address	Name	Description	
0x1A	MEASRATE_H	MEASURE RATE	Global Area: Affects all Channels
0x1B	MEASRATE_L		
0x1C	MEASCOUNT0	MEASCOUNT	
0x1D	MEASCOUNT1		
0x1E	MEASCOUNT2		
0x25	THRESHOLD0_H	THRESHOLD SETUP	
0x26	THRESHOLD0_L		
0x27	THRESHOLD1_H		
0x28	THRESHOLD1_L		
0x29	THRESHOLD2_H		
0x2A	THRESHOLD2_L		
0x2B	BURST	BURST	

7.1 Global Area of the Parameter Table

The Global Area represents resources that are shared among the six channels. See the next section for specific channel properties, and for channel-specific parameter setup.

Table 7.2. Global Area of the Parameter Table

Parameter	Parameter Address			
MEASRATE[1]	0x1A	MEASRATE[15:8]	Main Measurement Rate Counter	Governs how much time between measurement groups. One count represents an 800 µs time period.
MEASRATE[0]	0x1B	MEASRATE[7:0]		
MEASCOUNT0	0x1C	MEASCOUNT0[7:0]	Three Measurement Rate extension counters available for setting the rate.	Each of 6 channel setups selected which of these counters to use via the MEASCONFIG::COUNTER_INDEX[1:0] bits:
MEASCOUNT1	0x1D	MEASCOUNT1[7:0]		
MEASCOUNT2	0x1E	MEASCOUNT2[7:0]		
THRESHOLD0[1]	0x25	THRESHOLD0[15:8]	THRESHOLD0	One of these three (or none) us Chosen by MEASCONFIGx.THRESH_SEL[1:0]
THRESHOLD0[0]	0x26	THRESHOLD0[7:0]		
THRESHOLD1[1]	0x27	THRESHOLD1[15:8]	THRESHOLD1	
THRESHOLD1[0]	0x28	THRESHOLD1[7:0]		
THRESHOLD2[1]	0x29	THRESHOLD2[15:8]	THRESHOLD2	
THRESHOLD2[0]	0x2A	THRESHOLD2[7:0]		
BURST	0x2B	BURST[7:0]		Bit 7 is Burst Enable while BURST_COUNT[6:0] are the count
CHAN_LIST	0x01	CHAN_LIST[5:0]		The six least significant bits enable the 6 possible channels.

7.2 Channel Specific Setup Areas of the Parameter Table

Below is the summary of the four-byte channel-specific area in the parameter table. There are six copies in the table corresponding to up to six tasks/channels assigned to the sensor. They are located between addresses 0x02 and 0x18 hex.

Table 7.3. Channel Specific Setup Areas of the Parameter Table

<table>
<tr><th></th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>ADCCONFIGx</td><td>RSRVD</td><td colspan="2">DECIM_RATE[1:0]</td><td colspan="5">ADCMUX[4:0]</td></tr>
<tr><td>ADCSENSx</td><td>HSIG</td><td colspan="3">SW_GAIN[2:0]</td><td colspan="4">HW_GAIN[3:0]</td></tr>
<tr><td>ADCPOSTx</td><td>RSRVD</td><td>24BIT_OUT</td><td colspan="3">POSTSHIFT[2:0]</td><td>UNUSED</td><td colspan="2">THRESH_SEL[1:0]</td></tr>
<tr><td>MEASCONFIGx</td><td colspan="2">COUNTER_INDEX[1:0]</td><td colspan="6">RSRVD(5:0)</td></tr>
</table>

The following figure illustrates how to use the channel-specific registers in the parameter table above.

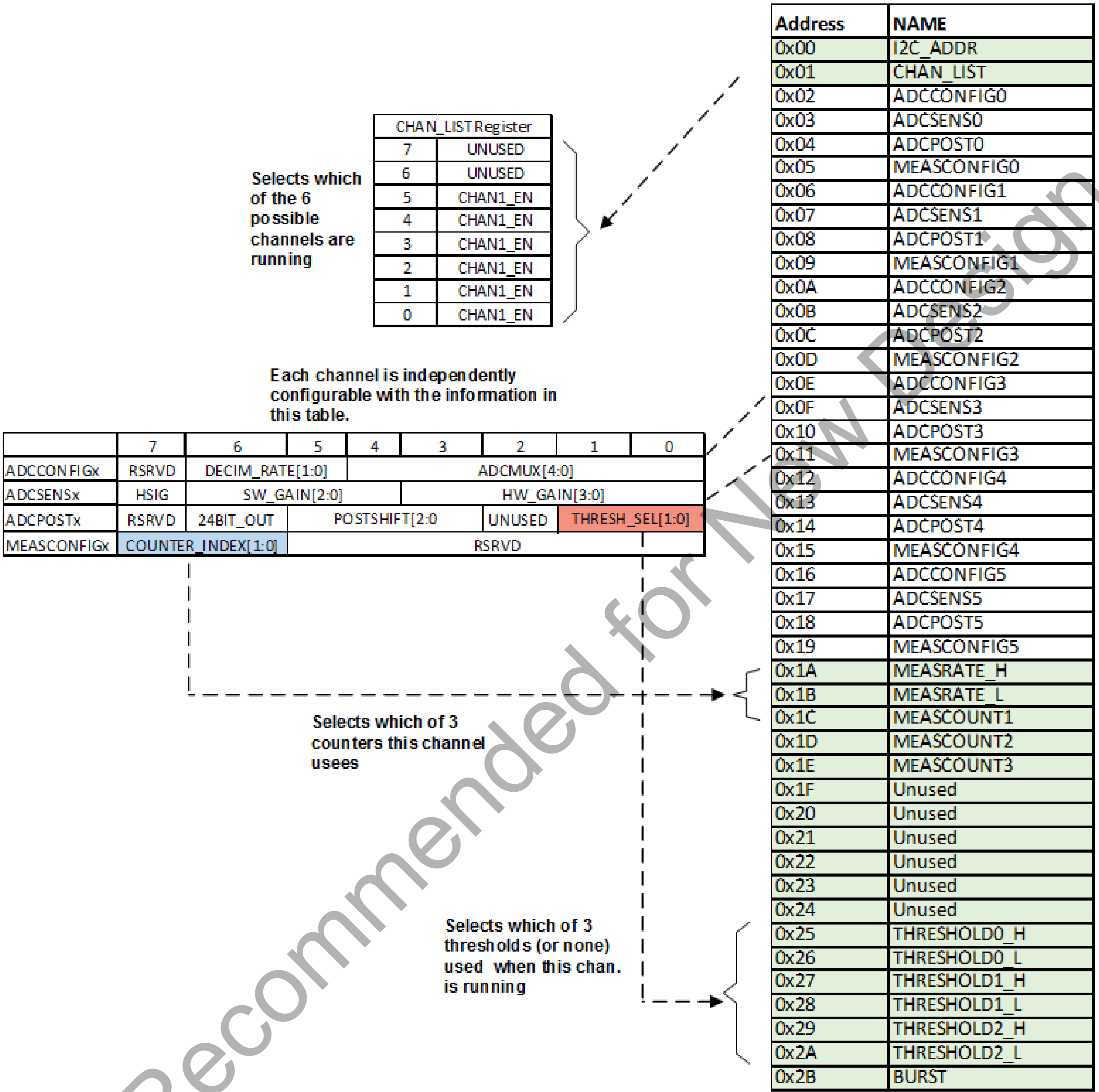


Figure 7.1. THRESH_SEL, COUNTER_INDEX Fields in Each Channel Specific Register Area Points to Global Area Register THRESHOLDx and MEASCOUNTx (Respectively)

Note: In the figure above, the counter selected (1, 2, or 3) defines the number of 800 µs periods to have between readings when the channel runs. The threshold selected (0, 1, or 2) defines the threshold used.

7.2.1 ADCCONFIGx

<table>
<tr><th colspan="9">Parameter Addresses: 0x02, 0x06, 0x0A, 0x0E, 0x12, 0x16</th></tr>
<tr><th>Bit</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Name</td><td>Reserved</td><td colspan="2">DECIM_RATE[1:0]</td><td colspan="5">ADCMUX[4:0]</td></tr>
<tr><td>Reset</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

<table>
<tr><th>Bit</th><th>Name</th><th colspan="8">Function</th></tr>
<tr><td>7</td><td>RESERVED</td><td colspan="8">Must remain at 0.</td></tr>
<tr><td rowspan="7">6:5</td><td rowspan="7">DEC-
IM_RATE[1:0]</td><td colspan="8">Selects Decimations rate of A/Ds. This setting affects the number of clocks used per measurements. Decimation rate is an A/D optimization parameter. The most common decimation value is 0 for a 1024 clocks and 48.8 µs min measurement time. Consult the related application notes for more details.

Increasing the reading time by using more clocks does not cause the ADC count to be larger.</td></tr>
<tr><td colspan="2">Value</td><td colspan="2">No of 21 MHz Clocks</td><td>Measurement time at HW_GAIN[3:0] = 0</td><td>Measurement time at HW_GAIN[3:0] = n</td><td colspan="2">Usage</td></tr>
<tr><td colspan="2"></td><td colspan="2"></td><td colspan="2">Note: All measurements are repeated 2X internally for ADC offset cancellation purposes. The times below represent the integration time for one of these measurement pairs.</td><td colspan="2"></td></tr>
<tr><td colspan="2">0</td><td colspan="2">1024</td><td>48.8 µs</td><td>48.8*(2**n) µs</td><td colspan="2">Normal</td></tr>
<tr><td colspan="2">1</td><td colspan="2">2048</td><td>97.6 µs</td><td>97.6*(2**n) µs</td><td colspan="2">Useful for longer short measurement times</td></tr>
<tr><td colspan="2">2</td><td colspan="2">4096</td><td>195 µs</td><td>195*(2**n) µs</td><td colspan="2">Useful for longer short measurement times</td></tr>
<tr><td colspan="2">3</td><td colspan="2">512</td><td>24.4 µs</td><td>24.4*(2**n) µs</td><td colspan="2">Useful for very short measurement times</td></tr>
<tr><td rowspan="9">4:0</td><td rowspan="9">ADCMUX[4:0]</td><td colspan="8">The ADC Mux selects which photodiode(s) are connected to the ADCs for measurement.

See Photodiode Section for more information regarding the location of the photodiodes.</td></tr>
<tr><td colspan="5">ADCMUX[4:0]</td><td>Optical Functions</td><td>Operation</td><td>Comments</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Small IR</td><td>D1b</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>Medium IR</td><td>D1b + D2b</td><td></td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Large IR</td><td>D1b + D2b + D3b + D4b</td><td></td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>White</td><td>D1</td><td></td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Large White</td><td>D1 + D4</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>UV</td><td>D - 10</td><td></td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>UV-Deep</td><td>D - 10b</td><td></td></tr>
</table>

7.2.2 ADCSENSx

Parameter Addresses: 0x03, 0x07, 0x0B, 0x0F, 0x13, 0x17								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	HSIG	SW_GAIN[2:0]			HW_GAIN[2:0]			
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function	
7	HSIG	This is the Ranging bit for the A/D. Normal gain at 0 and High range (sensitivity is divided by 14.5) when set to 1.	
6:4	SW_GAIN[2:0]	Causes an internal accumulation of samples with no pause between readings when in FORCED Mode. In Autonomous mode the the accumulation happens at the measurement rate selected. The calculations are accumulated in 24 bits and an optional shift is applied later. See ADC-POSTx.ADC_MISC[1:0]	
		Value	Number of Measurements
		0	1
		1	2
		2	4
		3	8
		4	16
		5	32
		6	64
		7	128
3:0	HW_GAIN[3:0]	Value	Nominal Measurement time for 512 clocks
		0	24.4 µs
		1	48.8 µs
		2	97.5 µs
		……	……
		10	25 ms
		11	50 ms
		12 to 15	unused

7.2.3 ADCPOSTx

Parameter Addresses: 0x04, 0x08, 0x0C, 0x10, 0x14, 0x18								
Bit	7	6	5	4	3	2	1	0
Name	Reserved	24BIT_OUT	POSTSHIFT[2:0]			UNUSED	THRESH_EN[1:0]	
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function		
7	RESERVED	Must be set to 0		
6	24BIT_OUT	Determines the size of the fields in the output registers.		
		Value	Bits/Result	Output
		0	16	Unsigned integer
		1	24	Signed Integer
5:3	POSTSHIFT[2:0]	The number of bits to shift right after SW accumulation. Allows the results of many additions not to overflow the output. Especially useful when the output is in 16 bit mode.		
2	UNUSED			
1:0	THRESH_EN [1:0]	Value	Operation	
		0	Do not use THRESHOLDs	
		1	Interrupt when the measurement is larger than the THRESHOLD0 Global Parameters	
		2	Interrupt when the measurement is larger than the THRESHOLD1 Global Parameters	
		3	Interrupt when the measurement is larger than the THRESHOLD2 Global Parameters	

7.2.4 MEASCONFIGx

Parameter Addresses: 0x05, 0x0A, 0x0D, 0x11, 0x15, 0x19								
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	COUNTER_INDEX[1:0]		RSRVD[5:0]					
Reset	0	0	0	0	0	0	0	0

Bit	Name	Function	
7:6	COUNTER_INDEX[1:0]	Selects which of the three counters (MEASCOUNTx) in the global parameter list is in use by this channel. These counters control the period/frequency of measurements. When the channel uses the COUNTER_INDEX[1:0] to select a MEASCOUNT**k** register in the parameter table, then the time between measurements for this channel is = 800 us * MEASRATE * MEASCOUNT**k**. A value of zero in MEASRATE will prevent autonomous mode from working. Similarly a zero in MEASCOUNT**k** will prevent the autonomous mode from working for the concerned channel	
		Value	**Results**
		0	No counter selected so this measurement will not be performed unless BURST or Forced measurements.
		1	Selects MEASCOUNT1
		2	Selects MEASCOUNT2
		3	Selects MEASCOUNT3
5:0	RESERVED[5:0]	Reserved	

7.3 Photodiode Selection

The ADCCONFIGx.ADCMUX [4:0] Register controls the photodiode selection. See section 7.2.1 ADCCONFIGx.

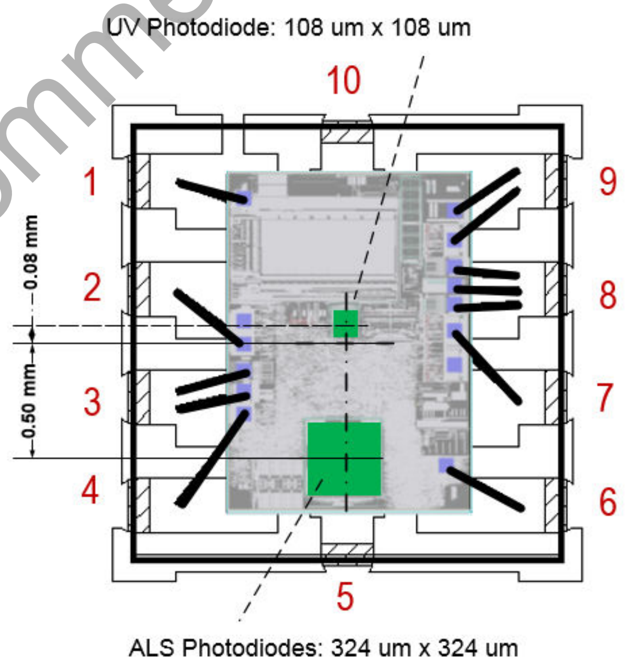


Figure 7.2. Photodiode Locations

8. Electrical Specifications

Table 8.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V_{DD} Supply Voltage	V_{DD}		1.62	—	3.6	V
V_{DD} OFF Supply Voltage	V_{DD_OFF}	OFF mode	–0.3	—	1.0	V
V_{DD} Supply Ripple Voltage		V_{DD} = 3.3 V 1 kHz–10 MHz	—	—	50	mVpp
Operating Temperature	T		–40	25	85	°C
SCL, SDA, Input High Logic Voltage	I^2C_{VIH}		V_{DD} x 0.7	—	V_{DD}	V
SCL, SDA Input Low Logic Voltage	I^2C_{VIL}		0	—	V_{DD} x 0.3	V
Start-Up Time		V_{DD} above 1.62 V	25	—	—	ms

Table 8.2. Performance Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I_{DD} Standby Mode (Sleep)	I_{sb}	No ADC Conversions No I^2C Activity; V_{DD} = 1.8 V	—	125	—	nA
	I_{sb}	No ADC Conversions No I^2C Activity; V_{DD} = 3.3 V	—	125	—	nA
I_{DD} Suspend Mode	I_{sus}	Autonomous Operation (RTC On) ADC conversion in Progress No I^2C Activity; V_{DD} = 1.8 V	—	0.550	—	µA
	I_{sus}	Autonomous Operation (RTC On) ADC conversion in Progress No I^2C Activity; V_{DD} = 3.3 V	—	0.525	—	µA
I active not measuring but active	I_{active}	Responding to commands and preparing and calculating results of readings; V_{DD} = 1.8 V	—	4.25	—	mA
	I_{active}	Responding to commands and preparing and calculating results of readings; V_{DD} = 3.3 V	—	4.5	—	mA
INT, SCL, SDA Leakage Current		V_{DD} = 3.3 V	–1	—	1	µA
Processing Time per Measurement (During this time the current is I Active)	$t_{process}$	UV or ALS	—	155	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
A/D Startup Time per Measurement (During this time the current is I Suspend)	$t_{adstart}$	UV or ALS	—	48.8	—	µs
White minus Dark Shallow Photodiode Response ADCMUX = 11 DECIM = 0 ADC_RANGE = 0 HSIG = 0		460 nm (blue) 525 nm (green) 625 nm (red) 850 nm (IR) 940 nm (IR)	— — — — —	190 160 100 30 10	— — — — —	ADC Counts / (W/m^2)
Dual White minus Dual Dark Photodiode Response ADCMUX = 13 DECIM = 0 ADC_GAIN = 0 HSIG = 0		460 nm (blue) 525 nm (green) 625 nm (red) 850 nm (IR) 940 nm (IR)	— — — — —	380 320 200 60 20	— — — — —	ADC Counts / (W/m^2)
Deep minus Dark Photodiode Response ADCMUX = 0 DECIM = 0 ADC_GAIN = 0 HSIG = 0		460 nm (blue) 525 nm (green) 625 nm (red) 850 nm (IR) 940 nm (IR)	— — — — —	90 260 510 690 490	— — — — —	ADC Counts / (W/m^2)
Dual Deep Photodiode minus Dual Dark Photodiode Response ADCMUX = 1 DECIM = 0 ADC_GAIN = 0 HSIG = 0		460 nm (blue) 525 nm (green) 625 nm (red) 850 nm (IR) 940 nm (IR)	— — — — —	190 520 1000 1280 860	— — — — —	ADC Counts / (W/m^2)
UV Photodiode Response ADCMUX = 24 DECIM = 0 ADC_GAIN = 11 HSIG = 0		310 nm	—	1740	—	ADC Counts / (W/m^2)
Ratio of readings with HSIG = 0 and HSIG = 1 for the shallow PD		525 nm, Internal ADCMUX = 11; ADC_GAIN = 0	—	15.2	—	Units

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ratio of readings with HSIG = 0 and HSIG = 1 for the deep PD		940 nm ADCMUX = 0; ADC_GAIN = 0	—	15.2	—	Units
SCL, SDA VOL			—	—	V_{DD} x 0.2	V
INT VOL			—	—	0.4	V

Note:
1. Unless specifically stated in "Conditions", electrical data assumes ambient light levels < 1 klx.
2. Guaranteed by design and characterization.

Table 8.3. I^{2}C Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Clock Frequency	f_{SCL}	—	—	400	kHz
Clock Pulse Width Low	t_{LOW}	1.3	—	—	µs
Clock Pulse Width High	t_{HIGH}	0.6	—	—	µs
Rise Time	t_R	20	—	300	ns
Fall Time	t_F	20 x (V_{DD} / 5.5)	—	300	ns
Start Condition Hold Time	$t_{HD.STA}$	0.6	—	—	µs
Start Condition Setup Time	$t_{SU.STA}$	0.6	—	—	µs
Input Data Setup Time	$t_{SU.DAT}$	100	—	—	ns
Data Hold Time	$t_{HD.DAT}$	0	—	—	ns
Output Data Valid Time	$t_{VD.DAT}$	—	—	0.9	µs
Stop Setup Time	$t_{SU.STO}$	0.6	—	—	µs
Bus Free Time	t_{BUF}	1.3	—	—	µs
Supressed Pulse Width	t_{SP}	—	—	40	ns
Bus Capacitance	C_b	—	—	400	pF

Table 8.4. Absolute Maximum Ratings

Parameter	Test Condition	Min	Max	Unit
V_{DD} Supply Voltage		–0.3	4	V
Operating Temperature		–40	85	°C
Storage Temperature		–65	85	°C
INT, SCL, SDA Voltage	V_{DD} = 0 V, T_A < 85 °C	–0.5	3.6	V
ESD Rating	Human Body Model	—	2	kV
	Machine Model	—	225	V
	Charged-Device Model	—	2	kV

9. Pin Descriptions

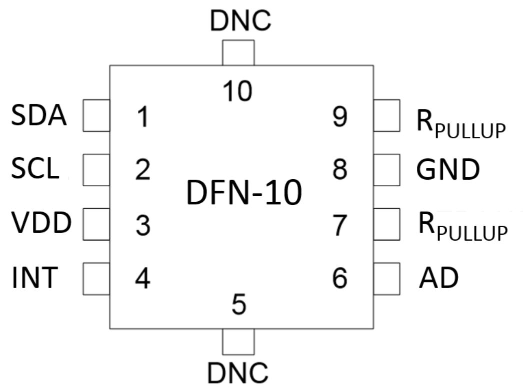


Figure 9.1. 10-Pin DFN

Table 9.1. Pin Descriptions

Pin	Name	Type	Description
1	SDA	Bidirectional	I^2C Data.
2	SCL	Input	I^2C Clock.
3	VDD	Power	Power Supply. Voltage source.
4	INT	Bidirectional	Interrupt Output. Open-drain interrupt output pin. Must be at logic level high during power-up sequence to enable low power operation.
5	DNC		Do Not Connect. This pin is electrically connected to an internal Si1133 node. It should remain unconnected.
6	AD	Input	I^2C Address Select. It is sensed during startup. Pull up to VDD with 47 k Resistor for default I^2C address (0x55). Pull down with 47 k Resistor to select alternate I^2C address (0x52).
7	RPullup	Input	Resistor Pullup. Always connect to V_{DD} through a pull-up resistor.
8	GND	Power	Ground. Reference voltage.
9	RPullup	Input	Resistor Pull-up. Connect to V_{DD} through a pull-up resistor when not in use.
10	DNC		Do Not Connect. This pin is electrically connected to an internal Si1133 node. It should remain unconnected.

10. 10-Pin 2x2 mm DFN Module Outline

DFN Package Diagram Dimensions illustrates the package details for the Si1133 DFN package lists the values for the dimensions shown in the illustration.

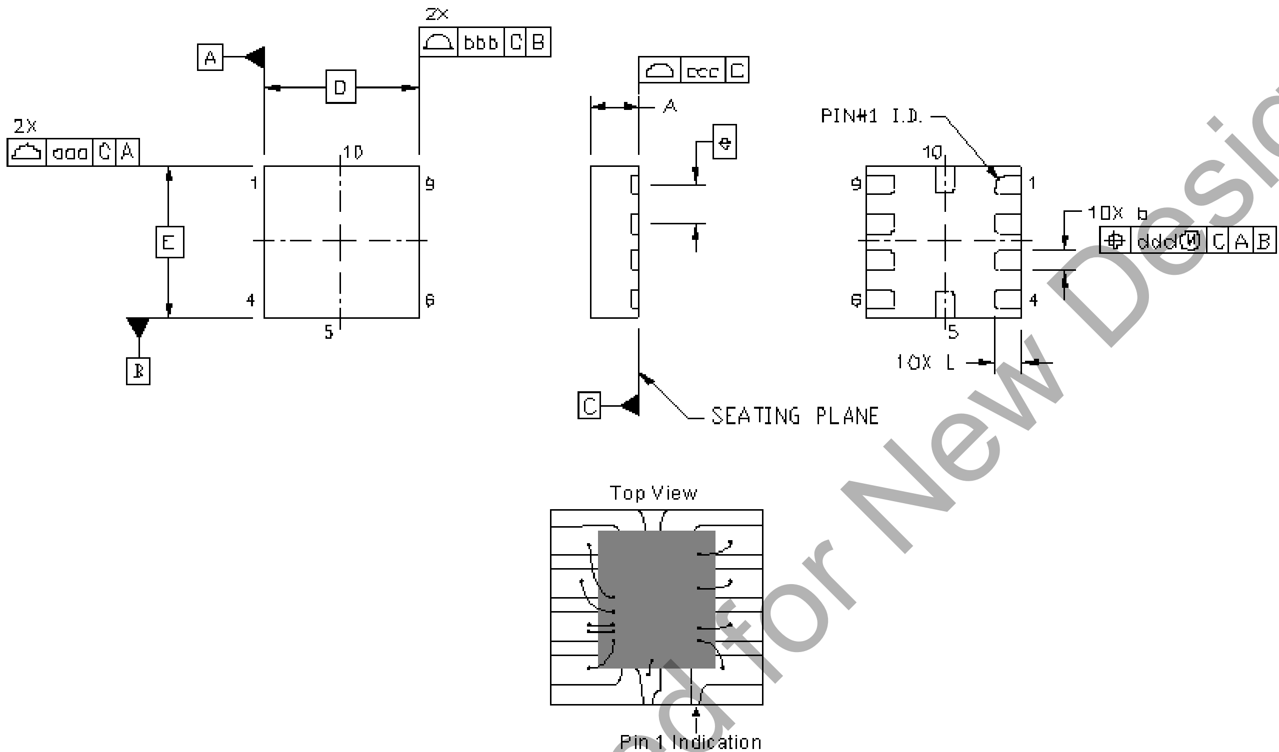


Figure 10.1. DFN Package Diagram Dimensions

Table 10.1. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.55	0.65	0.75
b	0.20	0.25	0.30
D		2.00 BSC.	
e		0.50 BSC.	
E		2.00 BSC.	
L	0.30	0.35	0.40
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	

Notes:
1. All dimensions shown are in millimeters (mm).
2. Dimensioning and Tolerance per ANSI Y14.5M-1994.

11. 2x2 mm DFN Land Pattern

See the figure and table below for the suggested 2 x 2 mm DFN PCB land pattern.

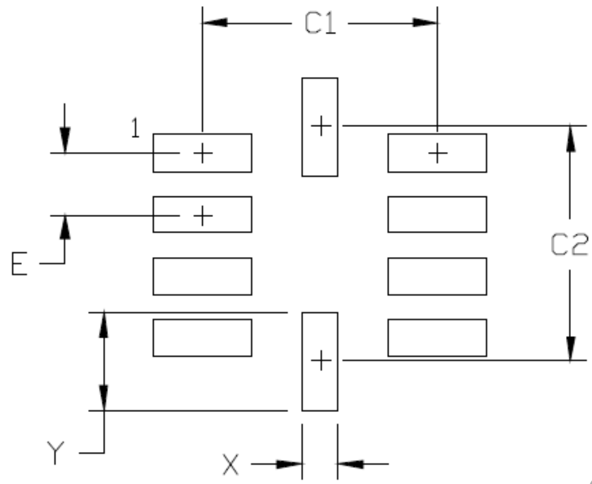


Figure 11.1. 2 x 2 mm DFN PCB Land Pattern

Table 11.1. Land Pattern Dimensions

Dimension	mm
C1	1.90
C2	1.90
E	0.50
X	0.30
Y	0.80

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 mm minimum, all the way around the pad.

Stencil Design

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for all pads.

Card Assembly

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

12. Revision History

12.1 Revision 0.9

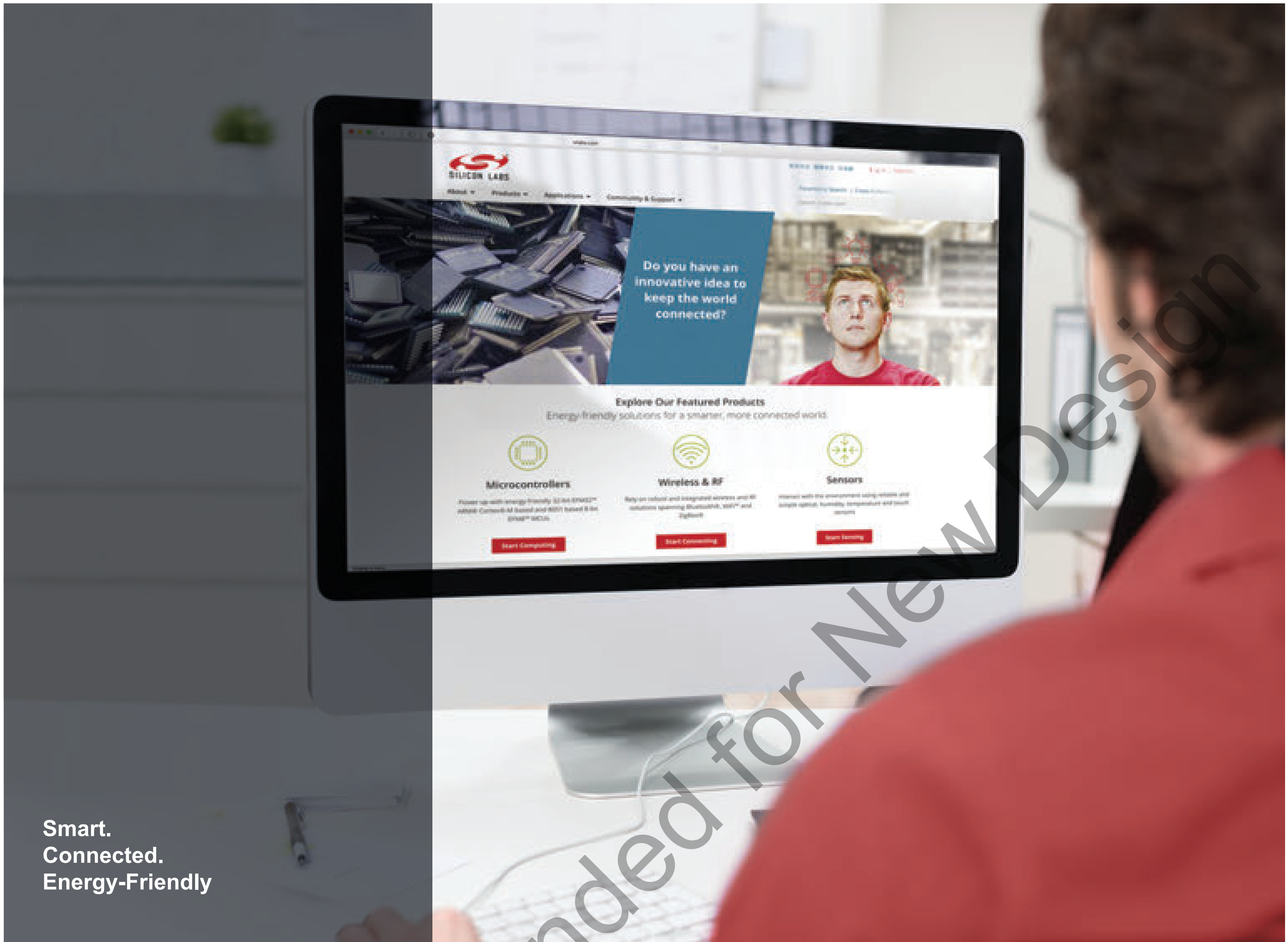
December 4th, 2015

- Initial release.

12.2 Revision 0.91

February 11, 2016

- Corrected the value of I^2C addresses to 0x55 and 0x52.
- Corrected Device ID value to 0x33.



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