SL28PCIe10

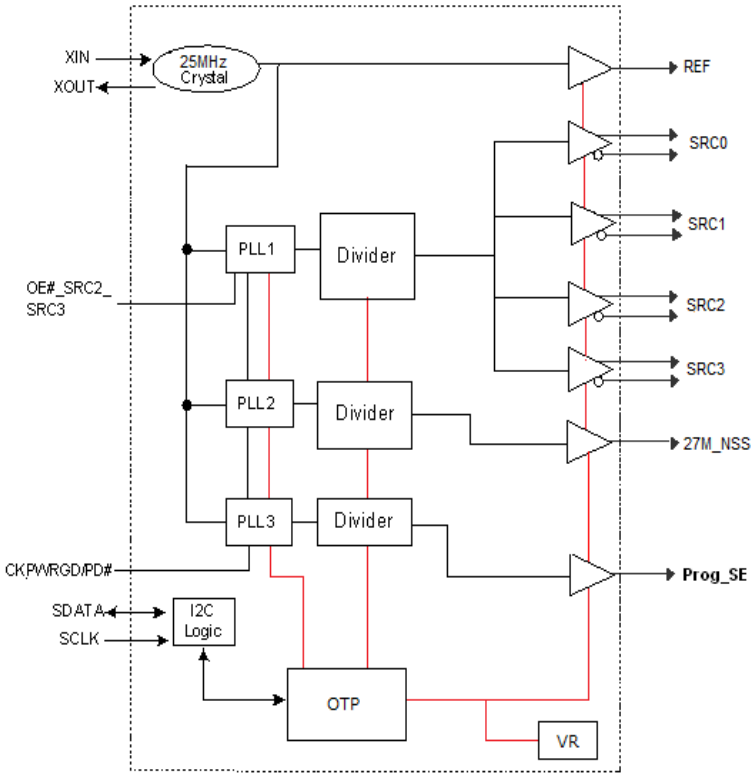
EProClock®PCI-Express Gen 2 Clock Generator

Features

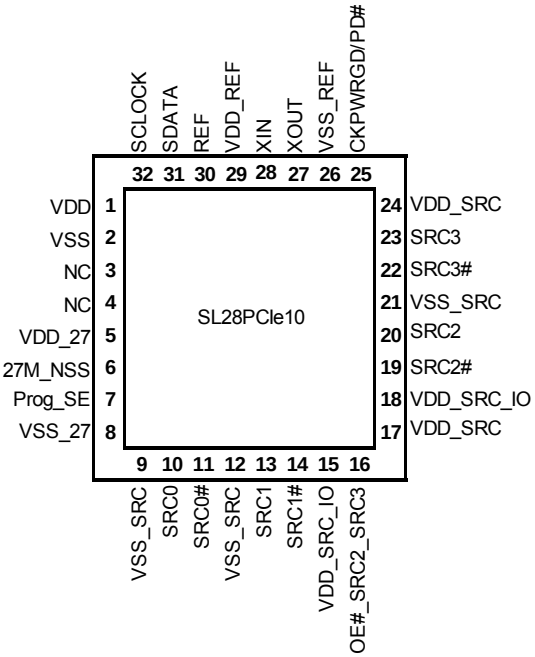
- One Programmable Spreadable Single-ended Clock
- PCI-Express Gen 2 Compliant
- Low power push-pull type differential output buffers
- Integrated voltage regulator
- Integrated resistors on differential clocks
- Scalable low voltage VDD_IO (3.3V to 1.05V)
- Wireless friendly 3-bits slew rate control on single-ended clocks.
- Four 100MHz Differential clocks
- 27MHz Video clock
- Buffered Reference Clock 25MHz
- EProClock® Programmable Technology
- I^2C support with readback capabilities
- Triangular Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial Temperature -40°C to 85°C
- 3.3V Power supply
- 32-pin QFN package

100Mhz	48M	REF	27M	Programmable Single-ended Clock
x4	x1	x1	x1	x1

Block Diagram



Pin Configuration



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32-QFN Pin Definitions

Pin No.	Name	Type	Description
1	VDD	PWR	3.3V Power supply
2	VSS	GND	Ground
3	NC	NC	No Connect.
4	NC	NC	No Connect.
5	VDD_27	PWR	3.3V Power supply
6	27M_NSS	O,SE	Non-spread 27MHz video clock output
7	Prog_SE	O, SE	Spreadable Programmable Single-Ended clock output
8	VSS_27	GND	Ground
9	VSS_SRC	GND	Ground
10	SRC0	O, DIF	100MHz True differential serial reference clock
11	SRC0#	O, DIF	100MHz Complement differential serial reference clock
12	VSS_SRC	GND	Ground
13	SRC1	O, DIF	100MHz True differential serial reference clock
14	SRC1#	O, DIF	100MHz Complement differential serial reference clock
15	VDD_SRC_IO	PWR	Scalable 3.3V to 1.05V power supply for output buffer
16	OE#_SRC2_SRC3	I	3.3V tolerance input to disable Output on Pin 7 and Pin 8
17	VDD_SRC	PWR	3.3V Power supply
18	VDD_SRC_IO	PWR	Scalable 3.3V to 1.05V power supply for output buffer
19	SRC2#	O, DIF	100MHz True differential serial reference clock
20	SRC2	O, DIF	100MHz Complement differential serial reference clock
21	VSS_SRC	GND	Ground
22	SRC3#	O, DIF	100MHz True differential serial reference clock
23	SRC3	O, DIF	100MHz Complement differential serial reference clock
24	VDD_SRC	PWR	3.3V Power supply
25	CK_PWRGD/PD#	I	3.3V LVTTL input. After CK_PWRGD (active HIGH) assertion, this pin becomes a real-time input for asserting power down (active LOW)
26	VSS_REF	GND	Ground
27	XOUT	O, SE	25MHz Crystal output
28	XIN	I	25MHz Crystal input
29	VDD_REF	PWR	3.3V Power supply for outputs and also maintains SMBUS registers during power-down
30	REF	PD, I/O	Reference 25MHz clock output
31	SDATA	I/O	SMBus compatible SDATA
32	SCLK	I	SMBus compatible SCLOCK

Programmable Single ended clock

SL28PCIe10 allows flexibility of programming any frequency at single ended output Prog_SE.

Prog_SE can be factory programmed to any frequency as required by the end user with a 3.3V swing single ended output. This clock can have a feature of Spread Spectrum to reduce EMI.

EProClock® Programmable Technology

EProClock® is the world's first non-volatile programmable clock. The EProClock® technology allows board designer to promptly achieve optimum compliance and clock signal integrity; historically, attainable typically through device and/or board redesigns.

EProClock® technology can be configured through SMBus or hard coded.

Features:

- > 4000 bits of configurations
- Can be configured through SMBus or hard coded
- Custom frequency sets
- Differential skew control on true or compliment or both
- Differential duty cycle control on true or compliment or both
- Differential amplitude control
- Differential and single-ended slew rate control
- Program Internal or External series resistor on single-ended clocks
- Program different spread profiles
- Program different spread modulation rate

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge

Table 2. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
		....	Stop

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	HW	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	PD_Restore	Save configuration when PD# is asserted 0 = Config. cleared, 1 = Config. saved

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	PLL1_SS_DC	Select for down or center SS 0 = Down spread, 1 = Center spread
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	1	REF_OE	Output enable for REF 0 = Output Disabled, 1 = Output Enabled
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED

Byte 3: Control Register 3

0	1	RESERVED	RESERVED

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	1	SRC0_OE	Output enable for SRC0 0 = Output Disabled, 1 = Output Enabled
5	1	SRC1_OE	Output enable for SRC1 0 = Output Disabled, 1 = Output Enabled
4	1	RESERVED	RESERVED
3	1	SRC3_OE	Output enable for SRC3 0 = Output Disabled, 1 = Output Enabled
2	1	SRC2_OE	Output enable for SRC2 0 = Output Disabled, 1 = Output Enabled
1	1	PLL1_SS_EN	Enable PLL1s spread modulation, 0 = Spread Disabled, 1 = Spread Enabled
0	1	RESERVED	RESERVED

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	REF Bit1	REF slew rate control *(see Byte 13 for Slew Rate Bit 0 and Bit 2)* 0 = High, 1 = Low
4	0	RESERVED	RESERVED
3	0	27MHz Bit 1	27MHz slew rate control *(see Byte 13 for Slew Rate Bit 0 and Bit 2)* 0 = High, 1 = Low
2	0	RESERVED	RESERVED
1	0	RESERVED	RESERVED
0	0	RESERVED	RESERVED

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Rev Code Bit 3	Revision Code Bit 3
6	1	Rev Code Bit 2	Revision Code Bit 2

Byte 7: Vendor ID

5	0	Rev Code Bit 1	Revision Code Bit 1
4	0	Rev Code Bit 0	Revision Code Bit 0
3	1	Vendor ID bit 3	Vendor ID Bit 3
2	0	Vendor ID bit 2	Vendor ID Bit 2
1	0	Vendor ID bit 1	Vendor ID Bit 1
0	0	Vendor ID bit 0	Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	1	Device_ID3	RESERVED
6	0	Device_ID2	RESERVED
5	0	Device_ID1	RESERVED
4	0	Device_ID0	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED
1	1	27M_non-SS_OE	Output enable for 27M_non-SS 0 = Output Disabled, 1 = Output Enabled
0	1	Prog_SE_OE	Output enable for Prog_SE 0 = Output Disabled, 1 = Output Enabled

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	TEST _MODE_SEL	Test mode select either REF/N or tri-state 0 = All outputs tri-state, 1 = All output REF/N
3	0	TEST_MODE_ENTRY	Allows entry into test mode 0 = Normal Operation, 1 = Enter test mode(s)
2	1	I2C_VOUT<2>	Amplitude configurations differential clocks I2C_VOUT[2:0] 000 = 0.30V 001 = 0.40V 010 = 0.50V 011 = 0.60V 100 = 0.70V 101 = 0.80V (default) 110 = 0.90V 111 = 1.00V
1	0	I2C_VOUT<1>	
0	1	I2C_VOUT<0>	

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	0	RESERVED	RESERVED

Byte 10: Control Register 10 (continued)

Bit	@Pup	Name	Description
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	RESERVED	RESERVED
0	1	RESERVED	RESERVED

Byte 12: Byte Count

Bit	@Pup	Name	Description
7	0	BC7	Byte count register for block read operation. The default value for Byte count is 15. In order to read beyond Byte 15, the user should change the byte count limit.to or beyond the byte that is desired to be read.
6	0	BC6	
5	0	BC5	
4	0	BC4	
3	1	BC3	
2	1	BC2	
1	1	BC1	
0	1	BC0	

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	1	REF_Bit2	Drive Strength Control - Bit[2:0], *Note: See Byte 6 Bit 5 for REF Slew Rate Bit 1 and Byte 6 Bit 3 for 27MHz Slew Rate Bit 1* Normal mode default '101' Wireless Friendly Mode default to '111'
6	1	REF_Bit0	
5	1	27MHz_NSS_Bit2	
4	1	27MHz_NSS_Bit0	
3	1	Prog_SE_Bit2	
2	1	Prog_SE_Bit0	
1	0	RESERVED	RESERVED
0	0	Wireless Friendly mode	Wireless Friendly Mode 0 = Disabled, Default all single-ended clocks slew rate config bits to '101' 1 = Enabled, Default all single-ended clocks slew rate config bits to '111'

Mode	Bit2	Bit1	Bit0	Buffer Strength
	0	0	0	Strong
	0	0	1	
	0	1	0	
	0	1	1	
	1	0	0	
Default	1	0	1	
	1	1	0	
Wireless Friendly	1	1	1	Weak

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	1	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	0	OTP_4	OTP_ID Identification for programmed device
3	0	OTP_3	
2	0	OTP_2	
1	0	OTP_1	
0	0	OTP_0	

Table 4. Output Driver Status during OE#_SRC2_SRC3

		OE#_SRC2_SRC3 Asserted	SMBus OE Disabled
Single-ended Clocks	Stoppable	Running	Driven low
	Non stoppable	Running	
Differential Clocks	Stoppable	Clock driven high	Clock driven low
		Clock# driven low	
	Non stoppable	Running	

Table 5. Output Driver Status

	All Single-ended Clocks		All Differential Clocks	
	w/o Strap	w/ Strap	Clock	Clock#
PD# = 0 (Power down)	Low	Hi-z	Low	Low

PD# (Power down) Clarification

The CK_PWRGD/PD# pin is a dual-function pin. During initial power up, the pin functions as CK_PWRGD. Once CK_PWRGD has been sampled HIGH by the clock chip, the pin assumes PD# functionality. The PD# pin is an asynchronous active LOW input used to shut off all clocks cleanly before shutting off power to the device. This signal is synchronized internally to the device before powering down the clock synthesizer. PD# is also an asynchronous input for powering up the system. When PD# is asserted LOW, clocks are driven to a LOW value and held before turning off the VCOs and the crystal oscillator.

PD# Assertion

When PD# has been sampled LOW by the internal reference clock all differential clocks will be stopped in a glitch free manner to the LOW/LOW state within their next two consecutive rising edges.

When PD# is sampled LOW by two consecutive cycles of an internal reference clock, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition.

PD# Deassertion

Power up latency will be less than 2ms for crystal input reference clock and less than 8ms for differential input reference clock. This is the delay from the power supply reaching the min value specified in the datasheet, until the time that the part is ready to sample any latched inputs on the first rising edge of CKPWRGD.

After the first rising edge on CKPWRGD this pin becomes PD#. After a valid rising edge on CKPWRGD/PD# pin, a time of not more than 1.8ms is allowed for the clock chip's internal PLL's to power up and lock, after this time all outputs are enabled in a glitch free manner within a few clock cycles of each clock.

OE#_SRC2_SRC3 Assertion

The OE#_SRC2_SRC3 signal is an active LOW input used for synchronous stopping and starting the SRC2 and SRC3 output clocks while the rest of the clock generator continues to function. When the OE#_SRC2_SRC3 pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable are stopped cleanly. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW.

OE#_SRC2_SRC3 Deassertion

The deassertion of the OE#_SRC2_SRC3 signal causes all stopped SRC2 AND SRC3 outputs to resume normal operation in a synchronous manner. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the deassertion to active outputs is no more than two SRC clock cycles.

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
$V_{DD\_3.3V}$	Main Supply Voltage		–	4.6	V
V_{DD_IO}	IO Supply Voltage			4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	4.6	V_{DC}
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	-40	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	MIL-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD core	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{IH}	3.3V Input High Voltage (SE)		2.0	V_{DD} + 0.3	V
V_{IL}	3.3V Input Low Voltage (SE)		V_{SS} – 0.3	0.8	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IH_FS}	FS Input High Voltage		0.7	VDD+0.3	V
V_{IL_FS}	FS Input Low Voltage		V_{SS} – 0.3	0.35	V
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	–	5	µA
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	–	µA
V_{OH}	3.3V Output High Voltage (SE)	I_{OH} = –1 mA	2.4	–	V
V_{OL}	3.3V Output Low Voltage (SE)	I_{OL} = 1 mA	–	0.4	V
$V_{DD\ IO}$	Low Voltage IO Supply Voltage		1	3.465	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		1.5	5	pF
C_{OUT}	Output Pin Capacitance			6	pF
L_{IN}	Pin Inductance		–	7	nH
IDD_PD	Power Down Current		–	1	mA
$I_{DD\_3.3V}$	Dynamic Supply Current	All outputs enabled. SE clocks with 8” traces and 4pF load. Differential clocks with 7” traces and 2pF load.	–	65	mA
$I_{DD\_VDD\_IO}$	Dynamic Supply Current	All outputs enabled. SE clocks with 8” traces and 4pF load. Differential clocks with 7” traces and 2pF load.	–	25	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
L_{ACC}	Long-term Accuracy	Measured at VDD/2 differential	–	250	ppm
Clock Input					
T_{DC}	CLKIN Duty Cycle	Measured at VDD/2	47	53	%
T_R/T_F	CLKIN Rise and Fall Times	Measured between $0.2V_{DD}$ and $0.8V_{DD}$	0.5	4.0	V/ns
T_{CCJ}	CLKIN Cycle to Cycle Jitter	Measured at VDD/2	–	250	ps
T_{LTJ}	CLKIN Long Term Jitter	Measured at VDD/2	–	350	ps
V_{IH}	Input High Voltage	XIN / CLKIN pin	2	VDD+0.3	V
V_{IL}	Input Low Voltage	XIN / CLKIN pin	–	0.8	V
I_{IH}	Input High Current	XIN / CLKIN pin, VIN = VDD	–	35	uA
I_{IL}	Input Low Current	XIN / CLKIN pin, 0 < VIN <0.8	-35	–	uA
SRC at 0.7V					
T_{DC}	SRC Duty Cycle	Measured at 0V differential	45	55	%
T_{PERIOD}	100 MHz SRC Period	Measured at 0V differential at 0.1s	9.99900	10.0010	ns
$T_{PERIODSS}$	100 MHz SRC Period, SSC	Measured at 0V differential at 0.1s	10.02406	10.02607	ns
$T_{PERIODAbs}$	100 MHz SRC Absolute Period	Measured at 0V differential at 1 clock	9.87400	10.1260	ns
$T_{PERIODSSAbs}$	100 MHz SRC Absolute Period, SSC	Measured at 0V differential at 1 clock	9.87406	10.1762	ns
$T_{SKEW(window)}$	Any SRC Clock Skew from the earliest bank to the latest bank	Measured at 0V differential	–	3.0	ns
T_{CCJ}	SRC Cycle to Cycle Jitter	Measured at 0V differential	–	125	ps
RMS_{GEN1}	Output PCIe* Gen1 REFCLK phase jitter	BER = 1E-12 (including PLL BW 8 - 16 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz)	0	108	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.0	ps
RMS_{GEN2}	Output PCIe* Gen2 REFCLK phase jitter	Includes PLL BW 8 - 16 MHz, Jitter Peaking = 3dB, ζ = 0.54, Td=10 ns), Low Band, F < 1.5MHz	0	3.1	ps
L_{ACC}	SRC Long Term Accuracy	Measured at 0V differential	–	100	ppm
T_R / T_F	SRC Rising/Falling Slew Rate	Measured differentially from ±150 mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Measured single-endedly from ±75 mV	–	20	%
V_{HIGH}	Voltage High			1.15	V
V_{LOW}	Voltage Low		–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		300	550	mV
27M_NSS at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread 27M Period	Measurement at 1.5V	37.03594	37.03813	ns
T_R / T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	50	ppm
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{PERIOD}	REF Period	Measurement at 1.5V	39.996	40.004	ns
T_R / T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	50	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns

Test and Measurement Setup

For Reference Clock

The following diagram shows the test load configurations for the single-ended REF output signal.

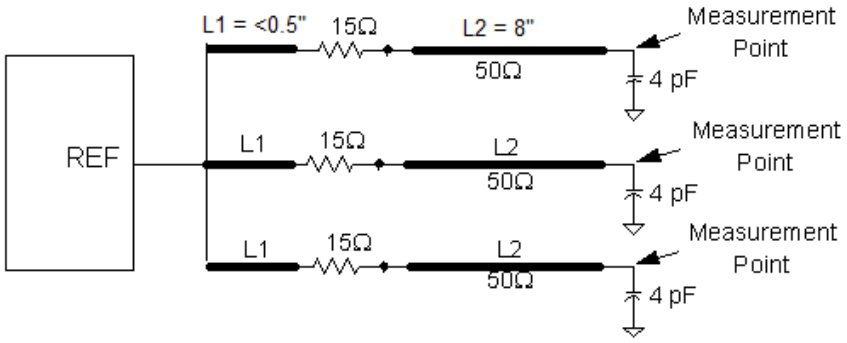


Figure 1. Single-ended REF Triple Load Configuration

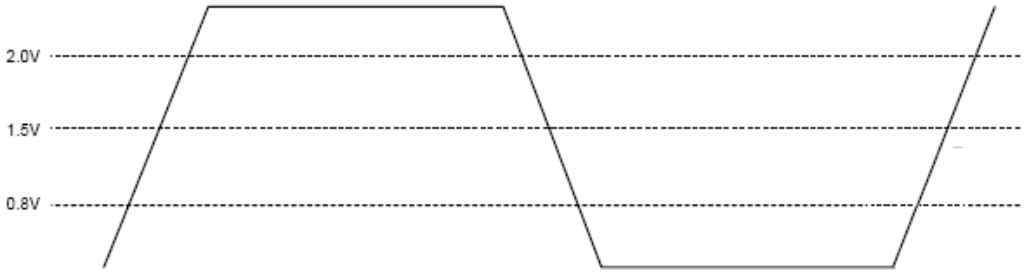


Figure 2. Single-ended Output Signals (for AC Parameters Measurement)

For Differential Clock Signals

This diagram shows the test load configuration for the differential clock signals

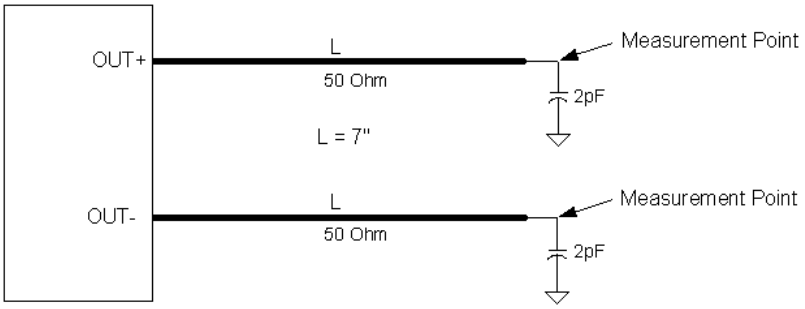


Figure 3. 0.7V Differential Load Configuration

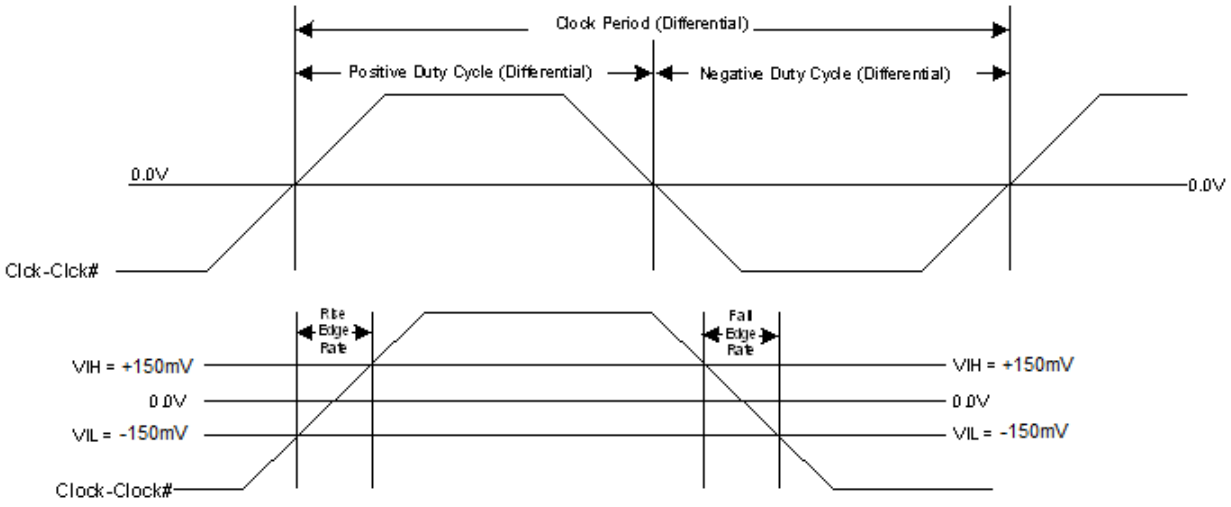


Figure 4. Differential Measurement for Differential Output Signals (for AC Parameters Measurement)

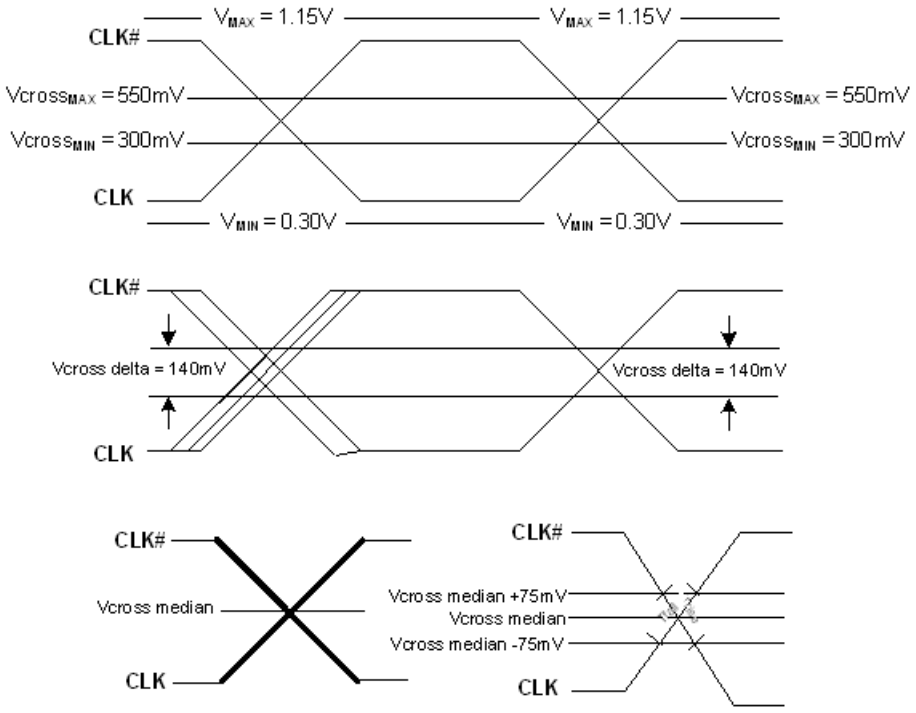
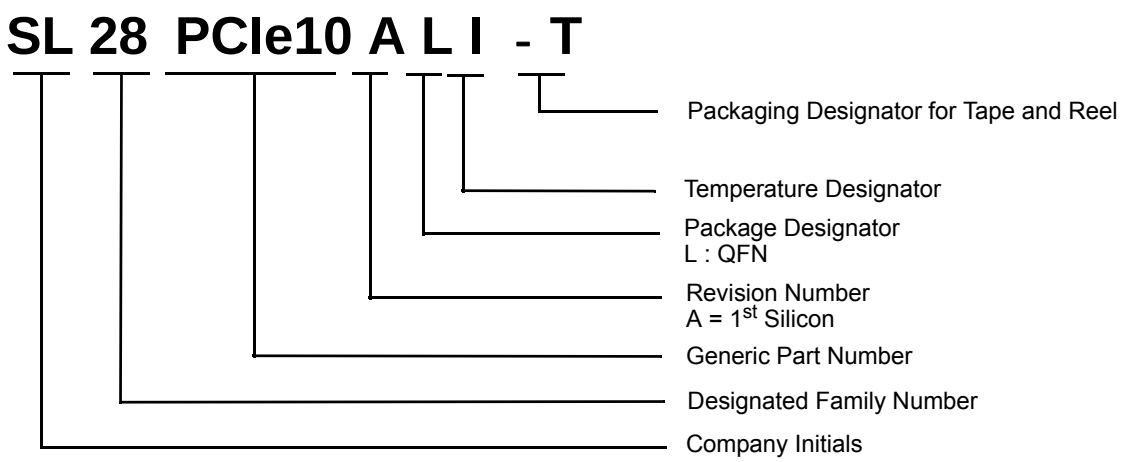


Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)

Ordering Information

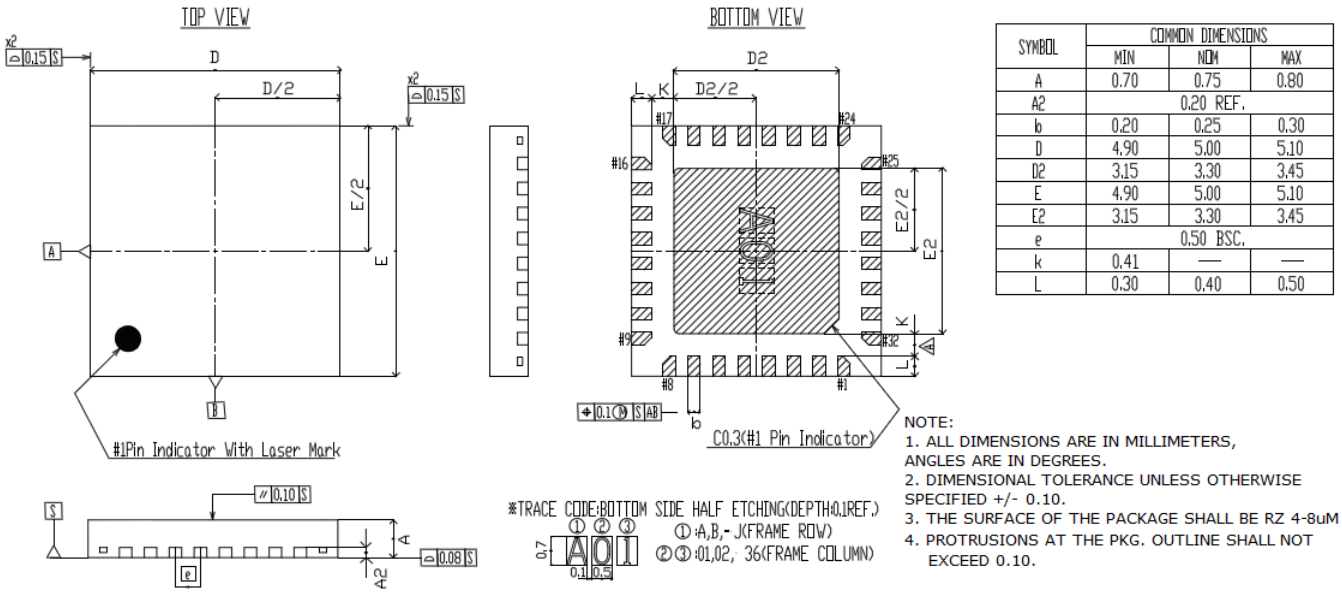
Part Number	Package Type	Product Flow
Lead-free		
SL28PCIe10ALI	32-pin QFN	Industrial, -40° to 85°C
SL28PCIe10ALIT	32-pin QFN–Tape and Reel	Industrial, -40° to 85°C
SL28PCIe10ALC	32-pin QFN	Commercial, 0° to 85°C
SL28PCIe10ALCT	32-pin QFN–Tape and Reel	Commercial, 0° to 85°C



This device is Pb free and RoHS compliant.

Package Diagrams

32-Lead QFN 5x 5mm (Saw Version)



SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A2		0.20 REF.	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.15	3.30	3.45
E	4.90	5.00	5.10
E2	3.15	3.30	3.45
e		0.50 BSC.	
k	0.41	—	—
L	0.30	0.40	0.50

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
2. DIMENSIONAL TOLERANCE UNLESS OTHERWISE SPECIFIED +/- 0.10.
3. THE SURFACE OF THE PACKAGE SHALL BE RZ 4-8uM
4. PROTRUSIONS AT THE PKG. OUTLINE SHALL NOT EXCEED 0.10.

Document History Page

Document Title: SL28PCIe10 PC EProClock®PCI-Express Gen 2 Clock Generator Document #: SP-AP-0212 (Rev. AA)			
REV.	**Issue Date**	**Orig. of Change**	**Description of Change**
1.0	10/15/10	TRP	Initial Release
AA	10/22/10	TRP	1. Updated miscellaneous text content 2. Updated absolute maximum value of VDD_IO
AA	12/2/10	TRP	1. Updated PD# Assertion, OE# _SRC2_SRC3 Assertion descriptions
AA	12/7/10	TRP	1. Added Crystal and Clock Input AC specifications 2. Removed redundant V_{IXH} and V_{IXL} from DC specifications
AA	12/15/10	TRP	1. Updated Power Down description

Mouser Electronics

Authorized Distributor

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