S-93C46B/56B/66B H Series

FOR AUTOMOTIVE 105°C OPERATION
3-WIRE SERIAL E^2PROM

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The S-93C46B/56B/66B H Series is a high temperature operation 3-wire serial E^2PROM for automotive components. The S-93C46B/56B/66B H Series has the capacity of 1 K-bit, 2 K-bit and 4 K-bit, and the organization is 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit. It is capable of sequential read, at which time addresses are automatically incremented in 16-bit blocks.
The communication method is by the Microwire bus.

■ Features

- Operating voltage range: Read 2.7 V to 5.5 V (Ta = −40°C to +105°C)
  Write 2.7 V to 5.5 V (Ta = −40°C to +105°C)
- Operation frequency: 1.0 MHz (V_{CC} = 4.5 V to 5.5 V, Ta = −40°C to +105°C)
- Write time: 8.0 ms max.
- Sequential read capable
- Write protect function during the low power supply voltage
- Function to protect against write due to erroneous instruction recognition
- Endurance: 10^6 cycles/word*1 (Ta = +85°C)
  5×10^5 cycles/word*1 (Ta = +105°C)
- Data retention: 100 years (Ta = +25°C)
  20 years (Ta = +105°C)
- Memory capacity: S-93C46B 1 K-bit
  S-93C56B 2 K-bit
  S-93C66B 4 K-bit
- Initial delivery state: FFFFh
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free*2
- AEC-Q100 qualified*3

***1.** For each address (Word: 16-bit)
***2.** Refer to "■ **Product Name Structure**" for details.
***3.** Contact our sales office for details.

■ Packages

- 8-Pin SOP (JEDEC)
- 8-Pin TSSOP
- TMSOP-8

Caution **Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

■ Pin Configurations

8-Pin SOP(JEDEC)
Top view

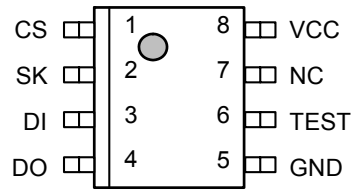


Figure 1

S-93C46BD0H-J8T2U
S-93C56BD0H-J8T2U
S-93C66BD0H-J8T2U

Table 1

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

8-Pin TSSOP
Top view

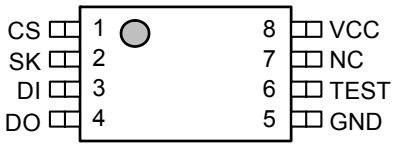


Figure 2

S-93C46BD0H-T8T2U
S-93C56BD0H-T8T2U
S-93C66BD0H-T8T2U

Table 2

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

TMSOP-8
Top view

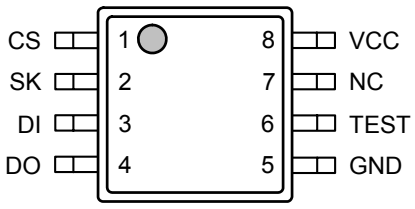


Figure 3

S-93C46BD0H-K8T2U
S-93C56BD0H-K8T2U
S-93C66BD0H-K8T2U

Table 3

Pin No.	Symbol	Description
1	CS	Chip select input
2	SK	Serial clock input
3	DI	Serial data input
4	DO	Serial data output
5	GND	Ground
6	TEST*1	Test
7	NC	No connection
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
Even if this pin is not connected, performance is not affected so long as the absolute maximum rating is not exceeded.

Remark See Dimensions for details of the package drawings.

■ Block Diagram

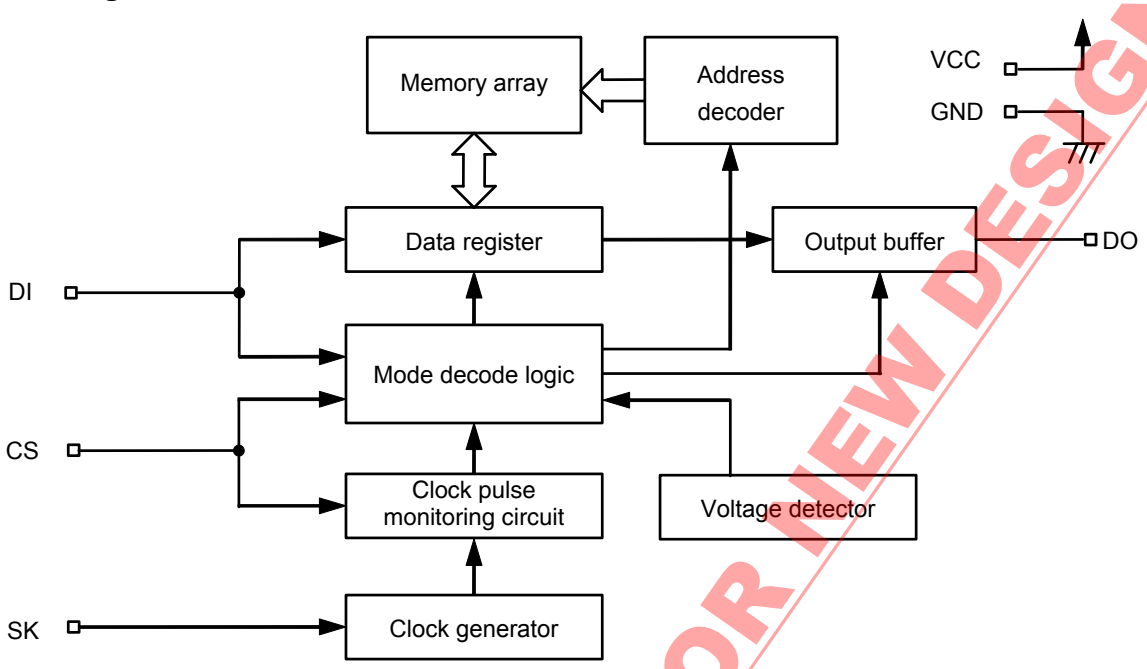


Figure 4

■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 2.
Contact our sales office for details of AEC-Q100 reliability specification.

■ Instruction Sets

1. S-93C46B

Table 4

Instruction	Start Bit	Operation Code		Address						Data
SK input clock	1	2	3	4	5	6	7	8	9	10 to 25
READ (Read data)	1	1	0	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

2. S-93C56B

Table 5

Instruction	Start Bit	Operation Code		Address								Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Read data)	1	1	0	x	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	x	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	x	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

3. S-93C66B

Table 6

Instruction	Start Bit	Operation Code		Address								Data
SK input clock	1	2	3	4	5	6	7	8	9	10	11	12 to 27
READ (Read data)	1	1	0	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Output*1
WRITE (Write data)	1	0	1	A7	A6	A5	A4	A3	A2	A1	A0	D15 to D0 Input
ERASE (Erase data)	1	1	1	A7	A6	A5	A4	A3	A2	A1	A0	—
WRAL (Write all)	1	0	0	0	1	x	x	x	x	x	x	D15 to D0 Input
ERAL (Erase all)	1	0	0	1	0	x	x	x	x	x	x	—
EWEN (Write enable)	1	0	0	1	1	x	x	x	x	x	x	—
EWDS (Write disable)	1	0	0	0	0	x	x	x	x	x	x	—

***1.** When the 16-bit data in the specified address has been output, the data in the next address is output.

Remark x: Don't care

■ Absolute Maximum Ratings

Table 7

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} +0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operating ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Recommended Operating Conditions

Table 8

Item	Symbol	Conditions	−40 to +85°C		+85 to +105°C		Unit
			Min.	Max.	Min.	Max.	
Power supply voltage	V_{CC}	READ, EWDS	1.8	5.5	2.7	5.5	V
		WRITE, ERASE, EWEN	2.7	5.5	2.7	5.5	V
		WRAL, ERAL	2.7	5.5	4.5	5.5	V
High level input voltage	V_{IH}	V_{CC} = 4.5 to 5.5 V	2.0	V_{CC}	2.0	V_{CC}	V
		V_{CC} = 2.7 to 4.5 V	0.8 × V_{CC}	V_{CC}	0.8 × V_{CC}	V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.8 × V_{CC}	V_{CC}	—	—	V
Low level input voltage	V_{IL}	V_{CC} = 4.5 to 5.5 V	0.0	0.8	0.0	0.8	V
		V_{CC} = 2.7 to 4.5 V	0.0	0.2 × V_{CC}	0.0	0.2 × V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.0	0.15 × V_{CC}	—	—	V

■ Pin Capacitance

Table 9

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Conditions	Min.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	—	8	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	—	10	pF

■ Endurance

Table 10

Item	Symbol	Operating Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^6	—	cycles/word*1
		+85 to +105°C	5×10^5	—	cycles/word*1

***1.** For each address (Word: 16 bits)

■ Data Retention

Table 11

Item	Symbol	Operating Ambient Temperature	Min.	Max.	Unit
Data Retention	—	+25°C	100	—	year
		−40 to +105°C	20	—	year

■ DC Electrical Characteristics

Table 12 (1/2)

Item	Symbol	Conditions	−40 to +85°C						Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	0.8	—	0.5	—	0.4	mA

Table 12 (2/2)

Item	Symbol	Conditions	+85 to +105°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	DO no load	—	0.8	—	0.5	mA

Table 13 (1/2)

Item	Symbol	Conditions	−40 to +85°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	2.0	—	1.5	mA

Table 13 (2/2)

Item	Symbol	Conditions	+85 to +105°C		Unit
			V_{CC} = 2.7 to 5.5 V		
			Min.	Max.	
Current consumption (WRITE)	I_{CC2}	DO no load	—	2.0	mA

Table 14 (1/2)

Item	Symbol	Conditions	−40 to +85°C						Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other inputs to V_{CC} or GND	—	1.5	—	1.5	—	1.5	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	—	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	—	—	—	V
		I_{OL} = 100 μA	—	0.1	—	0.1	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = −400 μA	2.4	—	—	—	—	—	V
		I_{OH} = −100 μA	V_{CC}− 0.3	—	V_{CC}− 0.3	—	—	—	V
		I_{OH} = −10 μA	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	—	1.5	—	1.5	—	V

Table 14 (2/2)

Item	Symbol	Conditions	+85 to +105°C				Unit
			V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	CS = GND, DO = Open, Other inputs to V_{CC} or GND	—	1.5	—	1.5	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	1.0	—	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	1.0	—	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA	—	0.4	—	—	V
		I_{OL} = 100 μA	—	0.1	—	0.1	V
High level output voltage	V_{OH}	I_{OH} = −400 μA	2.4	—	—	—	V
		I_{OH} = −100 μA	V_{CC}− 0.3	—	V_{CC}− 0.3	—	V
		I_{OH} = −10 μA	V_{CC}− 0.2	—	V_{CC}− 0.2	—	V
Data hold voltage of write enable latch	V_{DH}	Only program disable mode	1.5	—	1.5	—	V

■ AC Electrical Characteristics

Table 15 Measurement Conditions

Input pulse voltage	0.1 × V_{CC} to 0.9 × V_{CC}
Output reference voltage	0.5 × V_{CC}
Output load	100 pF

Table 16 (1/2)

Item	Symbol	−40 to +85°C						Unit
		V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.5 to 4.5 V		V_{CC} = 1.8 to 2.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
CS setup time	t_{CSS}	0.2	—	0.4	—	1.0	—	µs
CS hold time	t_{CSH}	0	—	0	—	0	—	µs
CS deselect time	t_{CDS}	0.2	—	0.2	—	0.4	—	µs
Data setup time	t_{DS}	0.1	—	0.2	—	0.4	—	µs
Data hold time	t_{DH}	0.1	—	0.2	—	0.4	—	µs
Output delay time	t_{PD}	—	0.4	—	0.8	—	2.0	µs
Clock frequency*1	f_{SK}	0	2.0	0	0.5	0	0.25	MHz
SK clock time “L” *1	t_{SKL}	0.1	—	0.5	—	1.0	—	µs
SK clock time “H” *1	t_{SKH}	0.1	—	0.5	—	1.0	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.15	0	0.5	0	1.0	µs
Output enable time	t_{SV}	0	0.15	0	0.5	0	1.0	µs

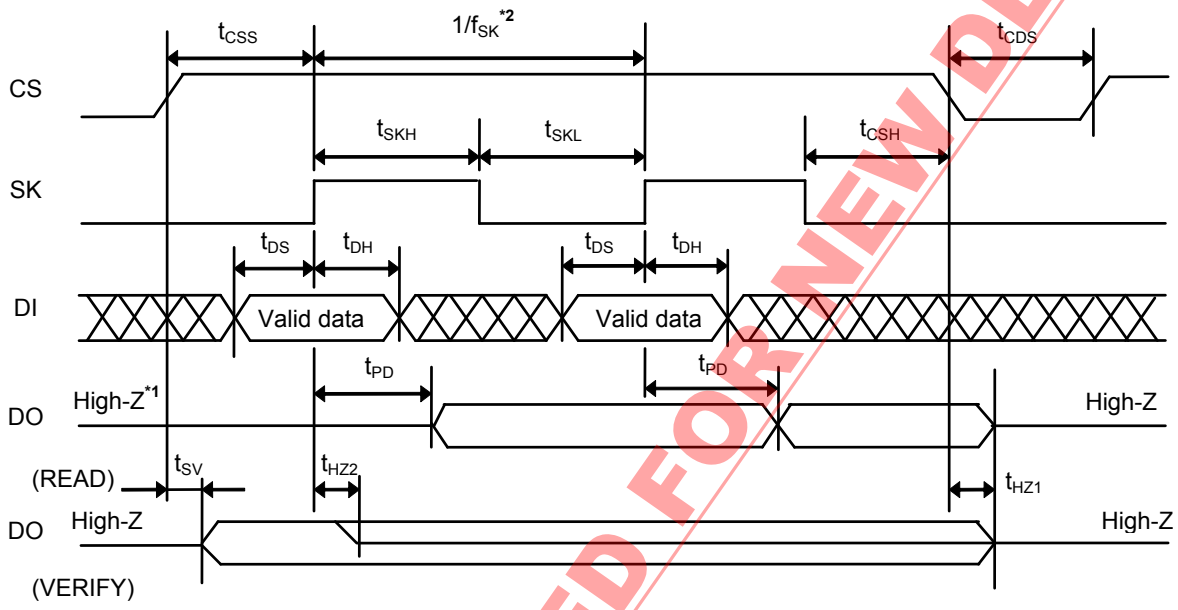
Table 16 (2/2)

Item	Symbol	+85 to +105°C				Unit
		V_{CC} = 4.5 to 5.5 V		V_{CC} = 2.7 to 4.5 V		
		Min.	Max.	Min.	Max.	
CS setup time	t_{CSS}	0.2	—	0.4	—	µs
CS hold time	t_{CSH}	0	—	0	—	µs
CS deselect time	t_{CDS}	0.2	—	0.2	—	µs
Data setup time	t_{DS}	0.1	—	0.2	—	µs
Data hold time	t_{DH}	0.1	—	0.2	—	µs
Output delay time	t_{PD}	—	0.6	—	0.8	µs
Clock frequency*1	f_{SK}	0	1.0	0	0.5	MHz
SK clock time “L” *1	t_{SKL}	0.25	—	0.5	—	µs
SK clock time “H” *1	t_{SKH}	0.25	—	0.5	—	µs
Output disable time	t_{HZ1}, t_{HZ2}	0	0.15	0	0.5	µs
Output enable time	t_{SV}	0	0.15	0	0.5	µs

***1.** The clock cycle of the SK clock (frequency: f_{SK}) is $1/f_{SK}$ µs. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made equal to t_{SKL}(Min.) + t_{SKH}(Min.).

Table 16

Item	Symbol	−40 to +85°C			+85 to +105°C			Unit
		V_{CC} = 2.7 to 5.5 V			V_{CC} = 2.7 to 5.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Write time	t_{PR}	—	4.0	8.0	—	4.0	8.0	ms



***1.** Indicates high impedance.

***2.** $1/f_{SK}$ is the SK clock cycle. This clock cycle is determined by a combination of several AC characteristics, so be aware that even if the SK clock cycle time is minimized, the clock cycle ($1/f_{SK}$) cannot be made equal to t_{SKL}(Min.) + t_{SKH}(Min.).

Figure 5 Timing Chart

■ Initial Delivery State

Initial delivery state of all addresses is "FFFFh".

■ Operation

All instructions are executed by inputting DI in synchronization with the rising edge of SK after CS goes high. An instruction set is input in the order of start bit, instruction, address, and data.
Instruction input finishes when CS goes low. A low level must be input to CS between commands during t_{CDS}. While a low level is being input to CS, the S-93C46B/56B/66B is in standby mode, so the SK and DI inputs are invalid and no instructions are allowed.

■ Start Bit

A start bit is recognized when the DI pin goes high at the rise of SK after CS goes high. After CS goes high, a start bit is not recognized even if the SK pulse is input as long as the DI pin is low.

1. Dummy clock

SK clocks input while the DI pin is low before a start bit is input are called dummy clocks. Dummy clocks are effective when aligning the number of instruction sets (clocks) sent by the CPU with those required for serial memory operation. For example, when a CPU instruction set is 16 bits, the number of instruction set clocks can be adjusted by inserting a 7-bit dummy clock for the S-93C46B and a 5-bit dummy clock for the S-93C56B/66B.

2. Start bit input failure

- When the output status of the DO pin is high during the verify period after a write operation, if a high level is input to the DI pin at the rising edge of SK, the S-93C46B/56B/66B recognizes that a start bit has been input. To prevent this failure, input a low level to the DI pin during the verify operation period (refer to "**4.1 Verify operation**").

- When a 3-wire interface is configured by connecting the DI input pin and DO output pin, a period in which the data output from the CPU and the serial memory collide may be generated, preventing successful input of the start bit. Take the measures described in "**■ 3-Wire Interface (Direct Connection between DI and DO)**".

3. Reading (READ)

The READ instruction reads data from a specified address.
After CS has gone high, input an instruction in the order of the start bit, read instruction, and address. Since the last input address (A_0) has been latched, the output status of the DO pin changes from high impedance (Hi-Z) to low, which is held until the next rise of SK. 16-bit data starts to be output in synchronization with the next rise of SK.

3. 1 Sequential read

After the 16-bit data at the specified address has been output, inputting SK while CS is high automatically increments the address, and causes the 16-bit data at the next address to be output sequentially. The above method makes it possible to read the data in the whole memory space. The last address (A_n ••• A_1 A_0 = 1 •• 1 1) rolls over to the top address (A_n ••• A_1 A_0 = 0 ••• 0 0).

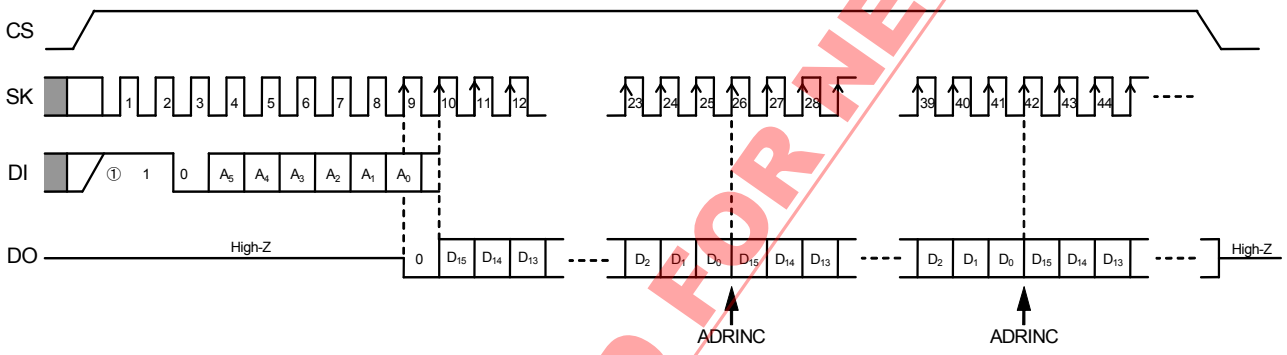


Figure 6 Read Timing (S-93C46B)

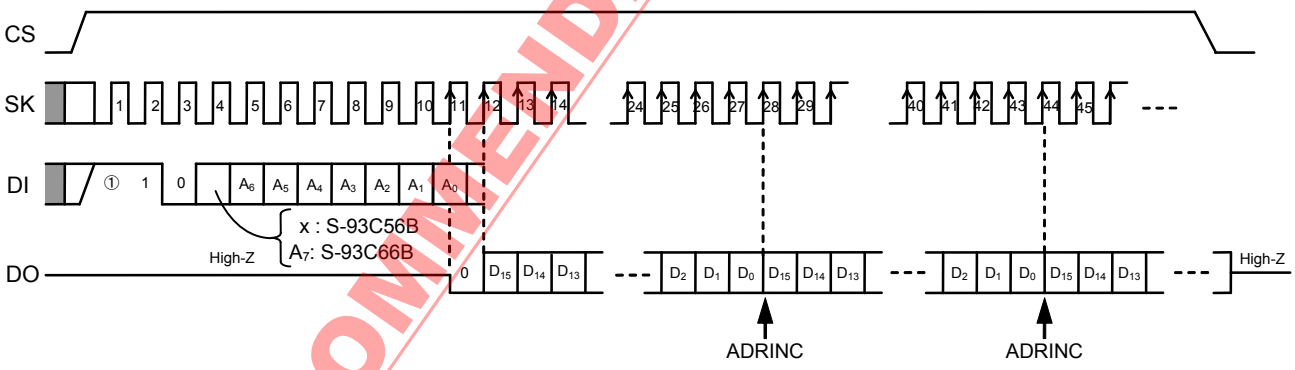


Figure 7 Read Timing (S-93C56B, S-93C66B)

4. Writing (WRITE, ERASE, WRAL, ERAL)

A write operation includes four write instructions: data write (WRITE), data erase (ERASE), chip write (WRAL), and chip erase (ERAL).
A write instruction (WRITE, ERASE, WRAL, ERAL) starts a write operation to the memory cell when a low level is input to CS after a specified number of clocks have been input. The SK and DI inputs are invalid during the write period, so do not input an instruction.
Input an instruction while the output status of the DO pin is high or high impedance (High-Z).
A write operation is valid only in program enable mode (refer to "**5. Write enable (EWEN) and write disable (EWDS)**").

4. 1 Verify operation

A write operation executed by any instruction is completed within 8 ms (write time t_{PR}: typically 4 ms), so if the completion of the write operation is recognized, the write cycle can be minimized. A sequential operation to confirm the status of a write operation is called a verify operation.

(1) Operation

After the write operation has started (CS = low), the status of the write operation can be verified by confirming the output status of the DO pin by inputting a high level to CS again. This sequence is called a verify operation, and the period that a high level is input to the CS pin after the write operation has started is called the verify operation period.
The relationship between the output status of the DO pin and the write operation during the verify operation period is as follows.

- DO pin = low: Writing in progress (busy)
- DO pin = high: Writing completed (ready)

(2) Operation example

There are two methods to perform a verify operation: Waiting for a change in the output status of the DO pin while keeping CS high, or suspending the verify operation (CS = low) once and then performing it again to verify the output status of the DO pin. The latter method allows the CPU to perform other processing during the wait period, allowing an efficient system to be designed.

Caution
1. **Input a low level to the DI pin during a verify operation.**
2. **If a high level is input to the DI pin at the rise of SK when the output status of the DO pin is high, the S-93C46B/56B/66B latches the instruction assuming that a start bit has been input. In this case, note that the DO pin immediately enters a high-impedance (High-Z) state.**

4. 2 Writing data (WRITE)

To write 16-bit data to a specified address, change CS to high and then input the WRITE instruction, address, and 16-bit data following the start bit. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRITE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

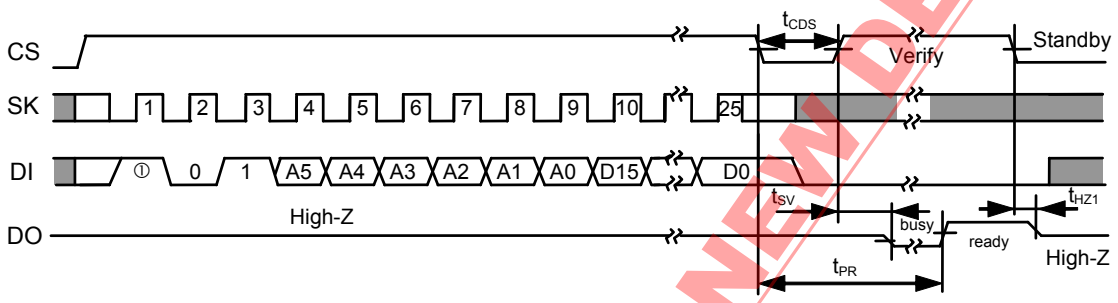


Figure 8 Data Write Timing (S-93C46B)

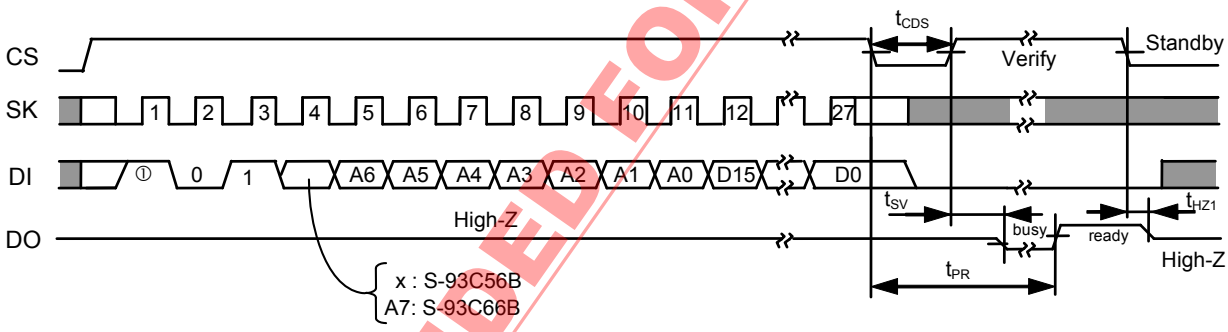


Figure 9 Data Write Timing (S-93C56B, S-93C66B)

4. 3 Erasing data (ERASE)

To erase 16-bit data at a specified address, set all 16 bits of the data to 1, change CS to high, and then input the ERASE instruction and address following the start bit. There is no need to input data. The data erase operation starts when CS goes low. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERASE instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

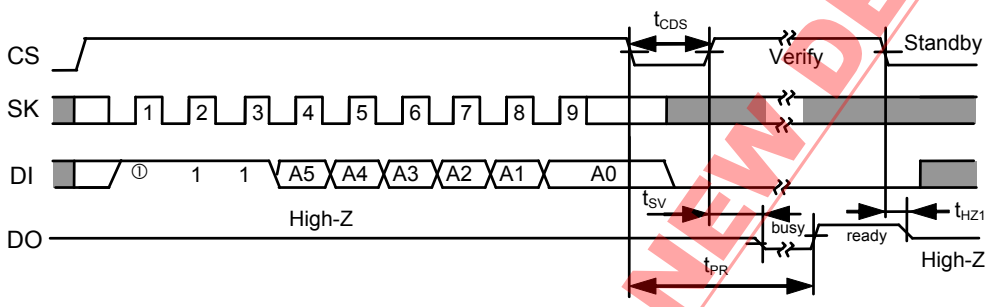


Figure 10 Data Erase Timing (S-93C46B)

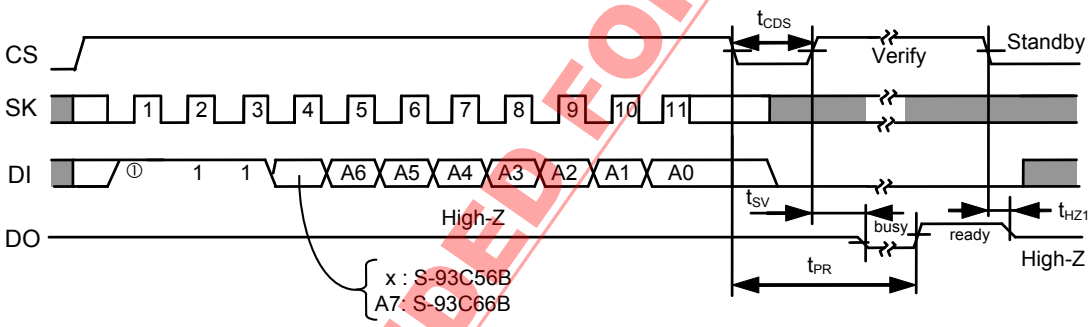


Figure 11 Data Erase Timing (S-93C56B, S-93C66B)

4. 4 Writing to chip (WRAL)

To write the same 16-bit data to the entire memory address space, change CS to high, and then input the WRAL instruction, an address, and 16-bit data following the start bit. Any address can be input. The write operation starts when CS goes low. There is no need to set the data to 1 before writing. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the WRAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

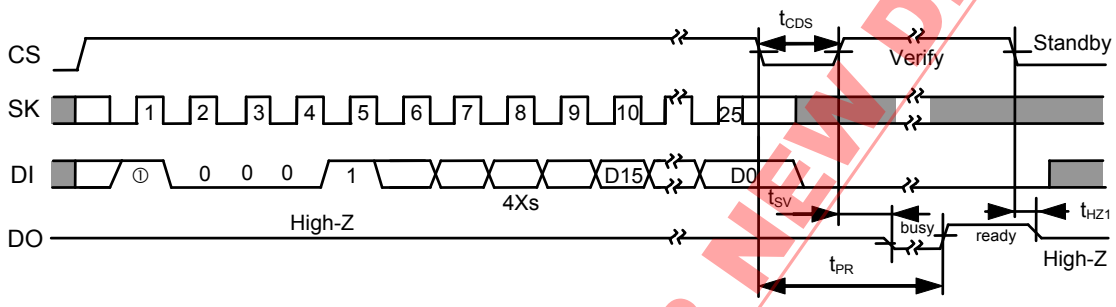


Figure 12 Chip Write Timing (S-93C46B)

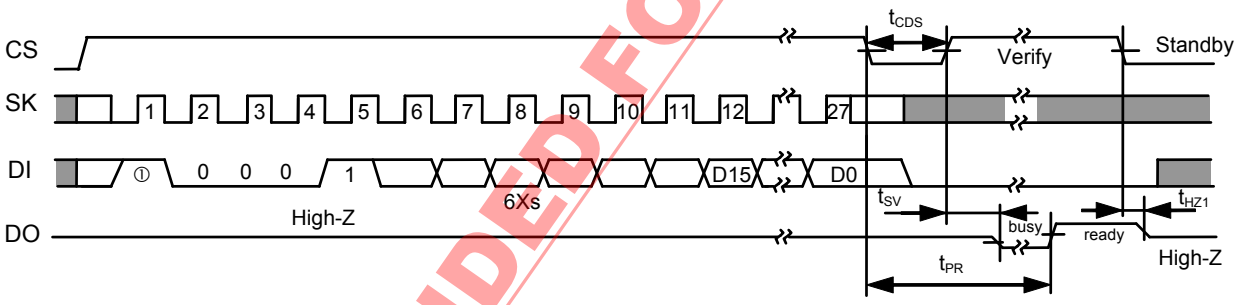


Figure 13 Chip Write Timing (S-93C56B, S-93C66B)

4. 5 Erasing chip (ERAL)

To erase the data of the entire memory address space, set all the data to 1, change CS to high, and then input the ERAL instruction and an address following the start bit. Any address can be input. There is no need to input data. The chips erase operation starts when CS goes low. If the clocks more than the specified number have been input, the clock pulse monitoring circuit cancels the ERAL instruction. For details of the clock pulse monitoring circuit, refer to "■ **Function to Protect Against Write due to Erroneous Instruction Recognition**".

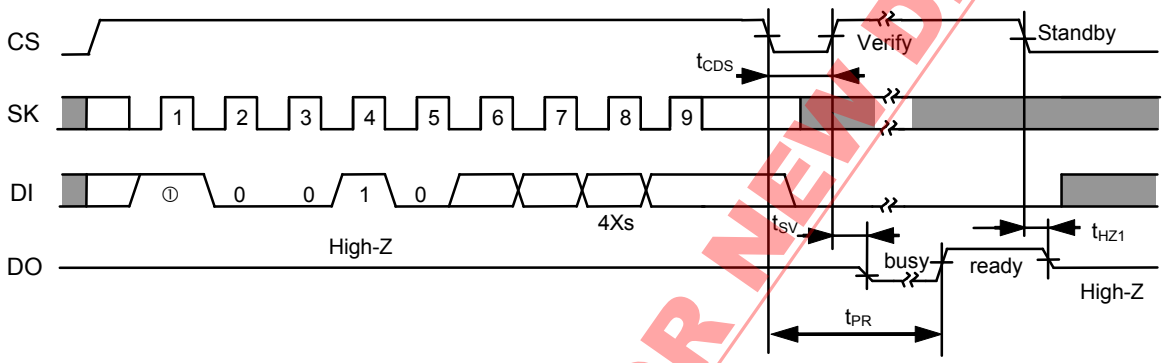


Figure 14 Chip Erase Timing (S-93C46B)

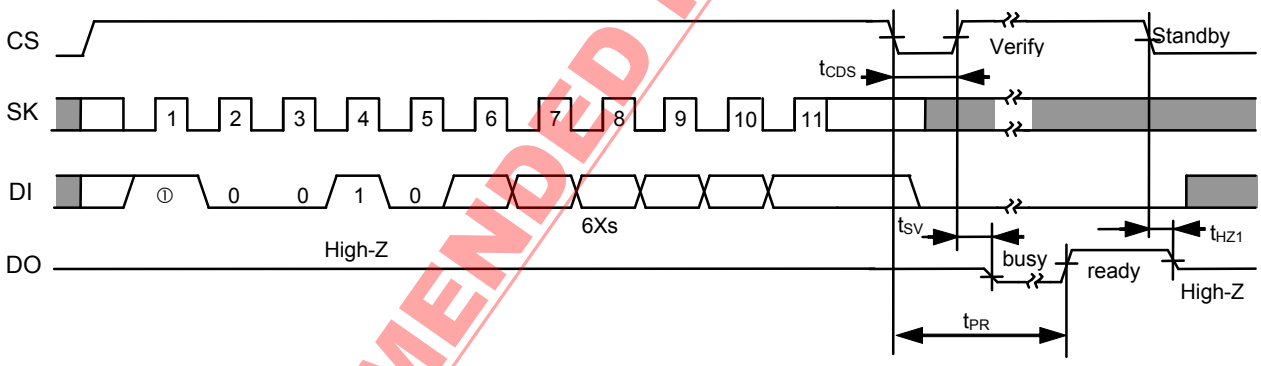


Figure 15 Chip Erase Timing (S-93C56B, S-93C66B)

5. Write enable (EWEN) and write disable (EWDS)

The EWEN instruction is an instruction that enables a write operation. The status in which a write operation is enabled is called the program enable mode.
The EWDS instruction is an instruction that disables a write operation. The status in which a write operation is disabled is called the program disable mode.
After CS goes high, input an instruction in the order of the start bit, EWEN or EWDS instruction, and address (optional). Each mode becomes valid by inputting a low level to CS after the last address (optional) has been input.

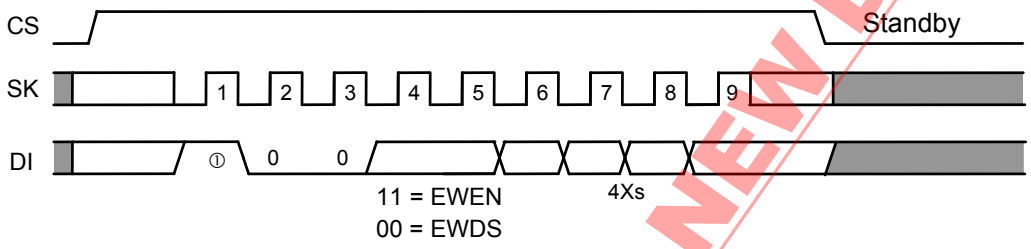


Figure 16 Write Enable/Disable Timing (S-93C46B)

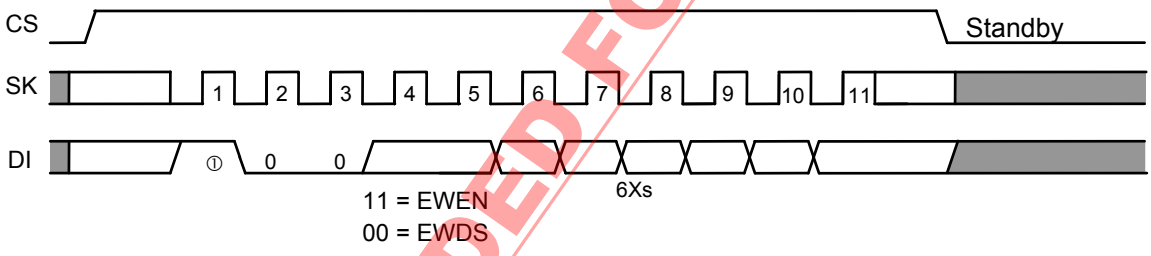


Figure 17 Write Enable/Disable Timing (S-93C56B, S-93C66B)

(1) Recommendation for write operation disable instruction

It is recommended to implement a design that prevents an incorrect write operation when a write instruction is erroneously recognized by executing the write operation disable instruction when executing instructions other than write instruction, and immediately after power-on and before power off.

■ Write Protect Function during the Low Power Supply Voltage

The S-93C46B/56B/66B provides a built-in detector. When the power supply voltage is low or at power application, the write instructions (WRITE, ERASE, WRAL, and ERAL) are cancelled, and the write disable state (EWDS) is automatically set. The detection voltage is 1.75 V typ., the release voltage is 2.05 V typ., and there is a hysteresis of about 0.3 V (refer to **Figure 18**). Therefore, when a write operation is performed after the power supply voltage has dropped and then risen again up to the level at which writing is possible, a write enable instruction (EWEN) must be sent before a write instruction (WRITE, ERASE, WRAL, or ERAL) is executed.
When the power supply voltage drops during a write operation, the data being written to an address at that time is not guaranteed.

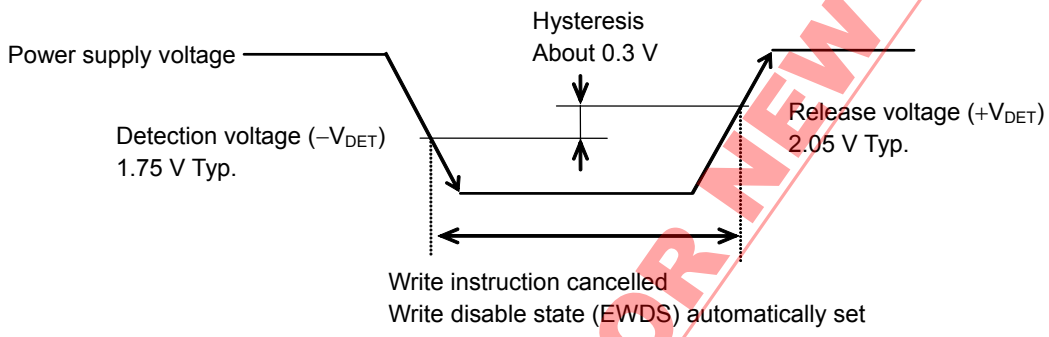
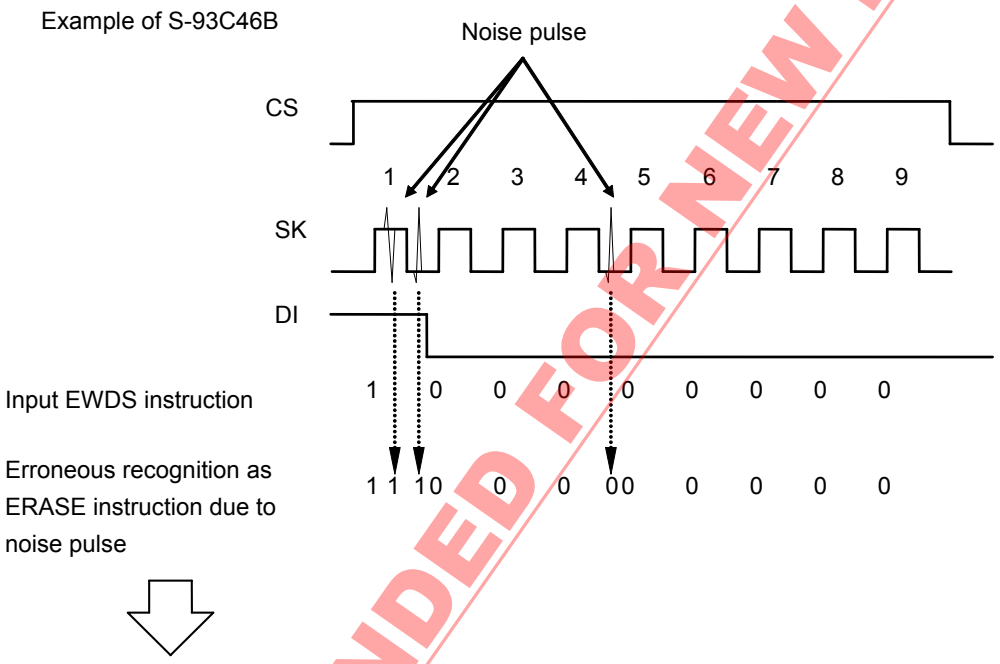


Figure 18 Operation during Low Power Supply Voltage

■ Function to Protect Against Write due to Erroneous Instruction Recognition

The S-93C46B/56B/66B provides a built-in clock pulse monitoring circuit which is used to prevent an erroneous write operation by canceling write instructions (WRITE, ERASE, WRAL, and ERAL) recognized erroneously due to an erroneous clock count caused by the application of noise pulses or double counting of clocks.
Instructions are cancelled if a clock pulse more or less than specified number decided by each write operation (WRITE, ERASE, WRAL, or ERAL) is detected.

<Example> Erroneous recognition of program disable instruction (EWDS) as erase instruction (ERASE)



In products that do not include a clock pulse monitoring circuit, FFFF is mistakenly written on address 00h. However the S-93C46B detects the overcount and cancels the instruction without performing a write operation.

Figure 19 Example of Clock Pulse Monitoring Circuit Operation

■ 3-Wire Interface (Direct Connection between DI and DO)

There are two types of serial interface configurations: a 4-wire interface configured using the CS, SK, DI, and DO pins, and a 3-wire interface that connects the DI input pin and DO output pin.
When the 3-wire interface is employed, a period in which the data output from the CPU and the data output from the serial memory collide may occur, causing a malfunction. To prevent such a malfunction, connect the DI and DO pins of the S-93C46B/56B/66B via a resistor (10 to 100 kΩ) so that the data output from the CPU takes precedence in being input to the DI pin (refer to "**Figure 20 Connection of 3-Wire Interface**").

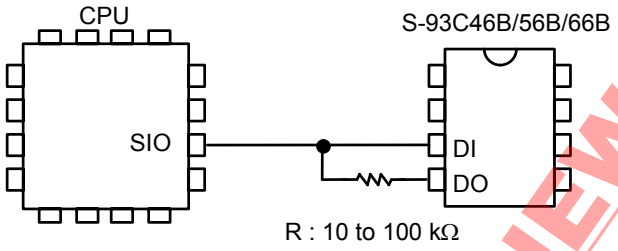


Figure 20 Connection of 3-Wire Interface

■ I/O Pin

1. Connection of input pins

All the input pins of the S-93C46B/56B/66B employ a CMOS structure, so design the equipment so that high impedance will not be input while the S-93C46B/56B/66B is operating. Especially, deselect the CS input (a low level) when turning on/off power and during standby. When the CS pin is deselected (a low level), incorrect data writing will not occur. Connect the CS pin to GND via a resistor (10 to 100 kΩ pull-down resistor). To prevent malfunction, it is recommended to use equivalent pull-down resistors for pins other than the CS pin.

2. Equivalent circuit of input and output pin

The following shows the equivalent circuits of input pins of the S-93C46B/56B/66B. None of the input pins incorporate pull-up and pull-down elements, so special care must be taken when designing to prevent a floating status.
Output pins are high-level/low-level/high-impedance tri-state outputs. The TEST pin is disconnected from the internal circuit by a switching transistor during normal operation. As long as the absolute maximum rating is satisfied, the TEST pin and internal circuit will never be connected.

2. 1 Input pin

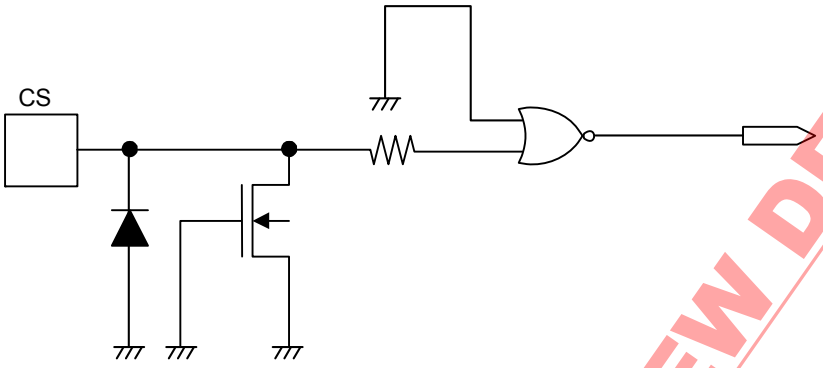


Figure 21 CS Pin

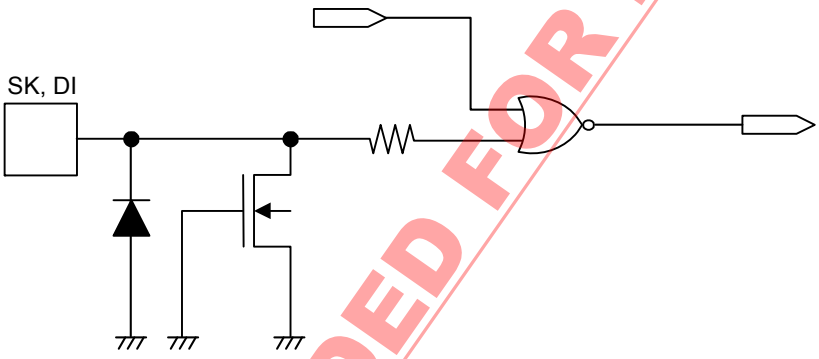


Figure 22 SK, DI Pin

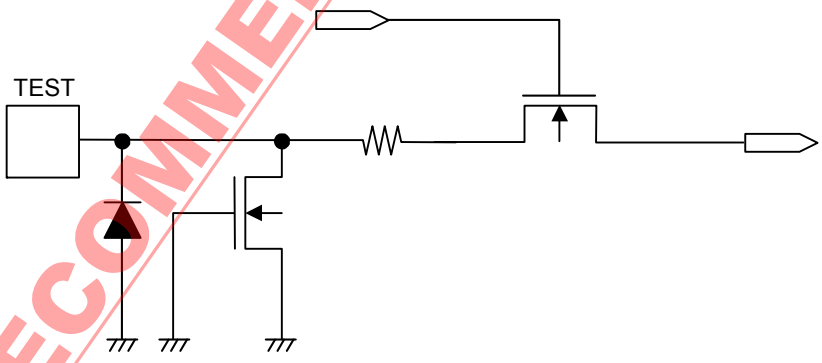


Figure 23 TEST Pin

2. 2 Output pin

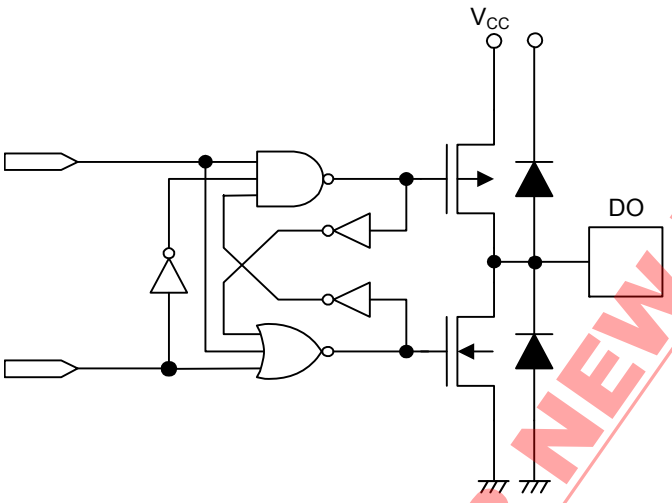


Figure 24 DO Pin

3. Input pin noise elimination time

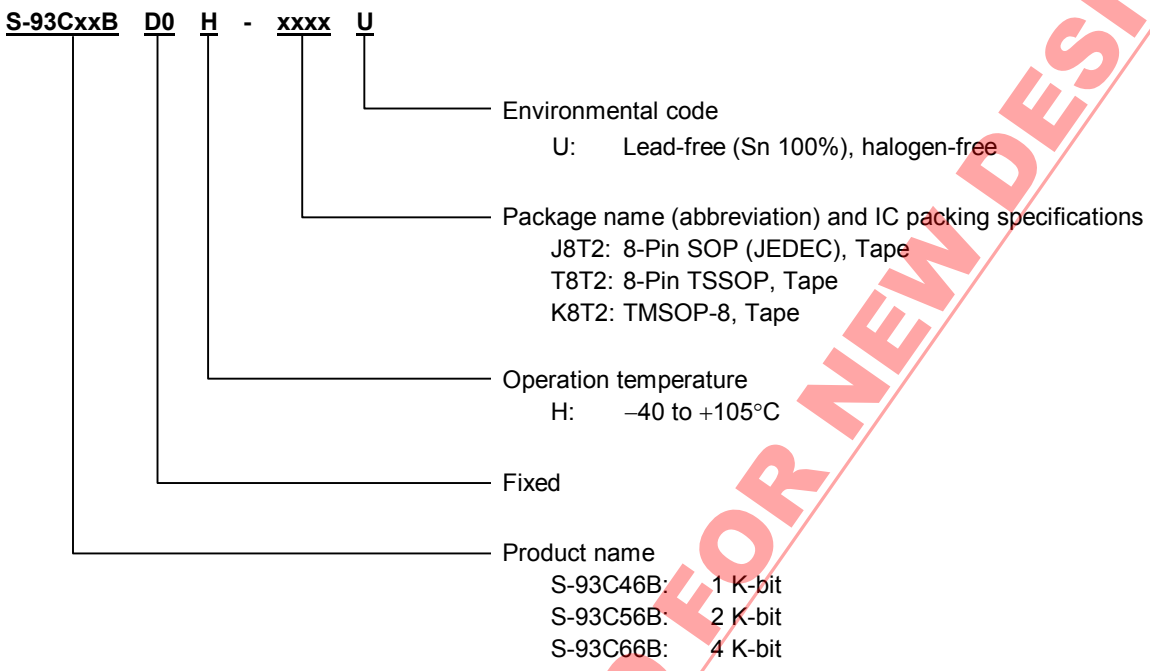
The S-93C46B/56B/66B include a built-in low-pass filter to eliminate noise at the SK, DI, and CS pins. This means that if the supply voltage is 5.0 V (at room temperature), noise with a pulse width of 20 ns or less can be eliminated. Note, therefore, the noise with a pulse width of more than 20 ns will be recognized as a pulse if the voltage exceeds V_{IH}/V_{IL}.

■ Precaution

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Product Name Structure

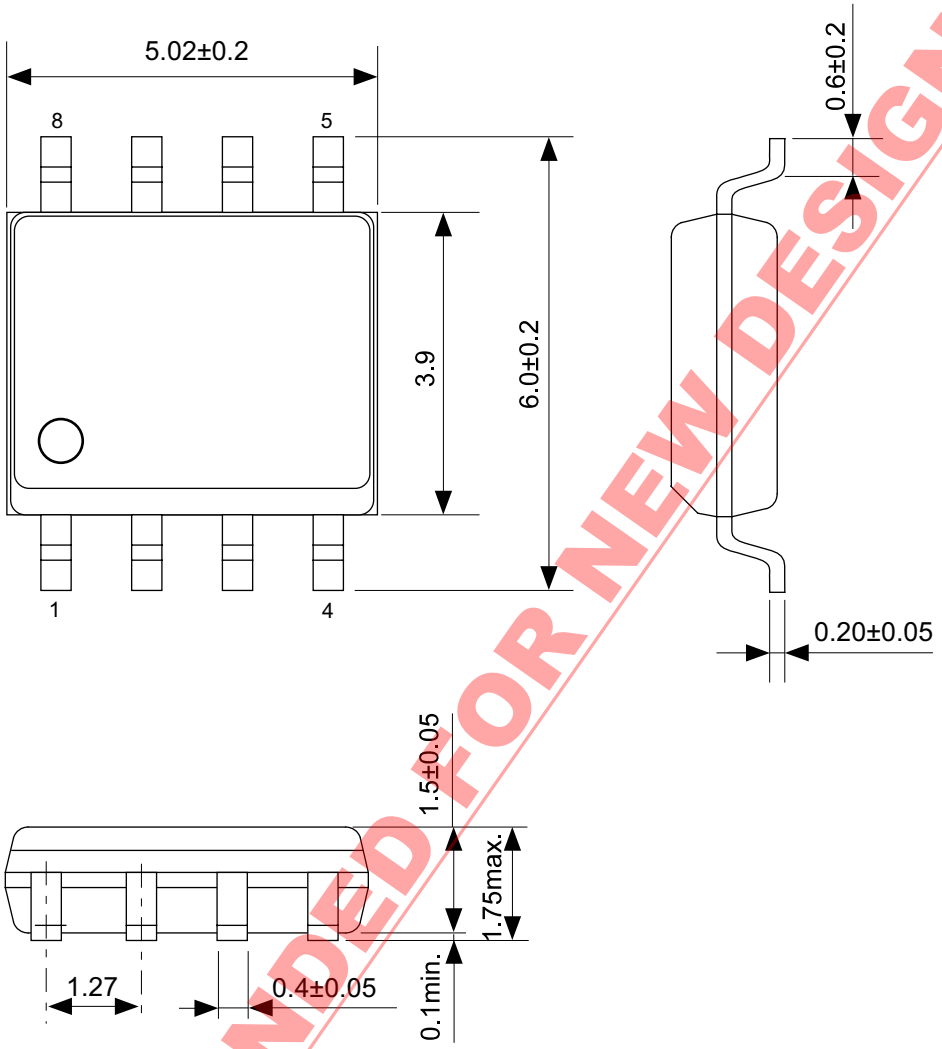
1. Product name



Remark Please contact our sales office for products with product name structure other than those specified above.

2. Package

Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A-P-SD	FJ008-D-C-SD	FJ008-D-R-SD
8-Pin TSSOP	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD



No. FJ008-A-P-SD-2.2

TITLE	SOP8J-D-PKG Dimensions
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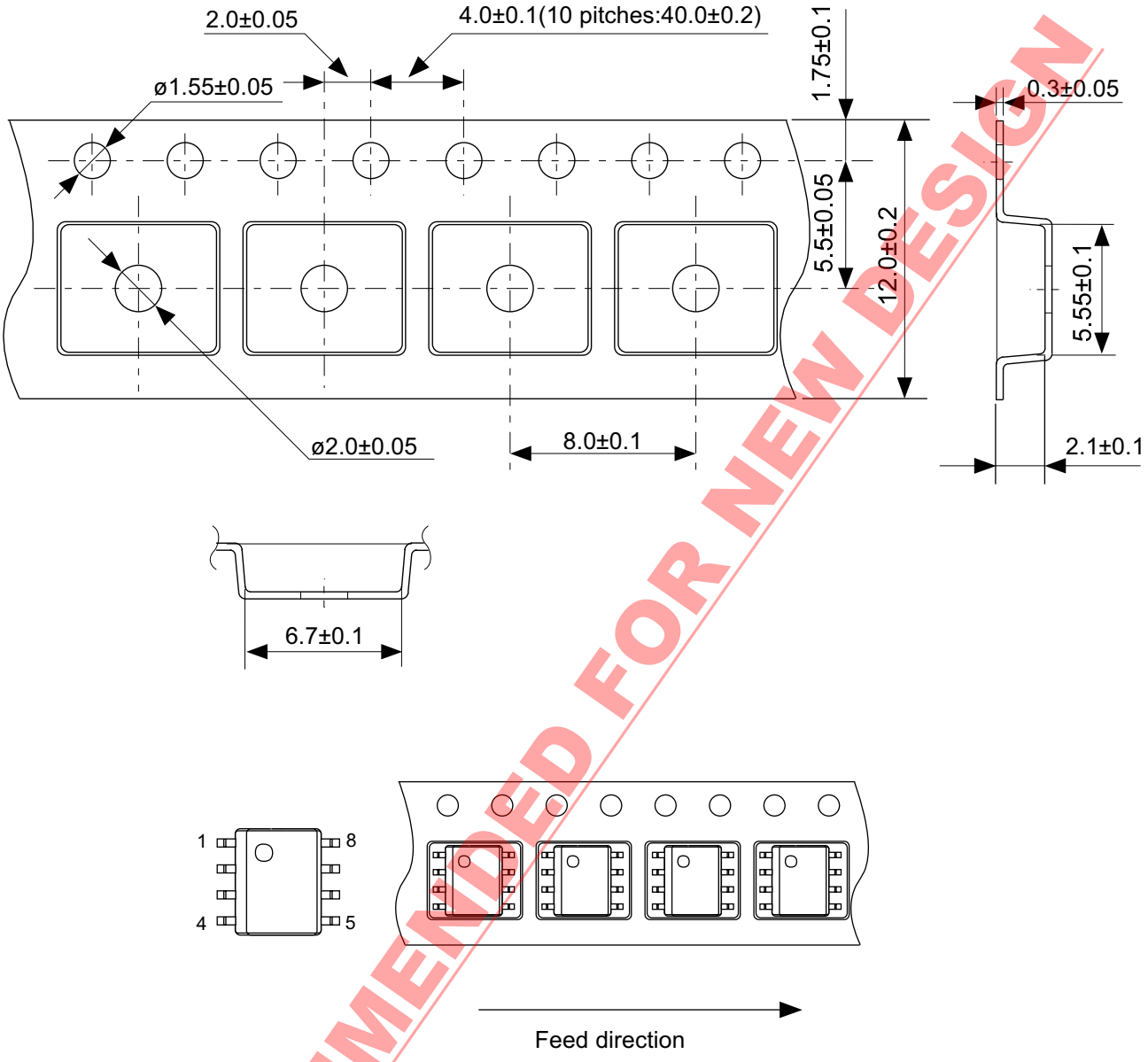
UNIT	mm

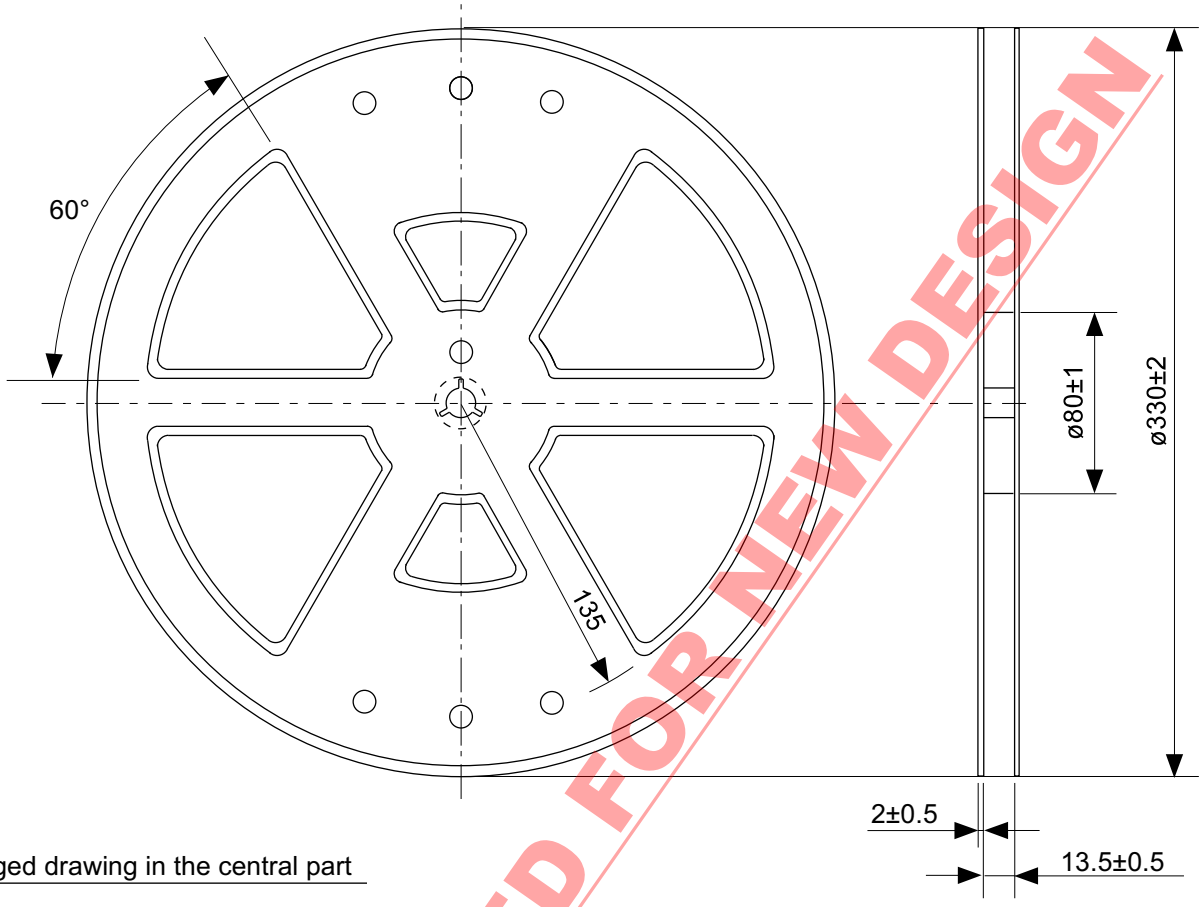
ABLIC Inc.



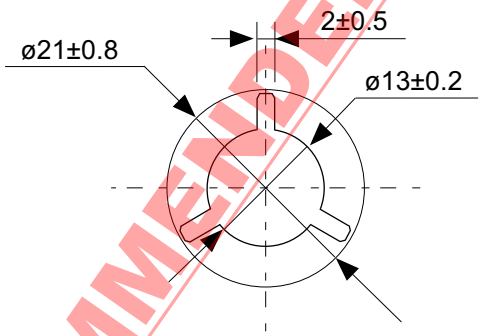
No. FJ008-D-C-SD-1.1

TITLE	SOP8J-D-Carrier Tape
No.	FJ008-D-C-SD-1.1
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part



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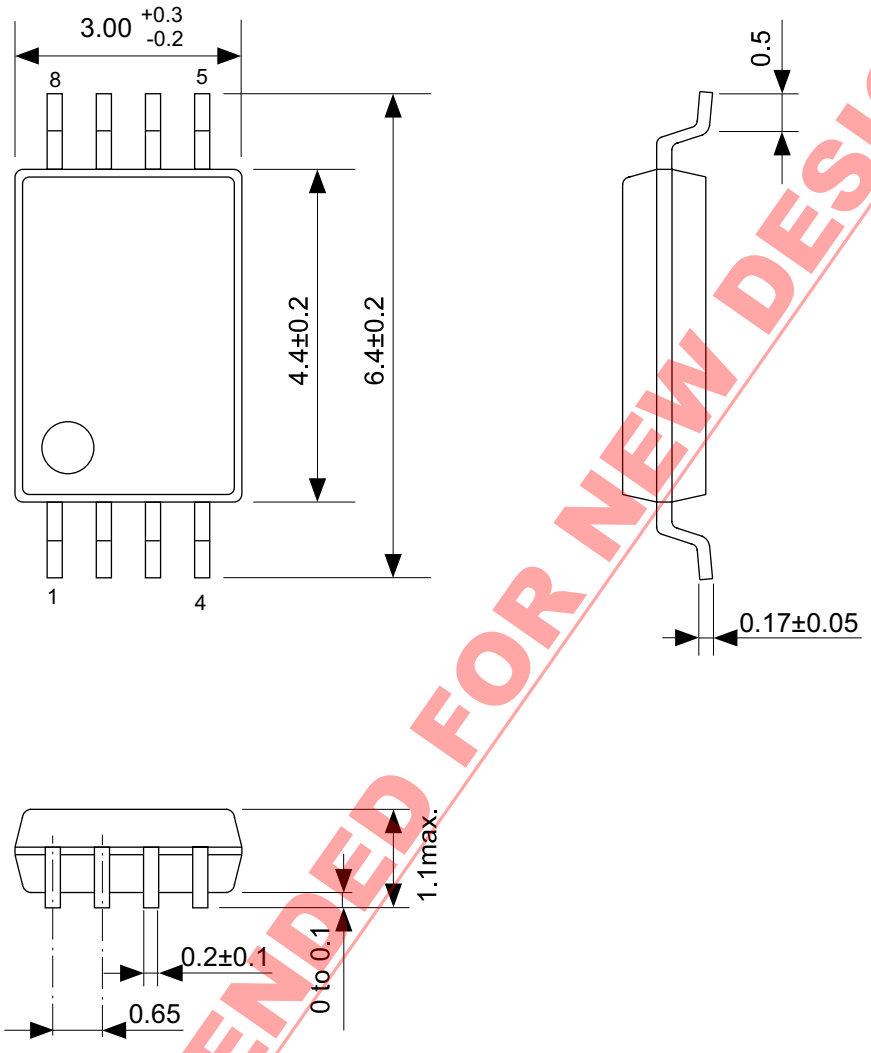
UNIT	mm		

ABLIC Inc.



No. FT008-A-P-SD-1.2

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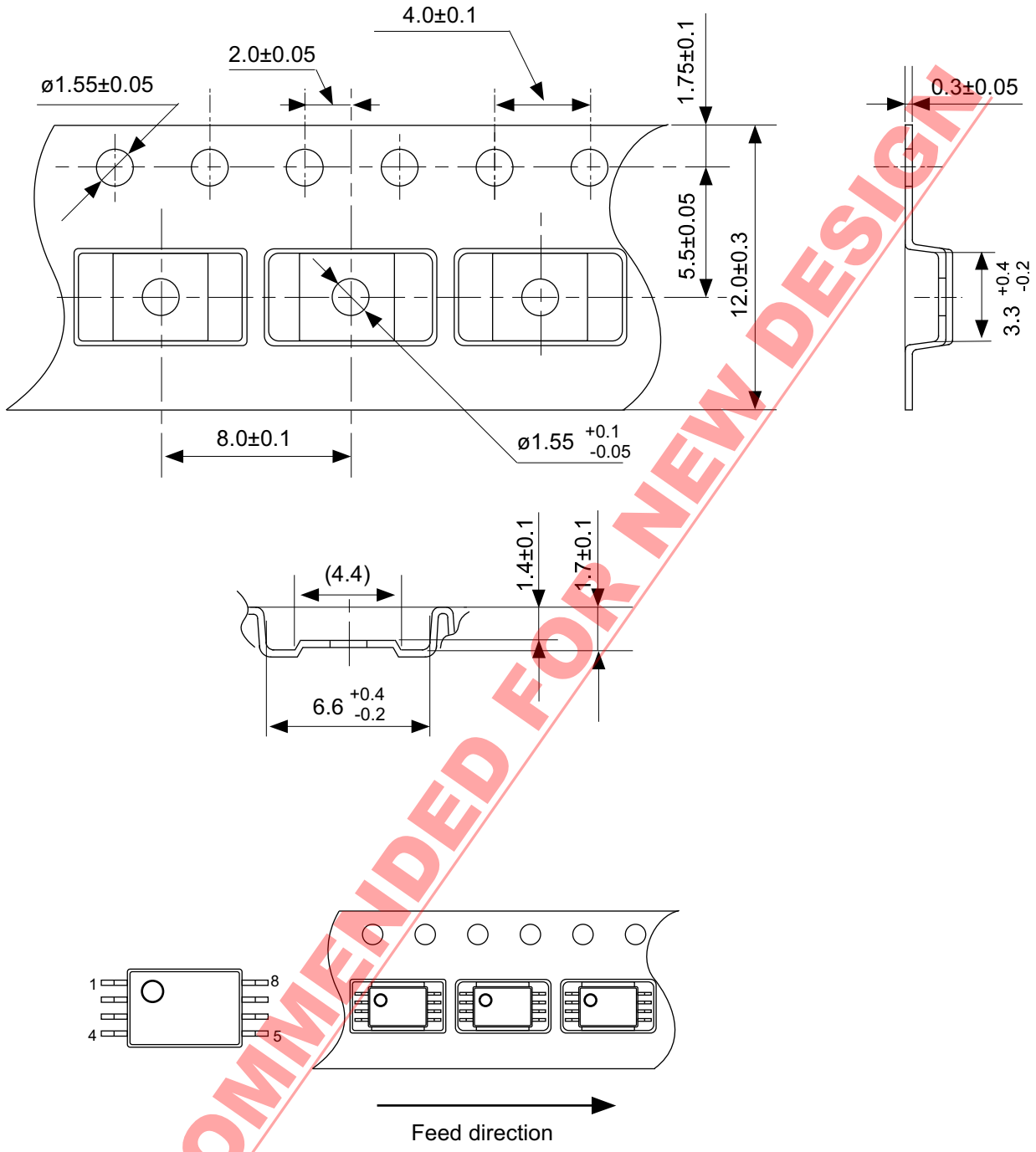
UNIT	mm

ABLIC Inc.



No. FT008-E-C-SD-1.0

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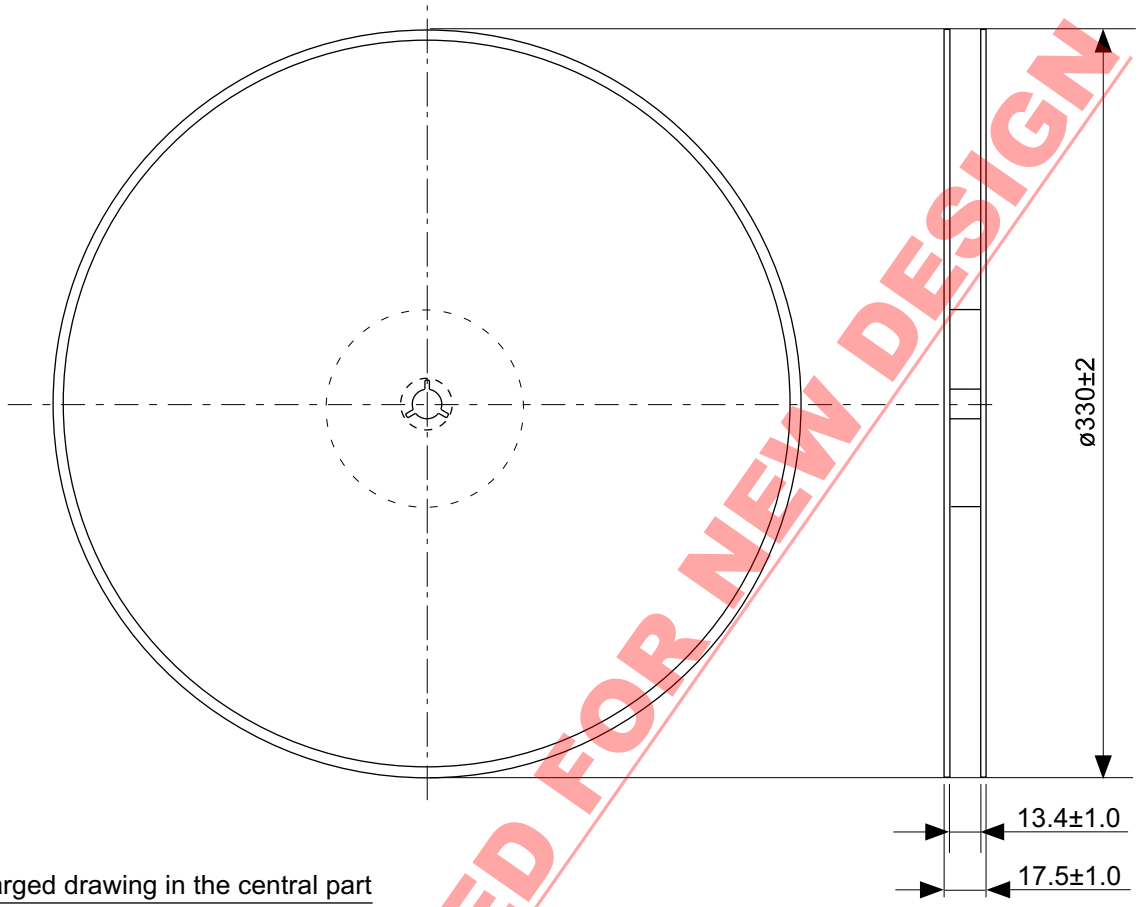
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



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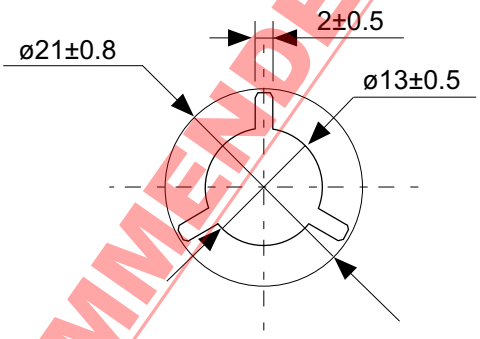

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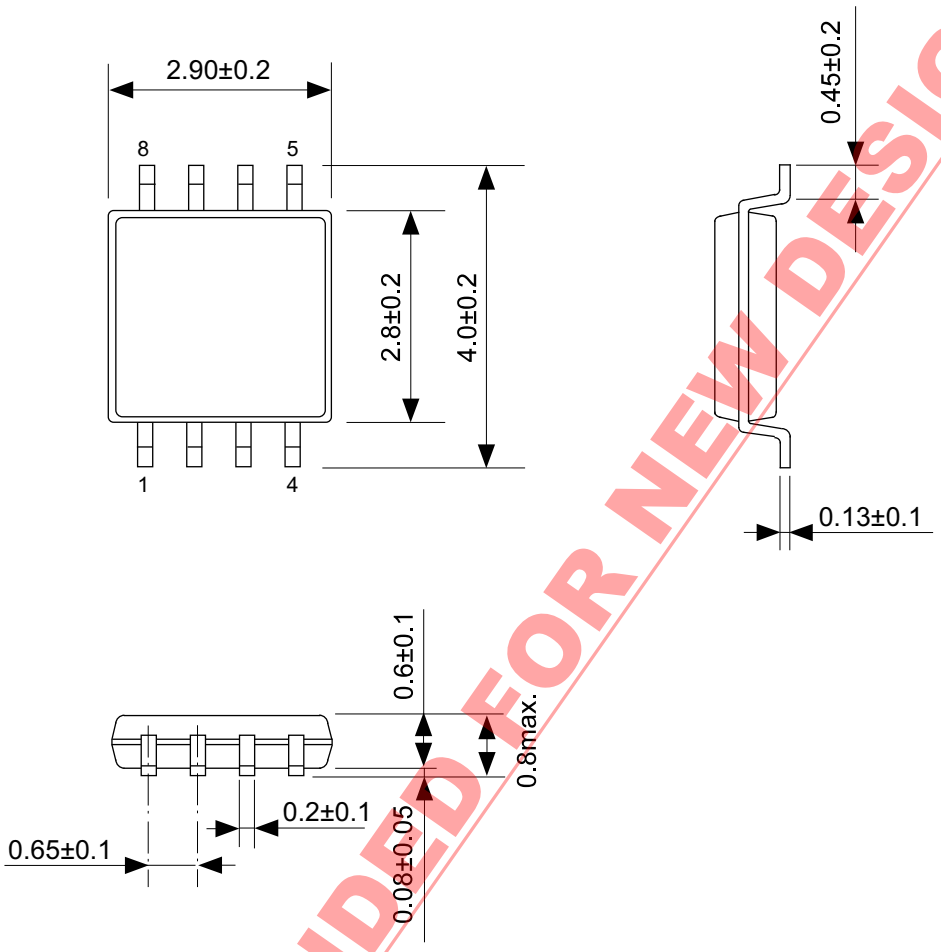
UNIT	mm		

ABLIC Inc.



No. FM008-A-P-SD-1.2

TITLE	TMSOP8-A-PKG Dimensions
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ANGLE	
UNIT	mm

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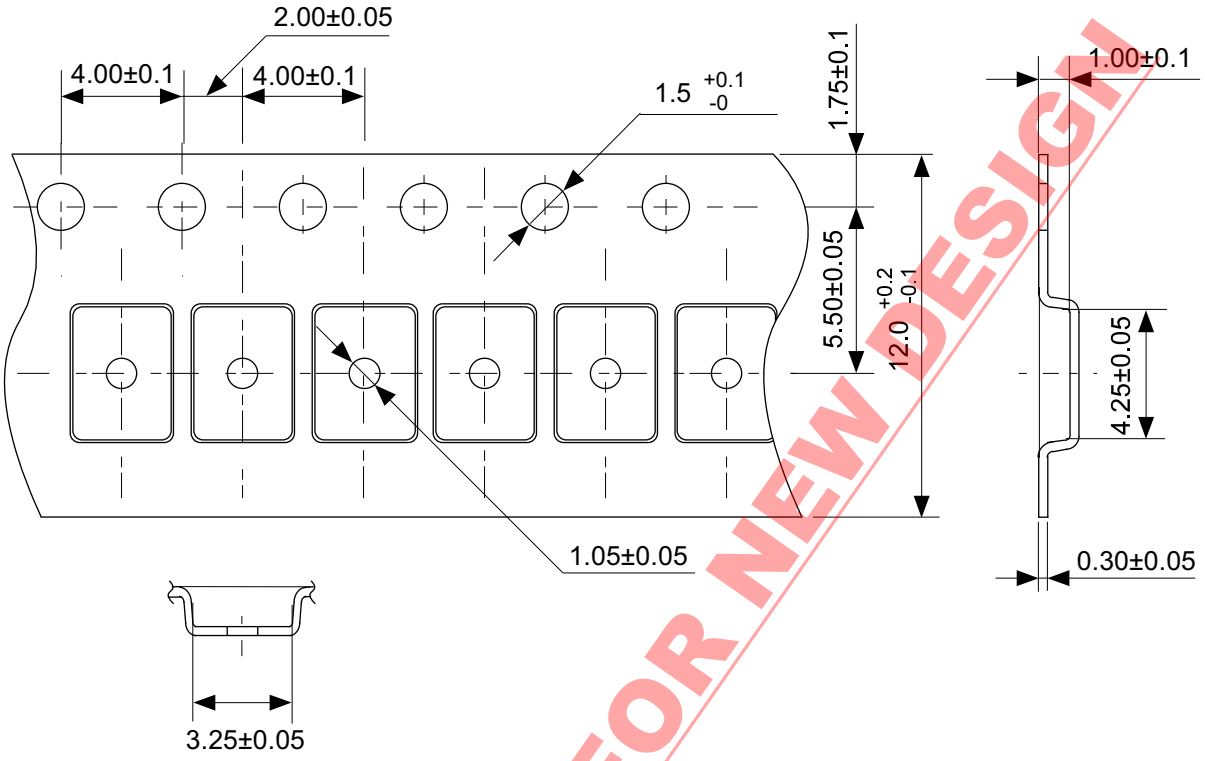
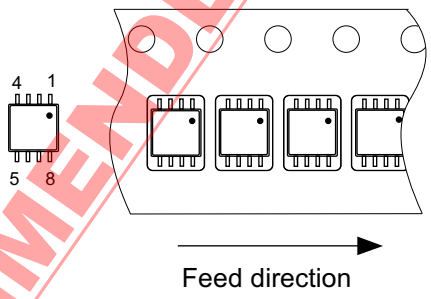
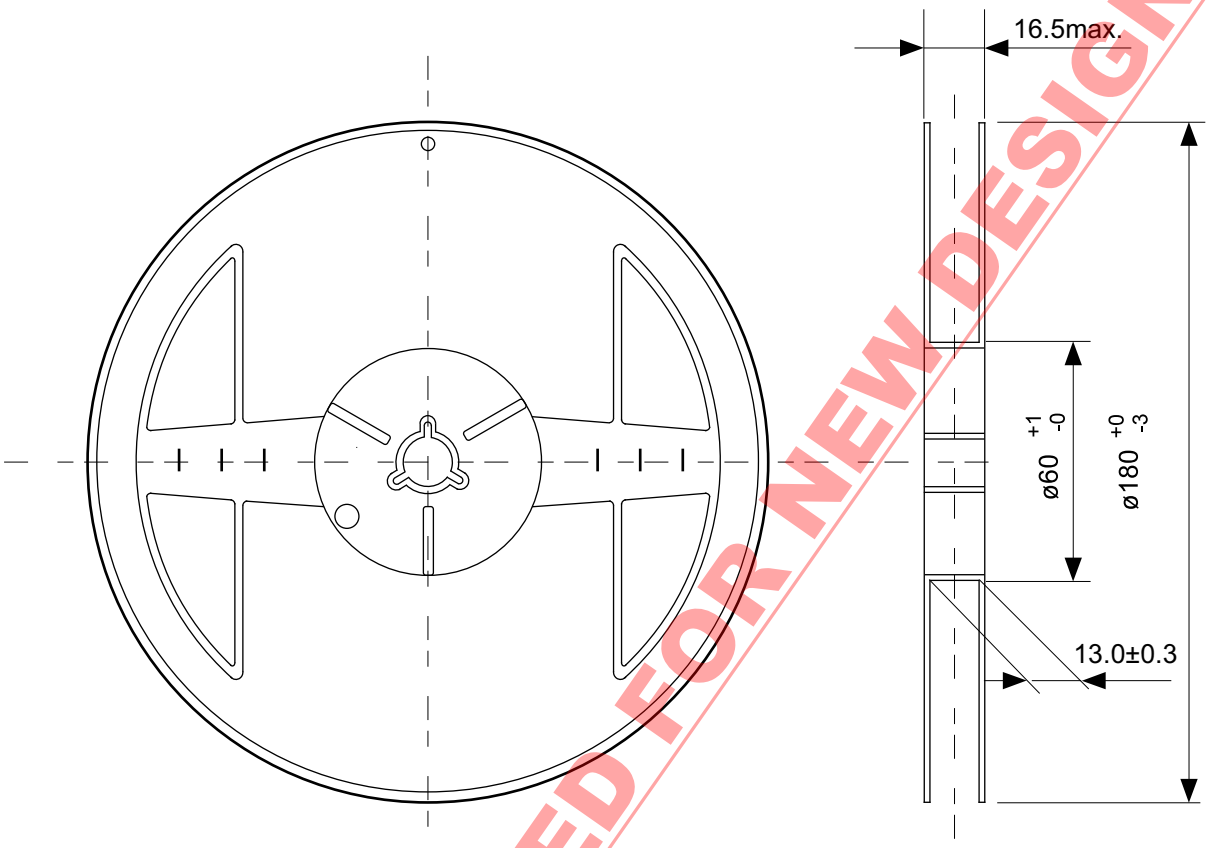




No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm

ABLIC Inc.



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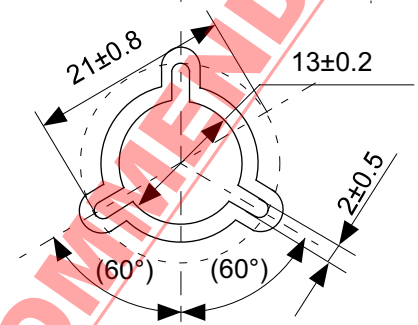

No. FM008-A-R-SD-1.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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