S-82L1A Series

BATTERY PROTECTION IC WITH ALARM FUNTION FOR 1-CELL PACK

www.ablic.com

Rev.1.3_00

The S-82L1A Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.
The alarm function enables the voltage detection immediately before the overcharge detection.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	4.200 V to 4.600 V (5 mV step)	Accuracy ±12 mV
Overcharge release voltage	4.000 V to 4.600 V*1	Accuracy ±50 mV
Overdischarge detection voltage	2.000 V to 3.000 V (10 mV step)	Accuracy ±50 mV
Overdischarge release voltage	2.000 V to 3.400 V*2	Accuracy ±100 mV
Alarm status detection voltage	4.200 V to 4.600 V (5 mV step)	Accuracy ±12 mV
Discharge overcurrent detection voltage	0.003 V to 0.100 V (1 mV step)	Accuracy ±3 mV
Load short-circuiting detection voltage	0.010 V to 0.100 V (5 mV step)	Accuracy ±7 mV
Charge overcurrent detection voltage	–0.100 V to –0.003 V (1 mV step)	Accuracy ±3 mV

- Detection delay times are generated only by an internal circuit (external capacitors are unnecessary).
- Discharge overcurrent control function
  - Release condition of discharge overcurrent status: Load disconnection
  - Release voltage of discharge overcurrent status: $V_{RIOV} = V_{DD} \times 0.8$ (typ.)
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- Alarm function
  - AO pin output logic: Active "L"
  - AO pin output form: CMOS output, Nch open-drain output
  - Connection when AO pin = "L": VSS pin, VM pin
- High-withstand voltage: VM pin, CO pin and AO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = –40°C to +85°C
- Low current consumption
  - During operation: 800 nA typ., 1500 nA max. (Ta = +25°C)
  - During power-down: 50 nA max. (Ta = +25°C)
  - During overdischarge: 500 nA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)

***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SNT-6A

■ Block Diagram

1. CMOS output, connection when AO pin = "L": VSS pin

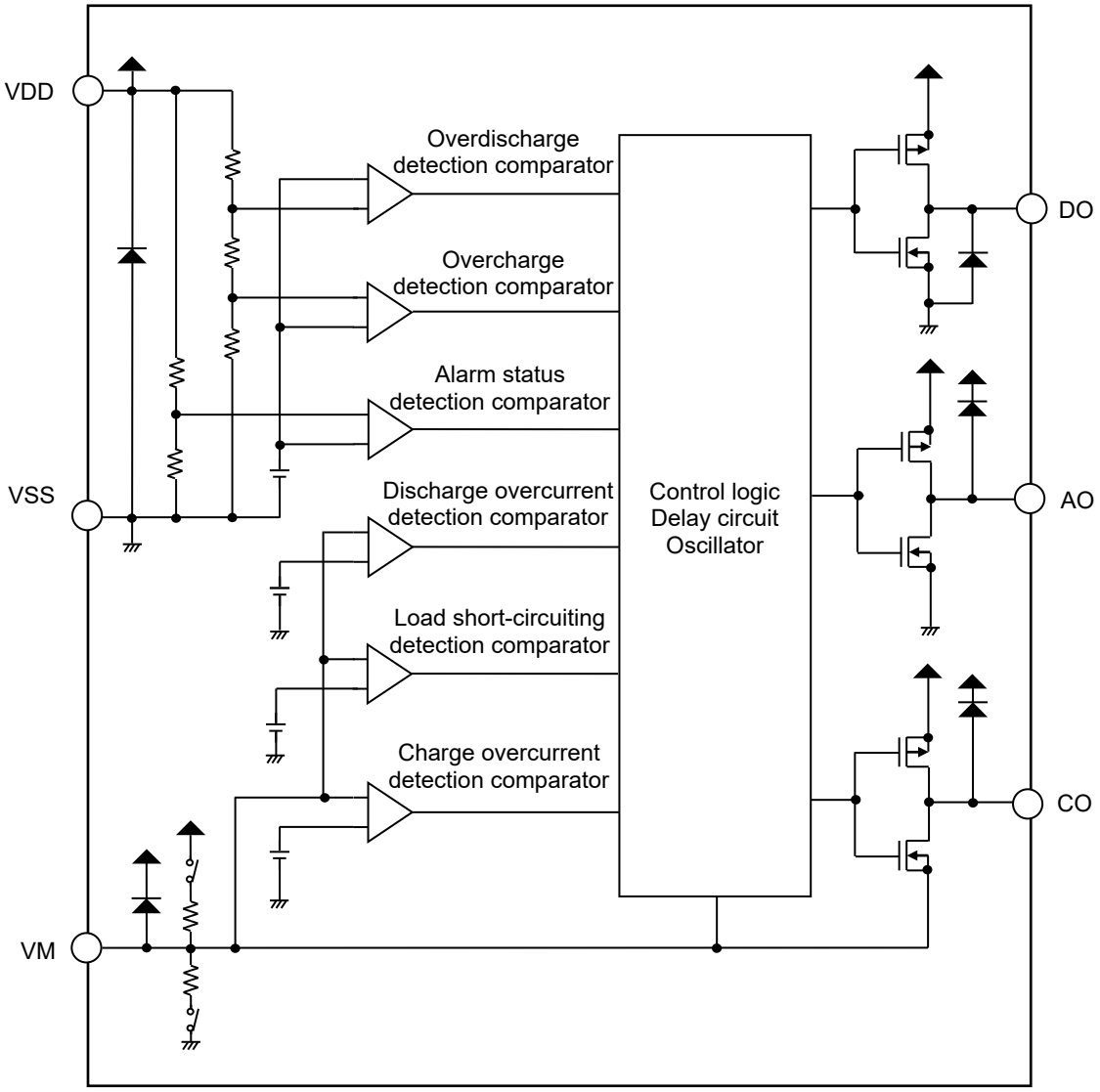


Figure 1

2. Nch open-drain output, connection when AO pin = "L": VSS pin

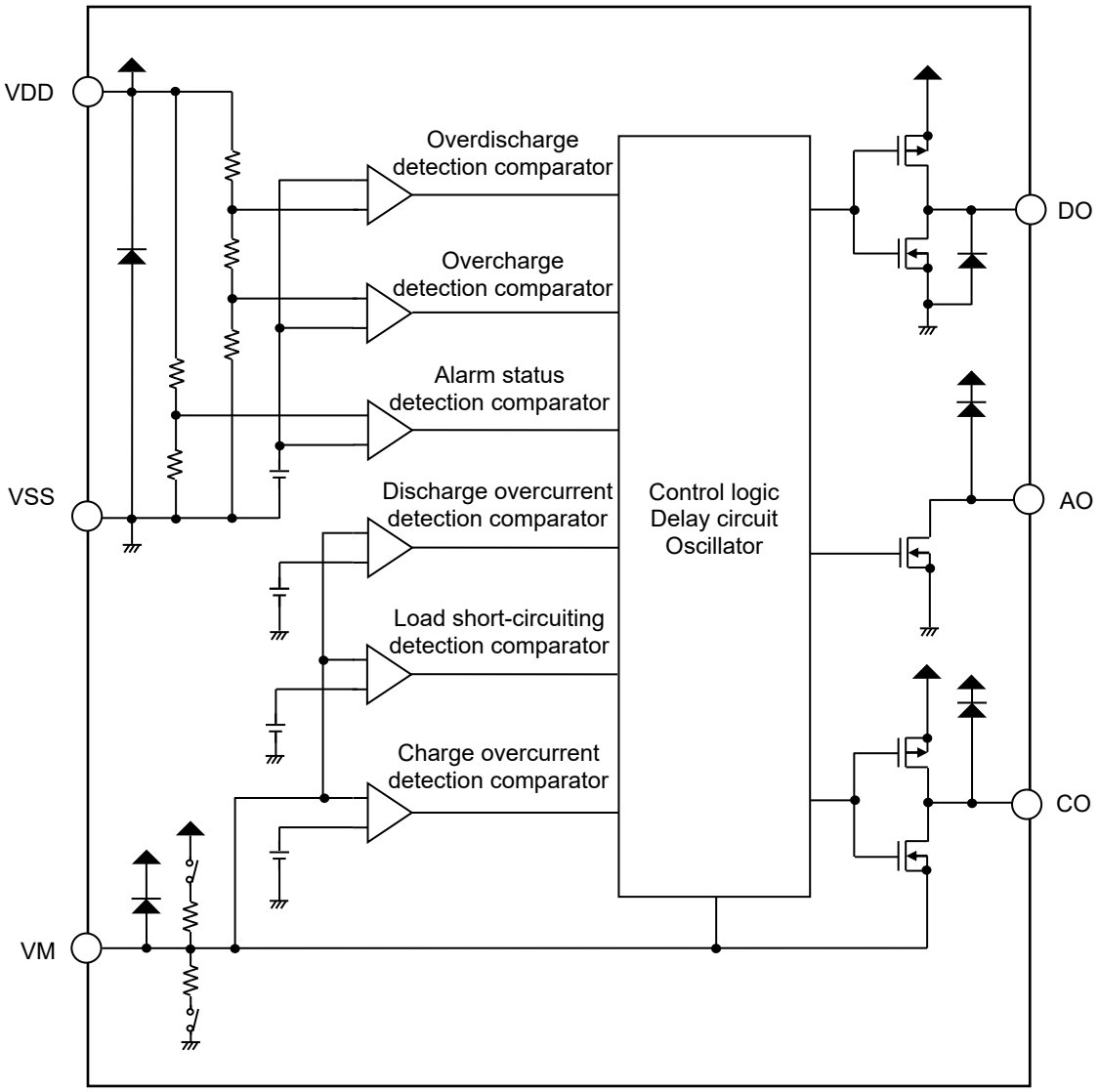


Figure 2

3. CMOS output, connection when AO pin = "L": VM pin

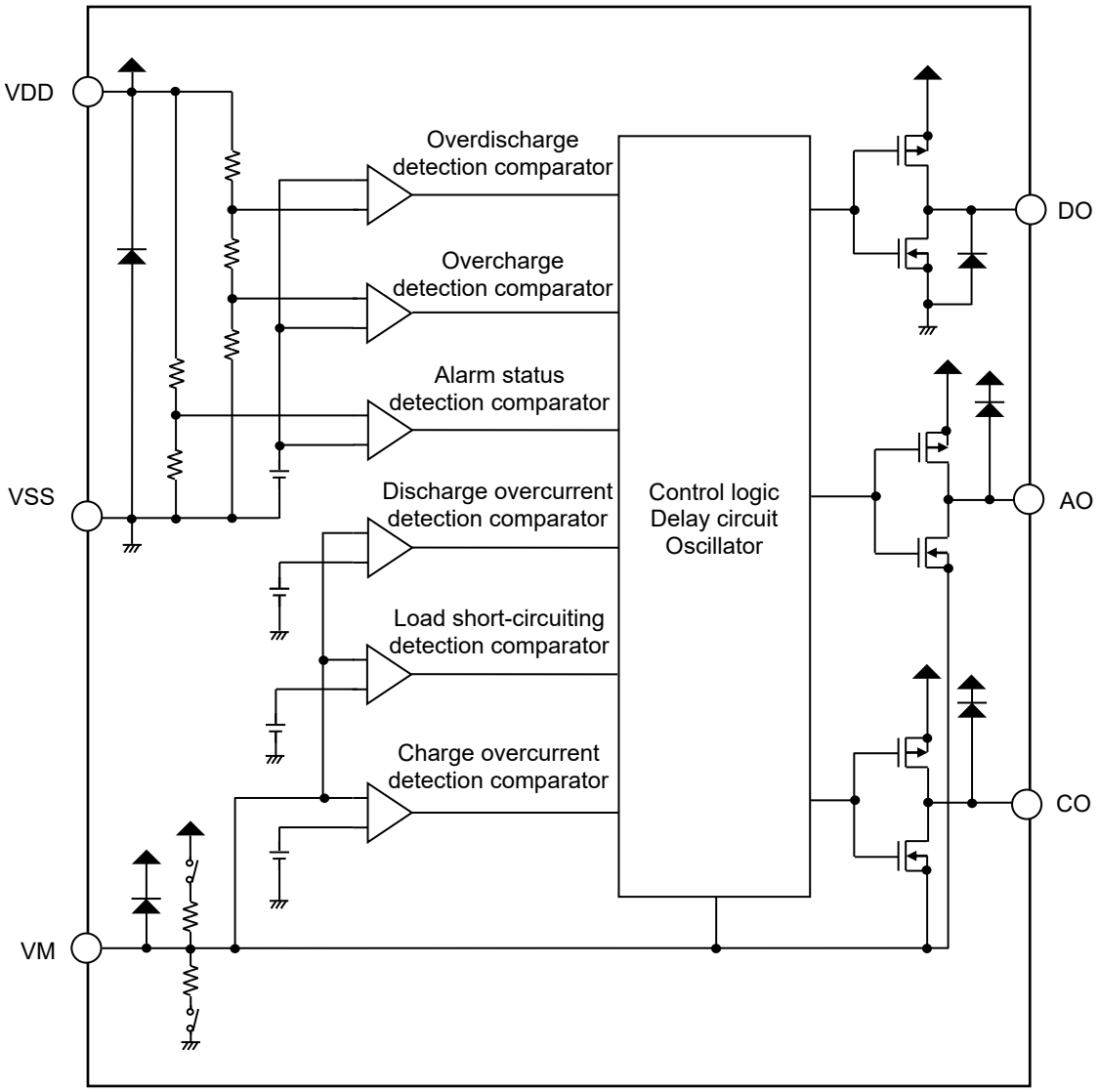


Figure 3

4. Nch open-drain output, connection when AO pin = "L": VM pin

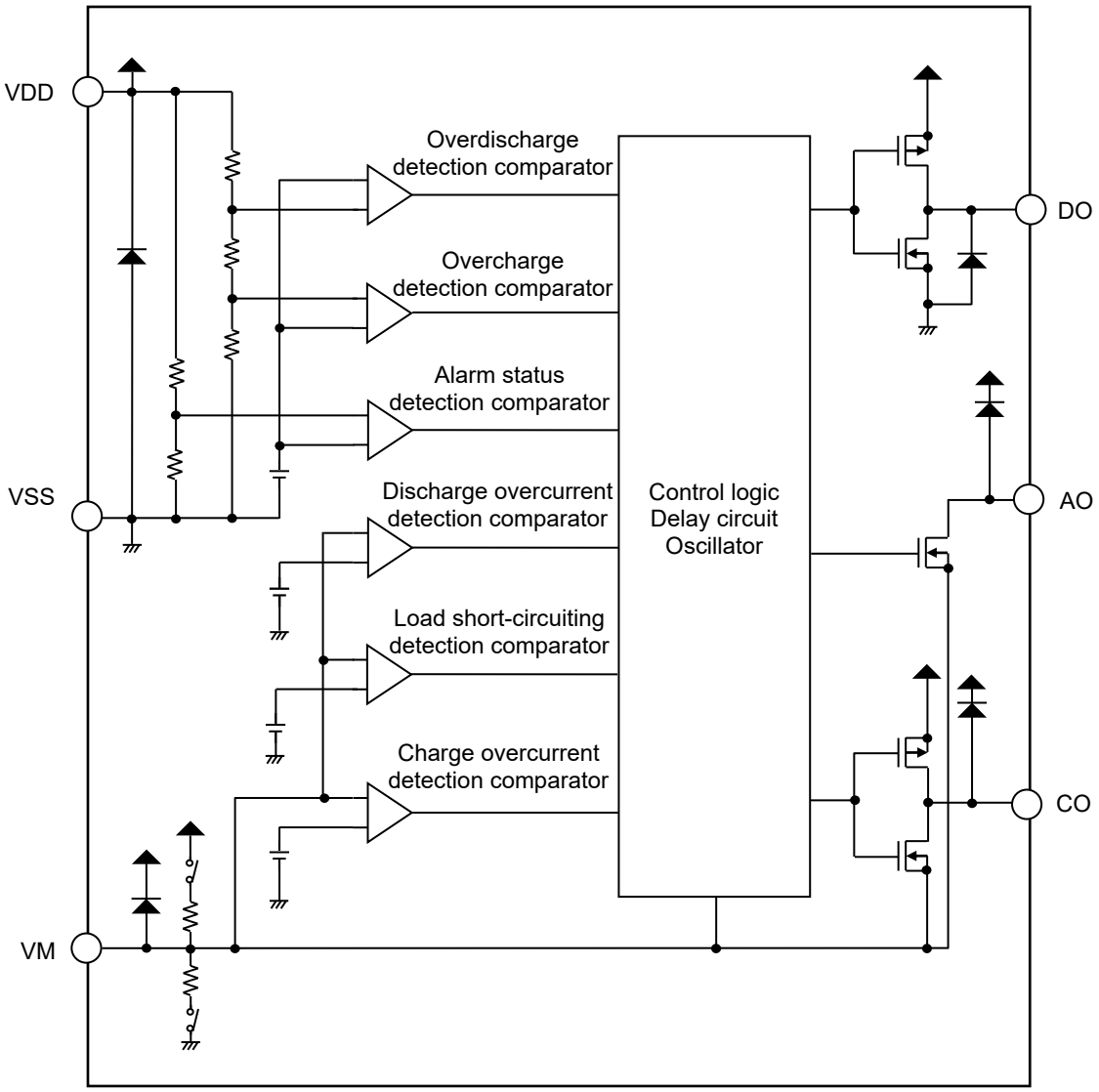


Figure 4

■ Product Name Structure

1. Product name

S-82L1A xx - I6T1 U 7

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - I6T1: SNT-6A, Tape
- Serial code*2
  - Sequentially set from AA to ZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

Table 2 (1 / 2)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Alarm Status Detection Voltage [V_{AU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82L1AAA-I6T1U7	4.550 V	4.350 V	2.600 V	3.000 V	4.440 V	0.045 V	0.095 V	–0.040 V

Table 2 (2 / 2)

Product Name	Delay Time Combination*1	AO Pin Output Form*2	Connection when AO Pin = "L"*3	0 V Battery Charge*4	Power-down Function*5
S-82L1AAA-I6T1U7	(1)	Nch open-drain output	VSS pin	Inhibited	Unavailable

***1.** Refer to **Table 3** about the details of the delay time combinations.
***2.** AO pin output form: CMOS output, Nch open-drain output
***3.** Connection when AO pin = "L": VSS pin, VM pin
***4.** 0 V battery charge: Enabled, inhibited
***5.** Power-down function: Available, unavailable

Remark Please contact our sales representatives for products other than the above.

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Alarm Status Detection Delay Time [t_{AU}]	Discharge Overcurrent Detection Delay Time [t_{DIOV}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]
(1)	1.0 s	64 ms	1.0 s	16 ms	280 µs	16 ms

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales representatives.

Table 4

Delay Time	Symbol	Selection Range					Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s	–	–	Select a value from the left.
Overdischarge detection delay time	t_{DL}	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.
Alarm status detection delay time	t_{AU}	1 ms	1.0 s	–	–	–	Select a value from the left.
Discharge overcurrent detection delay time	t_{DIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 µs	530 µs	–	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	Select a value from the left.

■ Pin Configuration

1. SNT-6A

Top view

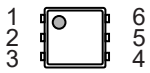


Figure 5

Table 5

Pin No.	Symbol	Description
1	AO	Alarm signal output pin (CMOS output or Nch open-drain output)
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Connection pin of discharge control FET gate (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Overcurrent detection pin

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 6	V
VM pin input voltage	V_{VM}	VM	V_{DD} – 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} – 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{DD} – 28 to V_{DD} + 0.3	V
AO pin output voltage	V_{AO}	AO	V_{DD} – 28 to V_{DD} + 0.3	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–55 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SNT-6A	Board A	–	224	–	°C/W
			Board B	–	176	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

1. Ta = +25°C

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	Ta = 0°C to +50°C*1	V_{CU} – 0.012	V_{CU}	V_{CU} + 0.012	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.050	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.017	V_{CL}	V_{CL} + 0.012	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.050	V_{DL}	V_{DL} + 0.050	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.100	V_{DU}	V_{DU} + 0.100	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.050	V_{DU}	V_{DU} + 0.050	V	2
Alarm status detection voltage	V_{AU}	Ta = 0°C to +50°C*1	V_{AU} – 0.012	V_{AU}	V_{AU} + 0.012	V	1
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIOV} – 0.003	V_{DIOV}	V_{DIOV} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.007	V_{SHORT}	V_{SHORT} + 0.007	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.003	V_{CIOV}	V_{CIOV} + 0.003	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	$V_{DD} \times 0.77$	$V_{DD} \times 0.80$	$V_{DD} \times 0.83$	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.7	1.1	1.5	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.9	1.2	1.5	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	500	1250	2500	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	5	10	15	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	800	1500	nA	3
Current consumption during power-down	I_{PDN}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	50	nA	3
Current consumption during overdischarge	I_{OPED}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	500	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	5	10	20	kΩ	4
CO pin resistance "L"	R_{COL}	–	2.5	5	10	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	1	2	4	kΩ	4
AO pin resistance "H"	R_{AOH}	CMOS output product	15	30	60	kΩ	4
AO pin resistance "L"	R_{AOL}	–	1	2	4	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.7$	t_{DL}	$t_{DL} \times 1.3$	–	5
Alarm status detetion delay time	t_{AU}	–	$t_{AU} \times 0.7$	t_{AU}	$t_{AU} \times 1.3$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV} \times 0.7$	t_{DIOV}	$t_{DIOV} \times 1.3$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.7$	t_{SHORT}	$t_{SHORT} \times 1.3$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.7$	t_{CIOV}	$t_{CIOV} \times 1.3$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Ta = –20°C to +60°C*1

Table 9

(Ta = –20°C to +60°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.017	V_{CU}	V_{CU} + 0.017	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.065	V_{CL}	V_{CL} + 0.057	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.022	V_{CL}	V_{CL} + 0.017	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.060	V_{DL}	V_{DL} + 0.055	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.110	V_{DU}	V_{DU} + 0.105	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.060	V_{DU}	V_{DU} + 0.055	V	2
Alarm status detection voltage	V_{AU}	–	V_{AU} – 0.017	V_{AU}	V_{AU} + 0.017	V	1
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIOV} – 0.003	V_{DIOV}	V_{DIOV} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.007	V_{SHORT}	V_{SHORT} + 0.007	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.003	V_{CIOV}	V_{CIOV} + 0.003	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	$V_{DD} \times 0.77$	$V_{DD} \times 0.80$	$V_{DD} \times 0.83$	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.7	1.2	1.7	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	250	1250	3500	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	3.5	10	20	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	800	3000	nA	3
Current consumption during power-down	I_{PDN}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	100	nA	3
Current consumption during overdischarge	I_{OPED}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	1000	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.5	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	–	1.25	5	15	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
AO pin resistance "H"	R_{AOH}	CMOS output product	7.5	30	90	kΩ	4
AO pin resistance "L"	R_{AOL}	–	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.6$	t_{CU}	$t_{CU} \times 1.4$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.6$	t_{DL}	$t_{DL} \times 1.4$	–	5
Alarm status detetion delay time	t_{AU}	–	$t_{AU} \times 0.6$	t_{AU}	$t_{AU} \times 1.4$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV} \times 0.65$	t_{DIOV}	$t_{DIOV} \times 1.35$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.6$	t_{SHORT}	$t_{SHORT} \times 1.4$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.6$	t_{CIOV}	$t_{CIOV} \times 1.4$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

3. Ta = –40°C to +85°C*1

Table 10

(Ta = –40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.045	V_{CU}	V_{CU} + 0.030	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.080	V_{CL}	V_{CL} + 0.060	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.050	V_{CL}	V_{CL} + 0.030	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.080	V_{DL}	V_{DL} + 0.060	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.130	V_{DU}	V_{DU} + 0.110	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.080	V_{DU}	V_{DU} + 0.060	V	2
Alarm status detection voltage	V_{AU}	–	V_{AU} – 0.045	V_{AU}	V_{AU} + 0.030	V	1
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIOV} – 0.003	V_{DIOV}	V_{DIOV} + 0.003	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	V_{SHORT} – 0.007	V_{SHORT}	V_{SHORT} + 0.007	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.003	V_{CIOV}	V_{CIOV} + 0.003	V	2
Discharge overcurrent release voltage	V_{RIOV}	V_{DD} = 3.4 V	$V_{DD} \times 0.77$	$V_{DD} \times 0.80$	$V_{DD} \times 0.83$	V	2
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	0.5	1.1	1.7	V	4
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge inhibited	0.7	1.2	1.7	V	2
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	V_{DD} = 1.8 V, V_{VM} = 0 V	250	1250	3500	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	V_{DD} = 3.4 V, V_{VM} = 1.0 V	3.5	10	20	kΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.0	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	800	3000	nA	3
Current consumption during power-down	I_{PDN}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	100	nA	3
Current consumption during overdischarge	I_{OPED}	$V_{DD} = V_{VM}$ = 1.5 V	–	–	1000	nA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.5	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	–	1.25	5	15	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	0.5	2	6	kΩ	4
AO pin resistance "H"	R_{AOH}	CMOS output product	7.5	30	90	kΩ	4
AO pin resistance "L"	R_{AOL}	–	0.5	2	6	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.4$	t_{CU}	$t_{CU} \times 1.6$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.4$	t_{DL}	$t_{DL} \times 1.6$	–	5
Alarm status detetion delay time	t_{AU}	–	$t_{AU} \times 0.4$	t_{AU}	$t_{AU} \times 1.6$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV} \times 0.4$	t_{DIOV}	$t_{DIOV} \times 1.6$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.4$	t_{SHORT}	$t_{SHORT} \times 1.6$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.4$	t_{CIOV}	$t_{CIOV} \times 1.6$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.
The output voltage levels "H" and "L" at AO pin (V_{AO}) are judged by V_{DD} – 1.0 V.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = 3.4 V, V2 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when setting V2 = 0.03 V and when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL}.

3. Alarm status detection voltage (Test circuit 1)

Alarm status detection voltage (V_{AU}) is defined as the voltage V1 at which V_{AO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = 3.4 V.

Caution Be sure to connect R_{AO} between the V1 and AO pin when measuring V_{AU} on an Nch open-drain output product.

4. Discharge overcurrent detection voltage, discharge overcurrent release voltage (Test circuit 2)

Discharge overcurrent detection voltage (V_{DIOV}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time (t_{DIOV}) when the voltage V2 is increased after setting V1 = 3.4 V, V2 = 0 V. Discharge overcurrent release voltage (V_{RIOV}) is defined as the voltage V2 at which V_{DO} goes from "L" to "H" when setting V2 = 3.4 V and when the voltage V2 is then gradually decreased.

5. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}) when the voltage V2 is increased after setting V1 = 3.4 V, V2 = 0 V.

6. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V2 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}) when the voltage V2 is decreased after setting V1 = 3.4 V, V2 = 0 V.

7. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.4 V, V2 = 0 V.

8. Current consumption during power-down, current consumption during overdischarge (Test circuit 3)

8. 1 With power-down function

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V.

8. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V.

9. Resistance between VDD pin and VM pin (Test circuit 3)

R_{VMD} is the resistance between VDD pin and VM pin under the set conditions of V1 = 1.8 V, V2 = 0 V.

10. Resistance between VM pin and VSS pin (Test circuit 3)

R_{VMS} is the resistance between VM pin and VSS pin under the set conditions of V1 = 3.4 V, V2 = 1.0 V.

11. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V3 = 3.0 V.

12. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 0 V, V3 = 0.4 V.

13. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V4 = 3.0 V.

14. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.4 V.

15. AO pin resistance "H" (Test circuit 4)

The AO pin resistance "H" (R_{AOH}) is the resistance between VDD pin and AO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V5 = 3.0 V (CMOS output product only).

16. AO pin resistance "L" (Test circuit 4)

The AO pin resistance "L" (R_{AOL}) is the resistance between VSS pin or VM pin and AO pin under the set conditions of $V_{AU} < V1 < V_{CU}$, V2 = 0 V, V5 = 0.4 V.

17. Overcharge detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V1 is increased. The time interval from when the voltage V1 exceeds V_{CU} until V_{CO} goes to "L" is the overcharge detection delay time (t_{CU}).

18. Overdischarge detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V1 is decreased. The time interval from when the voltage V1 falls below V_{DL} until V_{DO} goes to "L" is the overdischarge detection delay time (t_{DL}).

19. Alarm status detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V1 is increased. The time interval from when the voltage V1 exceeds V_{AU} until V_{AO} goes to "L" is the alarm status detection delay time (t_{AU}).

Caution Be sure to connect R_{AO} between the V1 and AO pin when measuring t_{AU} on an Nch open-drain output product.

20. Discharge overcurrent detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V2 is increased. The time interval from when the voltage V2 exceeds V_{DIOV} until V_{DO} goes to "L" is the discharge overcurrent detection delay time (t_{DIOV}).

21. Load short-circuiting detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V2 is increased. The time interval from when the voltage V2 exceeds V_{SHORT} until V_{DO} goes to "L" is the load short-circuiting detection delay time (t_{SHORT}).

22. Charge overcurrent detection delay time (Test circuit 5)

After setting V1 = 3.4 V, V2 = 0 V, the voltage V2 is decreased. The time interval from when the voltage V2 falls below V_{CIOV} until V_{CO} goes to "L" is the charge overcurrent detection delay time (t_{CIOV}).

23. 0 V battery charge starting charger voltage (0 V battery charge enabled) (Test circuit 4)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V2 at which the current flowing through the CO pin (I_{CO}) exceeds 1.0 μA when the voltage V2 is gradually decreased after setting V1 = 0 V, V2 = V3 = −0.5 V.

24. 0 V battery charge inhibition battery voltage (0 V battery charge inhibited) (Test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage V1 at which V_{CO} goes to "L" (V_{CO} = V_{VM}) when the voltage V1 is gradually decreased after setting V1 = 1.8 V, V2 = −2.0 V.

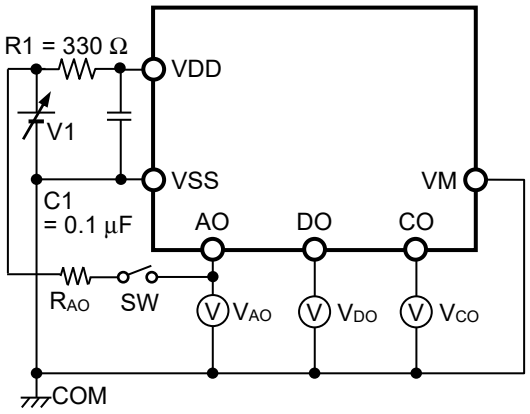


Figure 6 Test Circuit 1

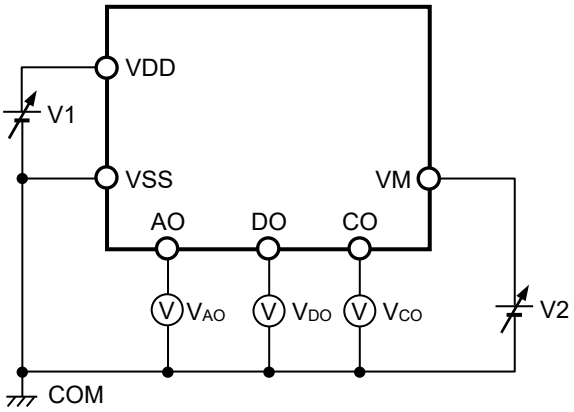


Figure 7 Test Circuit 2

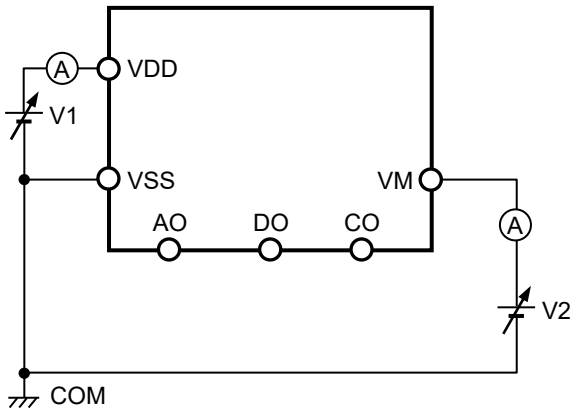


Figure 8 Test Circuit 3

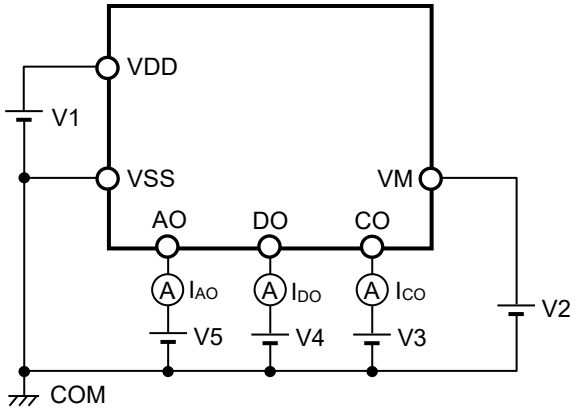


Figure 9 Test Circuit 4

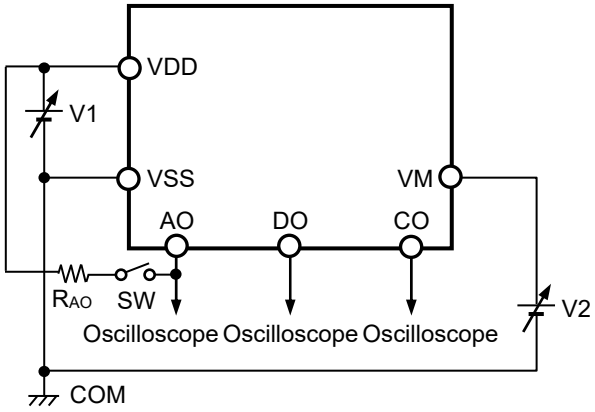


Figure 10 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

1. Normal status

The S-82L1A Series monitors the voltage of the battery connected between VDD pin and VSS pin, the voltage between VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to alarm status detection voltage (V_{AU}), and the VM pin voltage is in the range from charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent detection voltage (V_{DIOV}), the S-82L1A Series turns both the charge and discharge control FETs on. This status is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between VDD pin and VM pin (R_{VMD}), and the resistance between VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

Caution After the battery is connected, discharging may not be carried out. In this case, the S-82L1A Series returns to the normal status by connecting a charger.

2. Overcharge status

2. 1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, the S-82L1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is lower than 0.35 V typ., the S-82L1A Series releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is equal to or higher than 0.35 V typ., the S-82L1A Series releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82L1A Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2 V_{CL} = V_{CU} (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for t_{CU} or longer, the S-82L1A Series turns the charge control FET off to stop charging. This status is called the overcharge status.
In the case that the VM pin voltage is equal to or higher than 0.35 V typ. and the battery voltage falls below V_{CU}, the S-82L1A Series releases the overcharge status.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the internal parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than 0.35 V typ., the S-82L1A Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL}. The overcharge status is released when the discharge current flows and the VM pin voltage goes over 0.35 V typ. by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, the S-82L1A Series turns the discharge control FET off to stop discharging. This status is called the overdischarge status.
Under the overdischarge status, VDD pin and VM pin are shorted by R_{VMD} in the S-82L1A Series. The VM pin voltage is pulled up by R_{VMD}.
When connecting a charger in the overdischarge status, the battery voltage reaches V_{DL} or higher and the S-82L1A Series releases the overdischarge status if the VM pin voltage is below 0 V typ.
The battery voltage reaches the overdischarge release voltage (V_{DU}) or higher and the S-82L1A Series releases the overdischarge status if the VM pin voltage is not below 0 V typ.
R_{VMS} is not connected in the overdischarge status.

3. 1 With power-down function

Under the overdischarge status, when the VM pin voltage is 0.7 V typ. or higher, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

- When a battery is not connected to a charger and the VM pin voltage ≥ 0.7 V typ., the S-82L1A Series maintains the overdischarge status even when the battery voltage reaches V_{DU} or higher.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and the S-82L1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM pin voltage, the battery voltage reaches V_{DL} or higher and the S-82L1A Series releases the overdischarge status.

3. 2 Without power-down function

Under the overdischarge status, the power-down function does not work even when the VM pin voltage is 0.7 V typ. or higher.

- When a battery is not connected to a charger and the VM pin voltage ≥ 0.7 V typ., the battery voltage reaches V_{DU} or higher and the S-82L1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0.7 V typ. > the VM pin voltage > 0 V typ., the battery voltage reaches V_{DU} or higher and the S-82L1A Series releases the overdischarge status.
- When a battery is connected to a charger and 0 V typ. ≥ the VM pin voltage, the battery voltage reaches V_{DL} or higher and the S-82L1A Series releases the overdischarge status.

4. Alarm status

When the battery voltage becomes higher than the alarm status detection voltage (V_{AU}) during charging in the normal status and the condition continues for the alarm status detection delay time (t_{AU}) or longer, the AO pin outputs an alarm signal. This status is called the alarm status.
The S-82L1A Series releases the alarm status when the battery voltage falls below V_{AU} or when an overcharge status is detected.

Caution If the alarm status continues for 20 s typ. or longer, the charge control FET is turned off and charging is stopped.
In this case, the S-82L1A Series releases the alarm status.

5. Discharge overcurrent status (discharge overcurrent, load short- circuiting)

When a battery in the normal status is in the status where the VM pin voltage is equal to or higher than V_{DIOV} because the discharge current is equal to or higher than the specified value and the status continues for the discharge overcurrent detection delay time (t_{DIOV}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in the S-82L1A Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, the VM pin voltage returns to the VSS pin voltage.
When the VM pin voltage returns to V_{RIOV} or lower, the S-82L1A Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

6. Charge overcurrent status

When a battery in the normal status is in the status where the VM pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status continues for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-82L1A Series releases the charge overcurrent status when the discharge current flows and the VM pin voltage is 0.35 V typ. or higher by removing the charger.
The charge overcurrent detection does not function in the overdischarge status.

7. 0 V battery charge enabled

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.
When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DL}, the S-82L1A Series returns to the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.
2. The 0 V battery charge has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

8. 0 V battery charge inhibited

This function inhibits charging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged lithium-ion rechargeable battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge.

9. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV} and t_{SHORT} start when V_{DIOV} is detected. When V_{SHORT} is detected over t_{SHORT} after the detection of V_{DIOV}, the S-82L1A Series turns the discharge control FET off within t_{SHORT} of each detection.

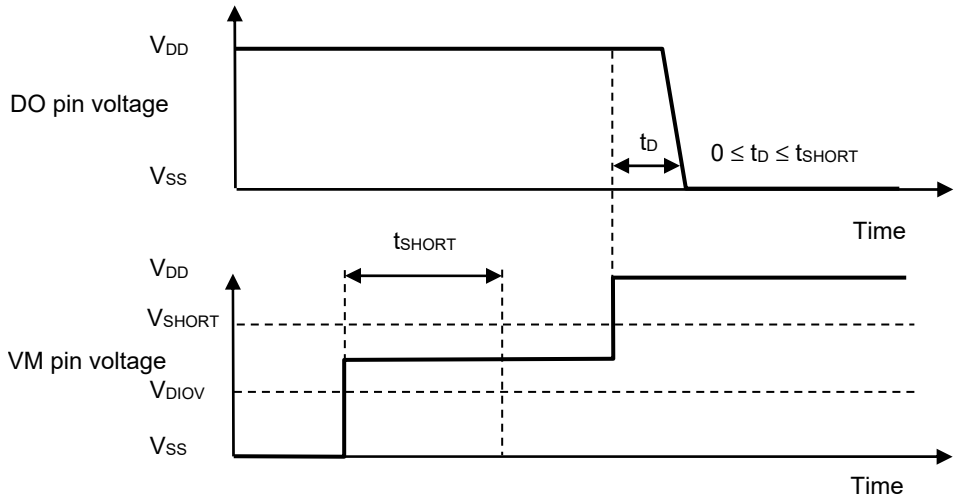
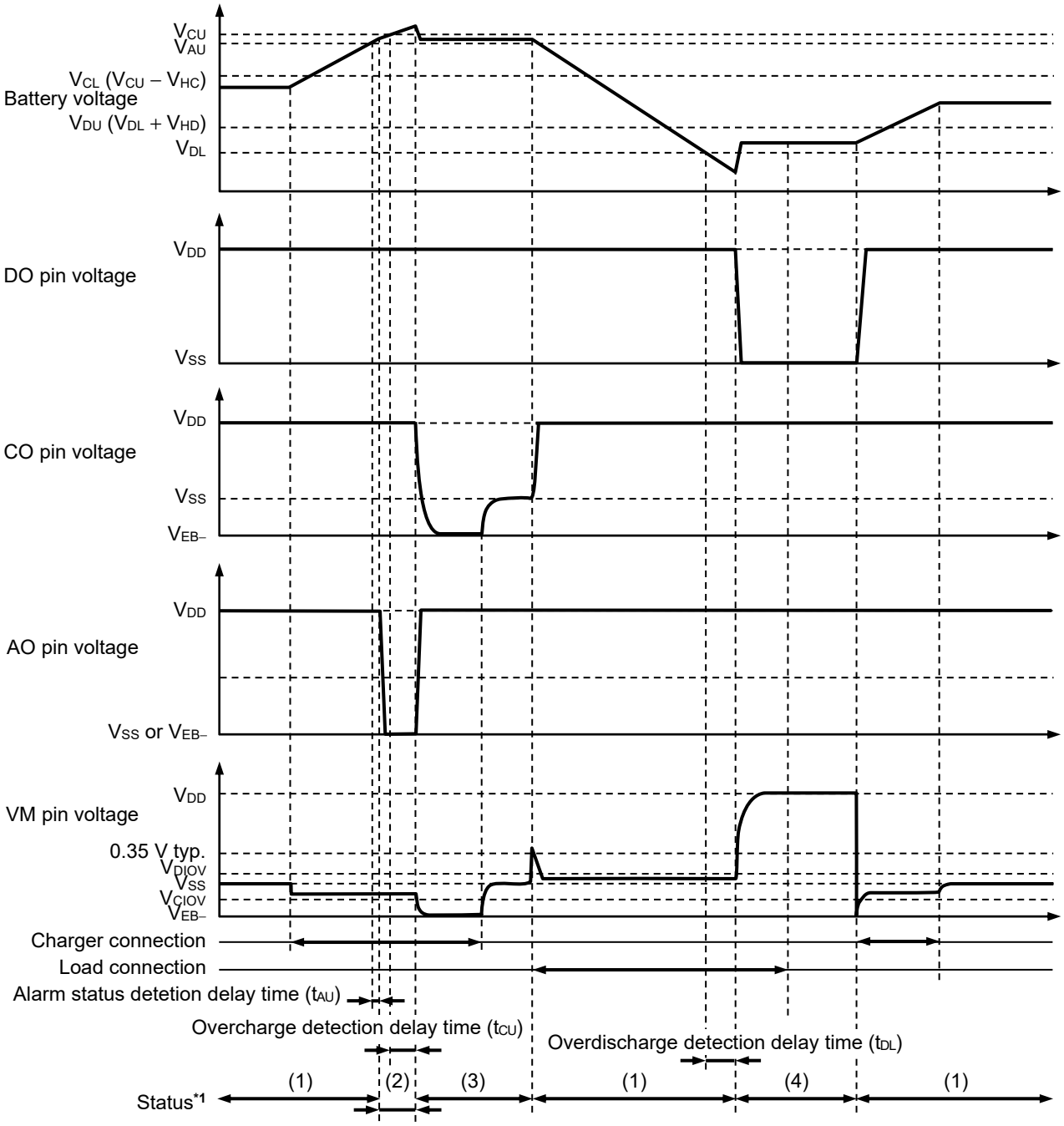


Figure 11

■ Timing Charts

1. Overcharge detection, overdischarge detection

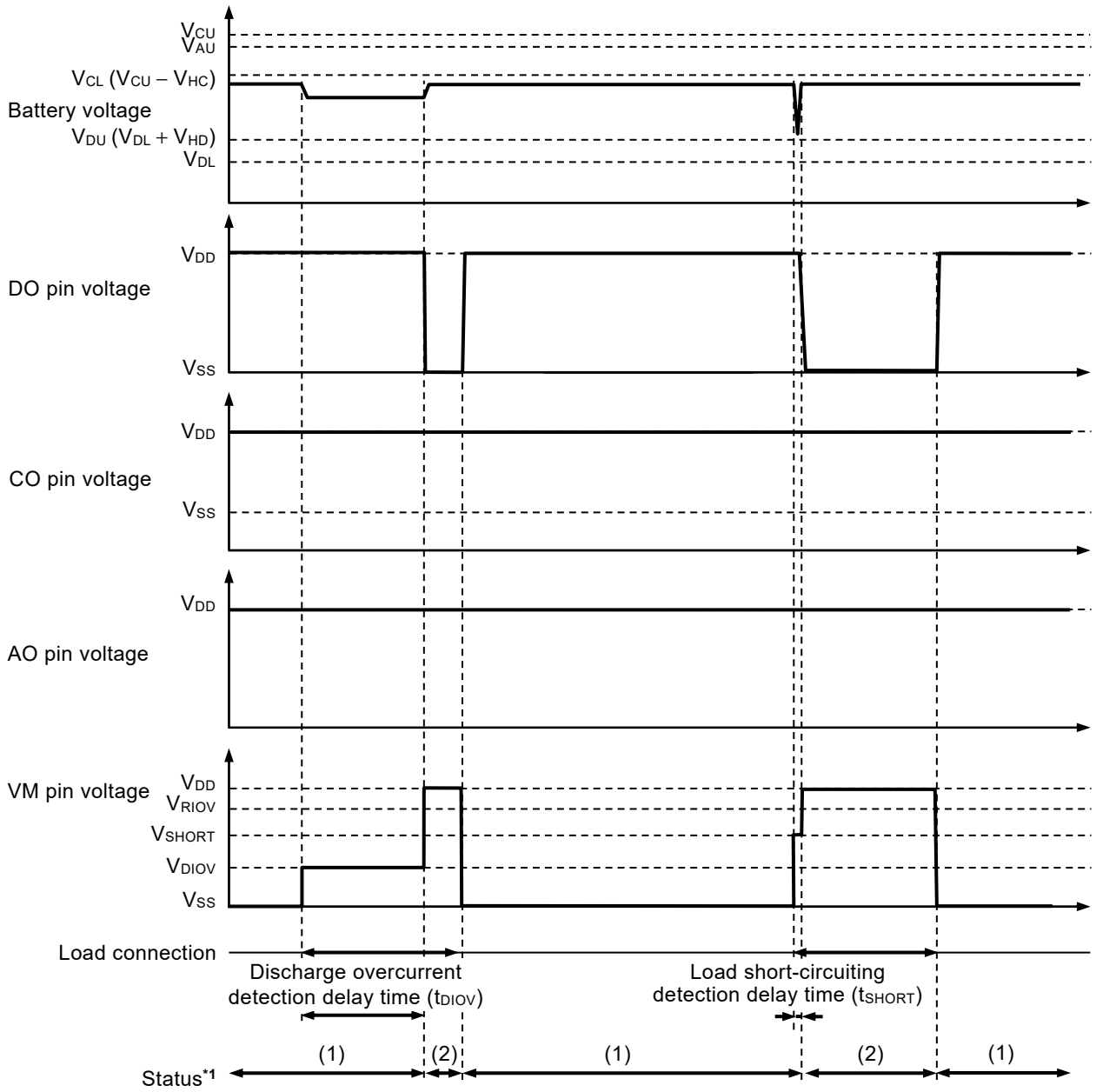


***1.** (1): Normal status
(2): Alarm status
(3): Overcharge status
(4): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 12

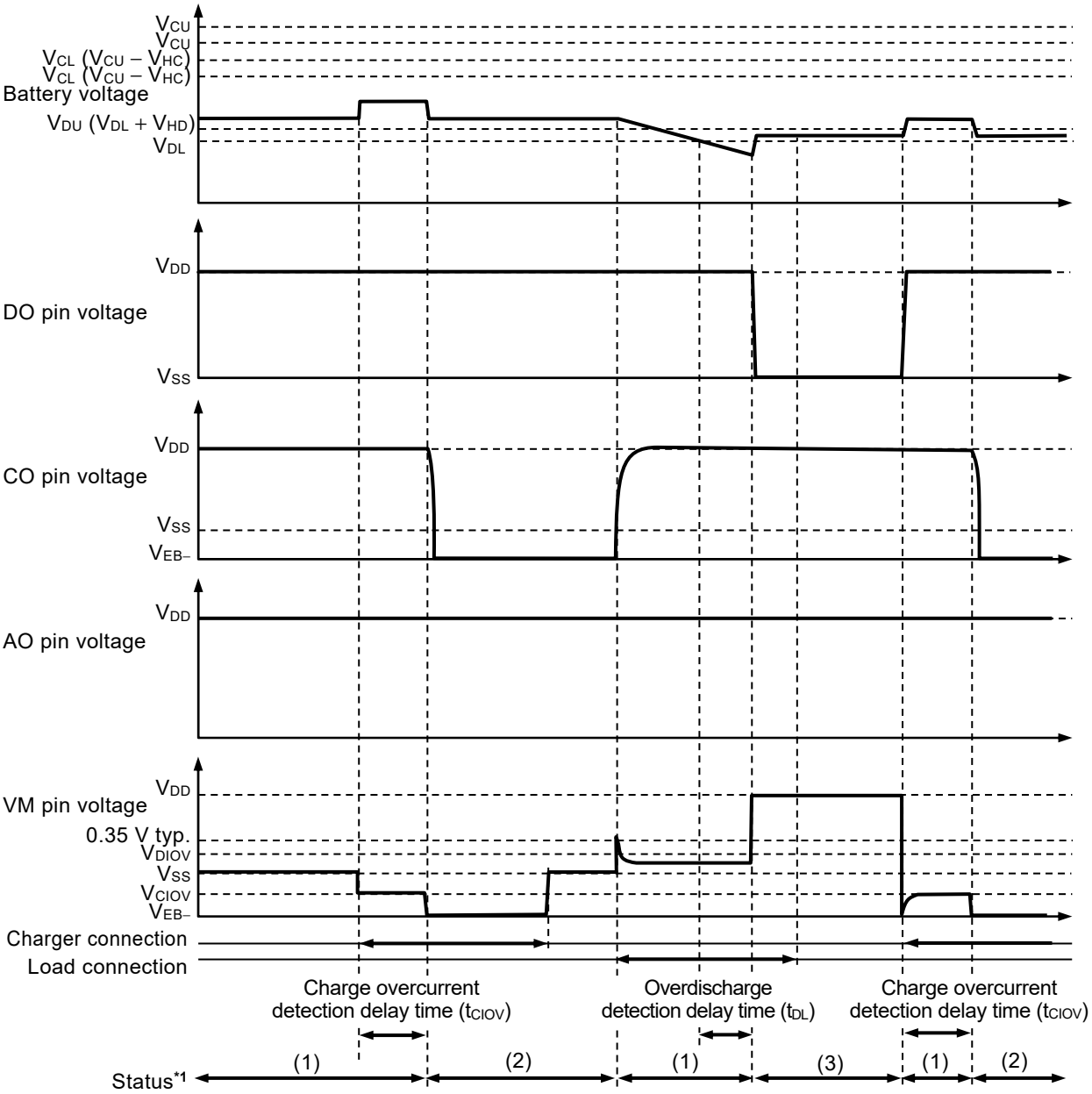
2. Discharge overcurrent detection



***1.** (1): Normal status
(2): Discharge overcurrent status

Figure 13

3. Charge overcurrent detection



***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 14

■ Battery Protection IC Connection Example

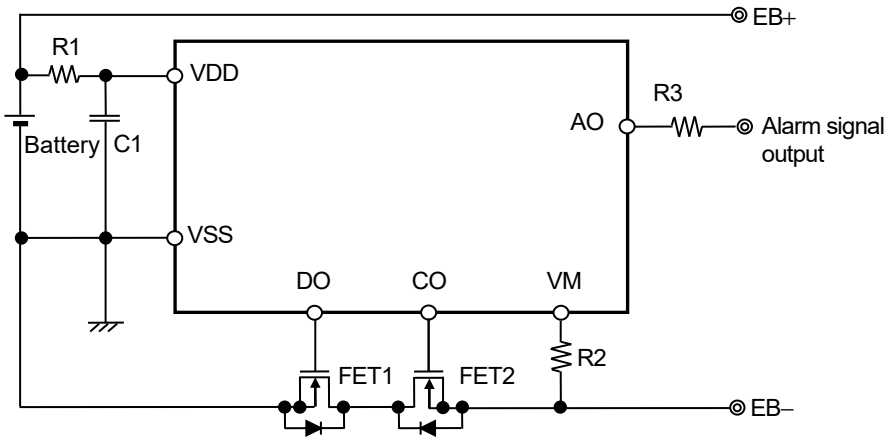


Figure 15

Table 11 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
FET1	Nch MOS FET	Discharge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
FET2	Nch MOS FET	Charge control	–	–	–	Threshold voltage ≤ Overdischarge detection voltage*1
R1	Resistor	ESD protection, For power fluctuation	270 Ω	330 Ω	1.0 kΩ*2	–
C1	Capacitor	For power fluctuation	0.1 μF	0.1 μF	1.0 μF	–
R2	Resistor	ESD protection, Protection for reverse connection of a charger	300 Ω	470 Ω	750 Ω	–
R3	Resistor	ESD protection	–	1.0 kΩ	–	–

***1.** If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** Accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values will worsen the accuracy.

Caution 1. The constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

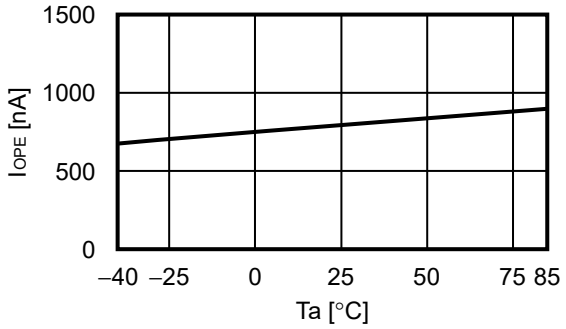
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

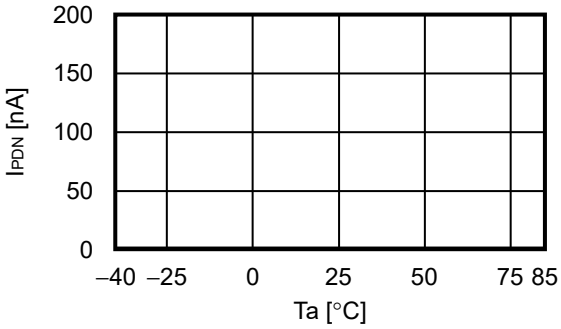
■ Characteristics (Typical Data)

1. Current consumption

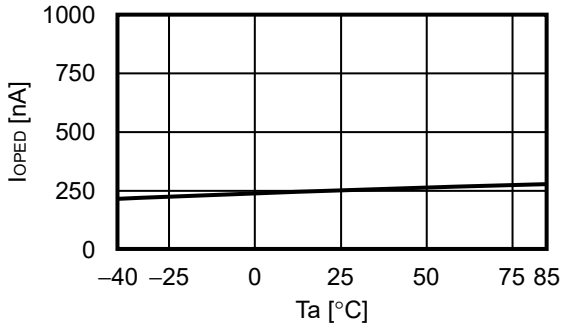
1. 1 I_{OPE} vs. Ta



1. 2 I_{PDN} vs. Ta

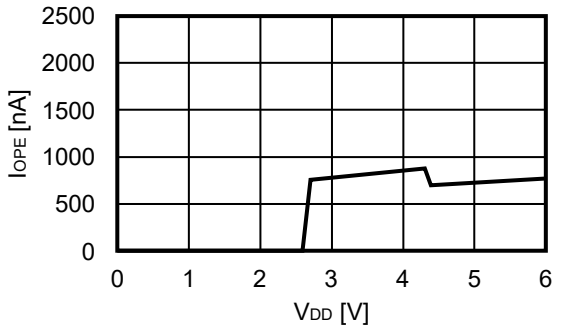


1. 3 I_{OPED} vs. Ta

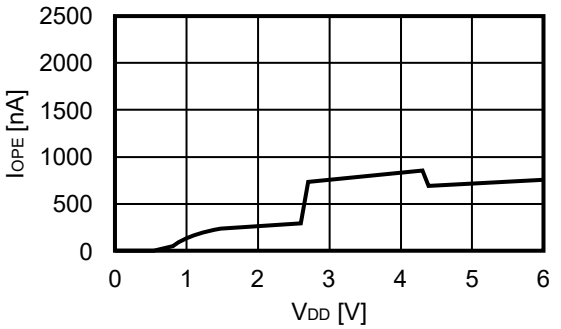


1. 4 I_{OPE} vs. V_{DD}

1. 4. 1 With power-down function

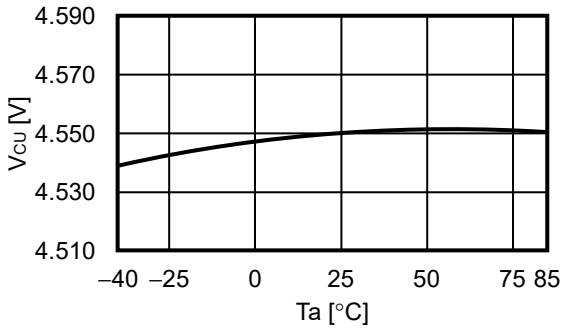


1. 4. 2 Without power-down function

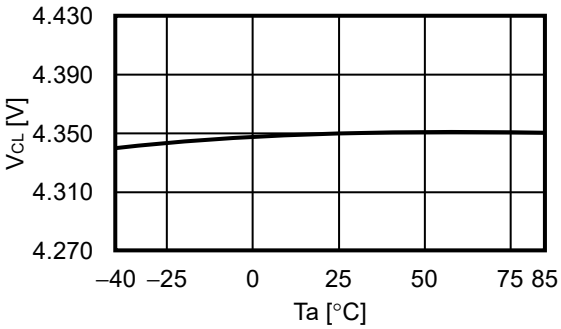


2. Detection voltage

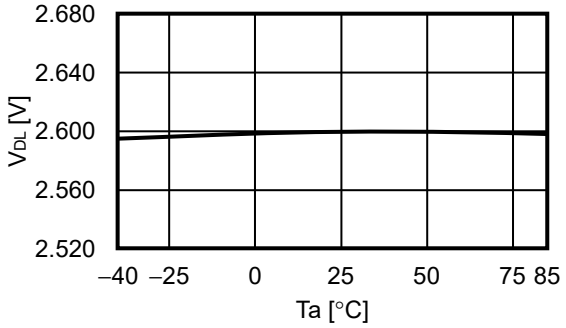
2. 1 V_{CU} vs. Ta



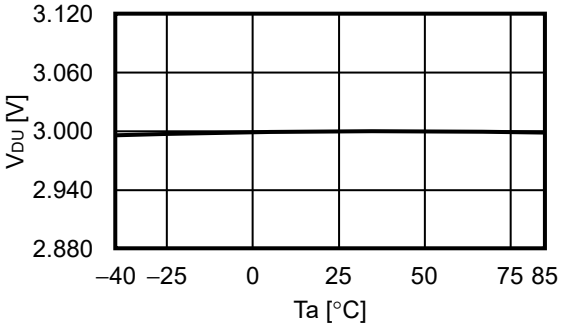
2. 2 V_{CL} vs. Ta



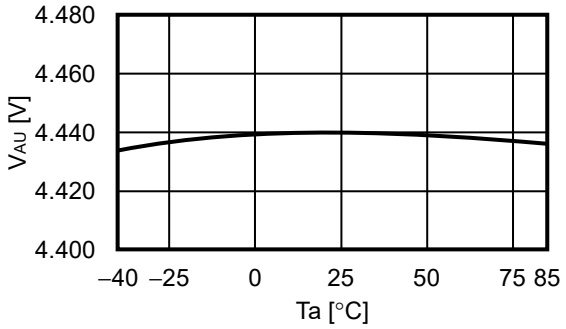
2. 3 V_{DL} vs. Ta



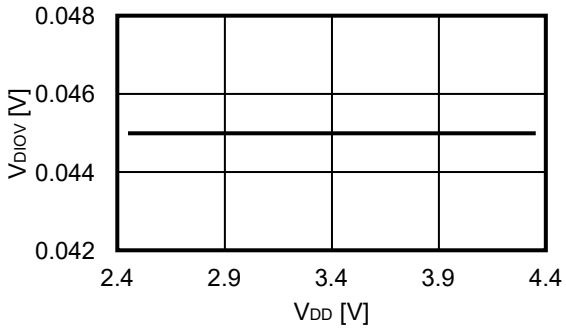
2. 4 V_{DU} vs. Ta



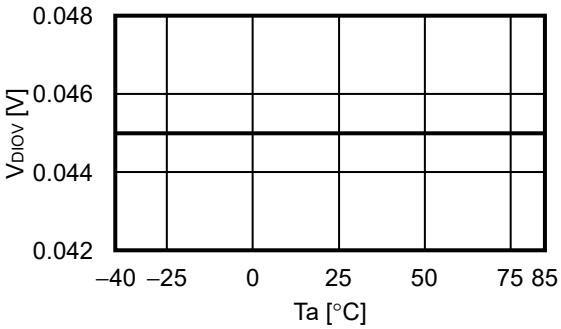
2. 5 V_{AU} vs. Ta



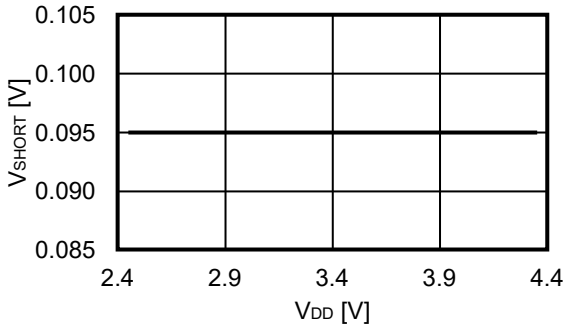
2. 6 V_{DIOV} vs. V_{DD}



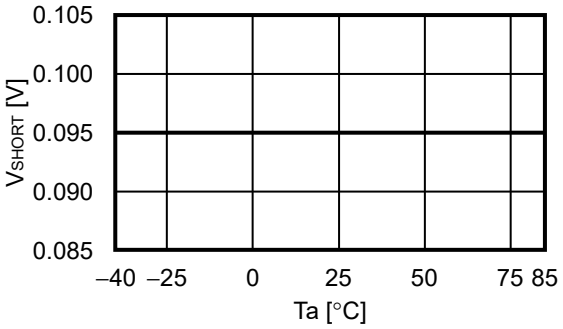
2. 7 V_{DIOV} vs. Ta



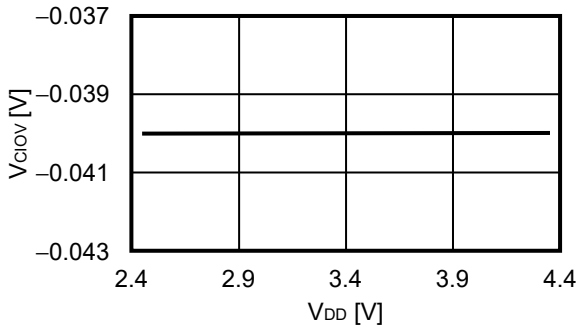
2. 8 V_{SHORT} vs. V_{DD}



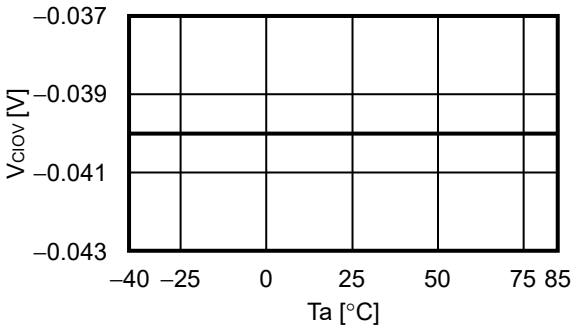
2. 9 V_{SHORT} vs. Ta



2. 10 V_{CIOV} vs. V_{DD}

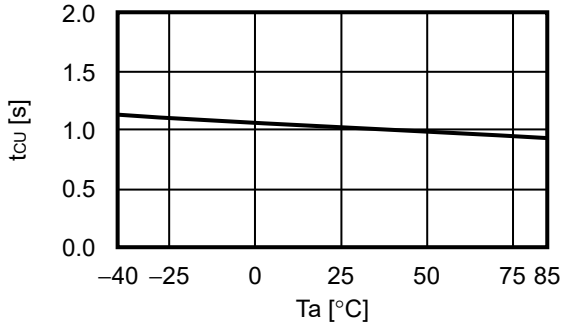


2. 11 V_{CIOV} vs. Ta

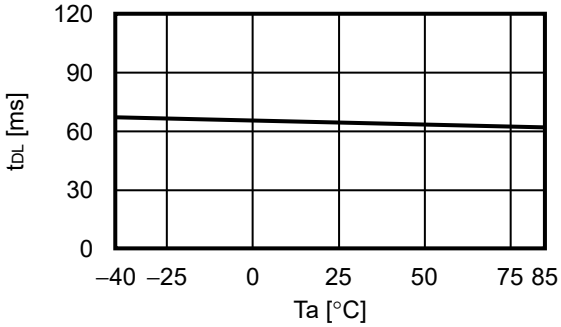


3. Delay time

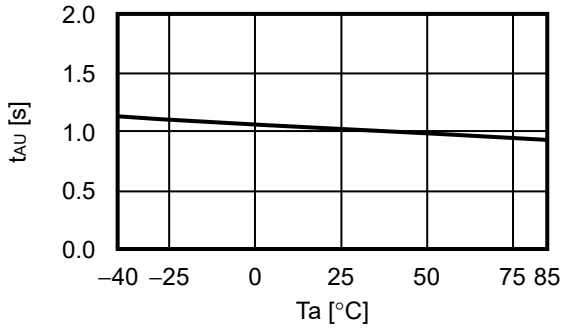
3. 1 t_{CU} vs. Ta



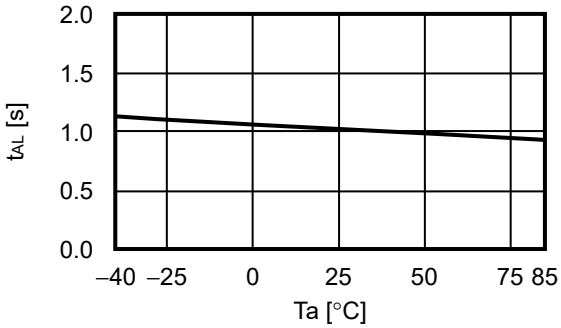
3. 2 t_{DL} vs. Ta



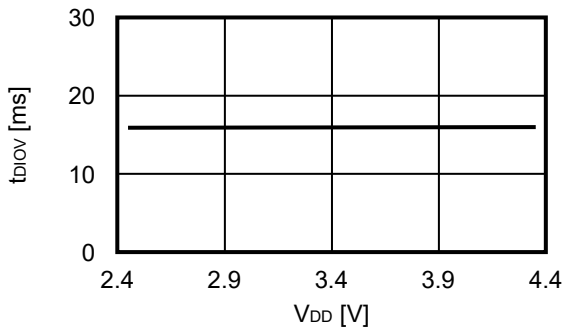
3. 3 t_{AU} vs. Ta



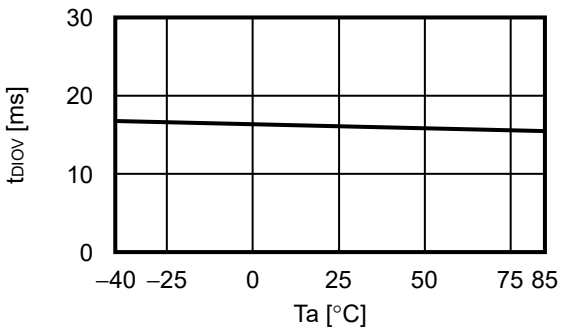
3. 4 t_{AL} vs. Ta



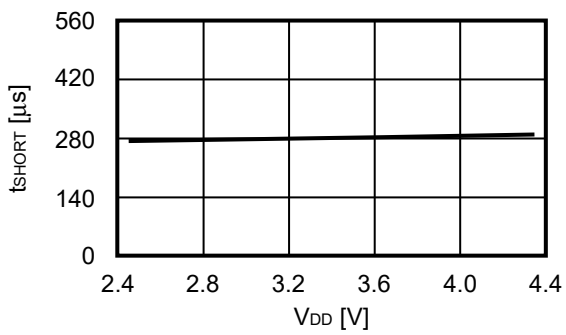
3. 5 t_{DIOV} vs. V_{DD}



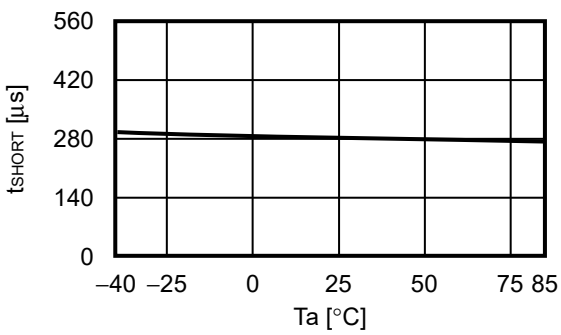
3. 6 t_{DIOV} vs. Ta



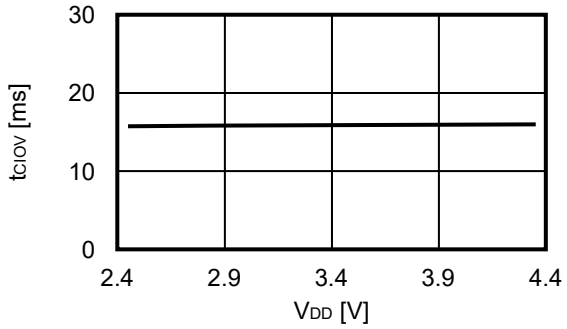
3. 7 t_{SHORT} vs. V_{DD}



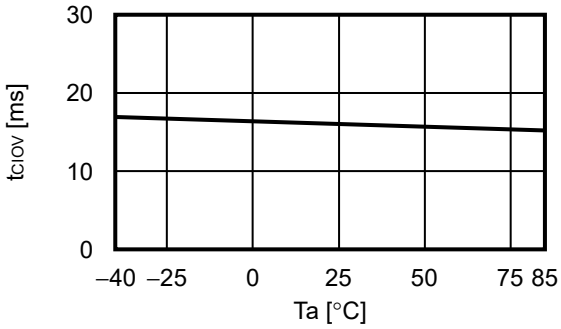
3. 8 t_{SHORT} vs. Ta



3. 9 t_{CIOV} vs. V_{DD}

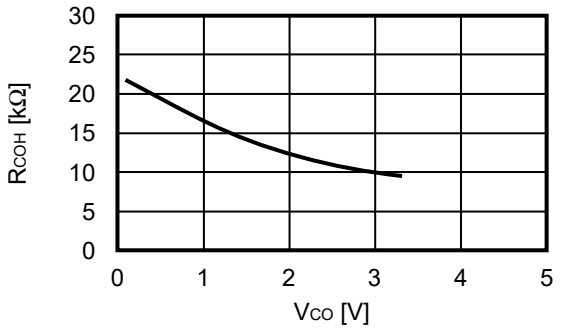


3. 10 t_{CIOV} vs. Ta

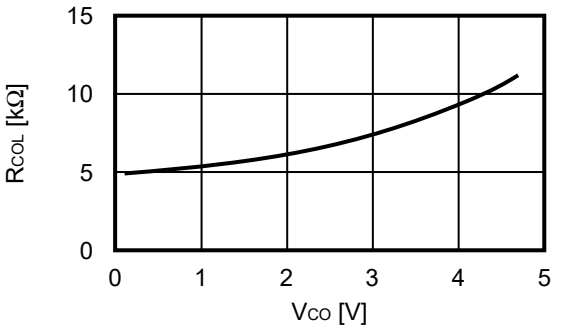


4. Output resistance

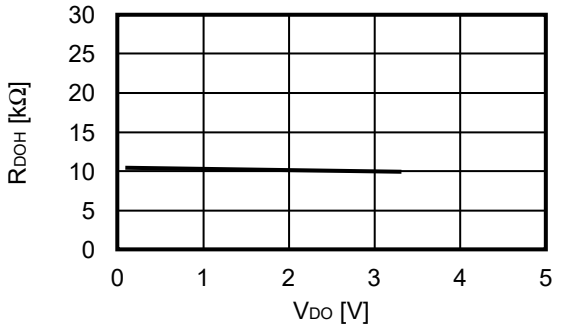
4. 1 R_{COH} vs. V_{CO}



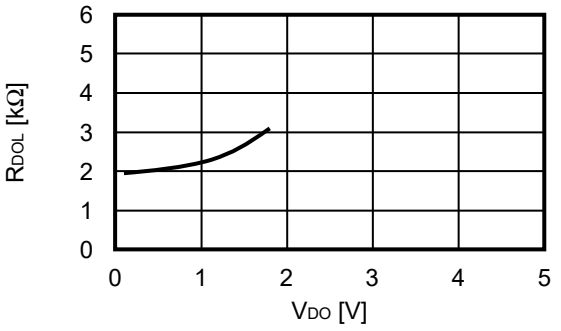
4. 2 R_{COL} vs. V_{CO}



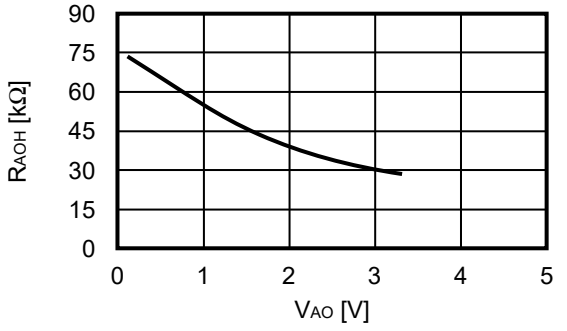
4. 3 R_{DOH} vs. V_{DO}



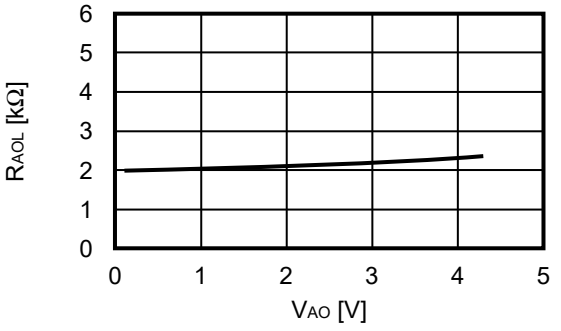
4. 4 R_{DOL} vs. V_{DO}



4. 5 R_{AOH} vs. V_{AO}



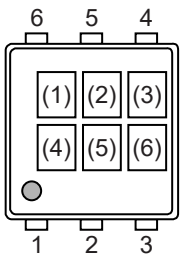
4. 6 R_{AOL} vs. V_{AO}



■ Marking Specifications

1. SNT-6A

Top view



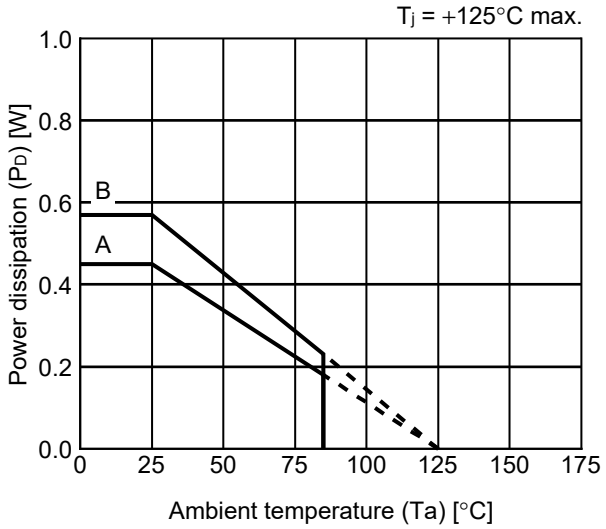
(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-82L1AAA-I6T1U7	8	L	A

■ Power Dissipation

SNT-6A

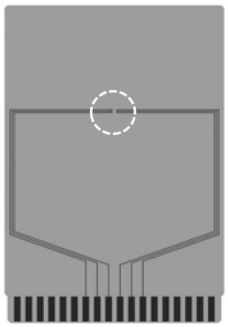


Board	Power Dissipation (P_D)
A	0.45 W
B	0.57 W
C	–
D	–
E	–

SNT-6A Test Board

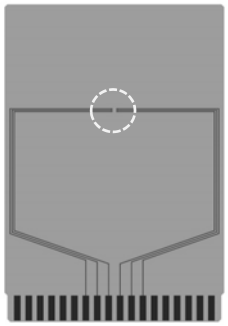
(1) Board A

IC Mount Area



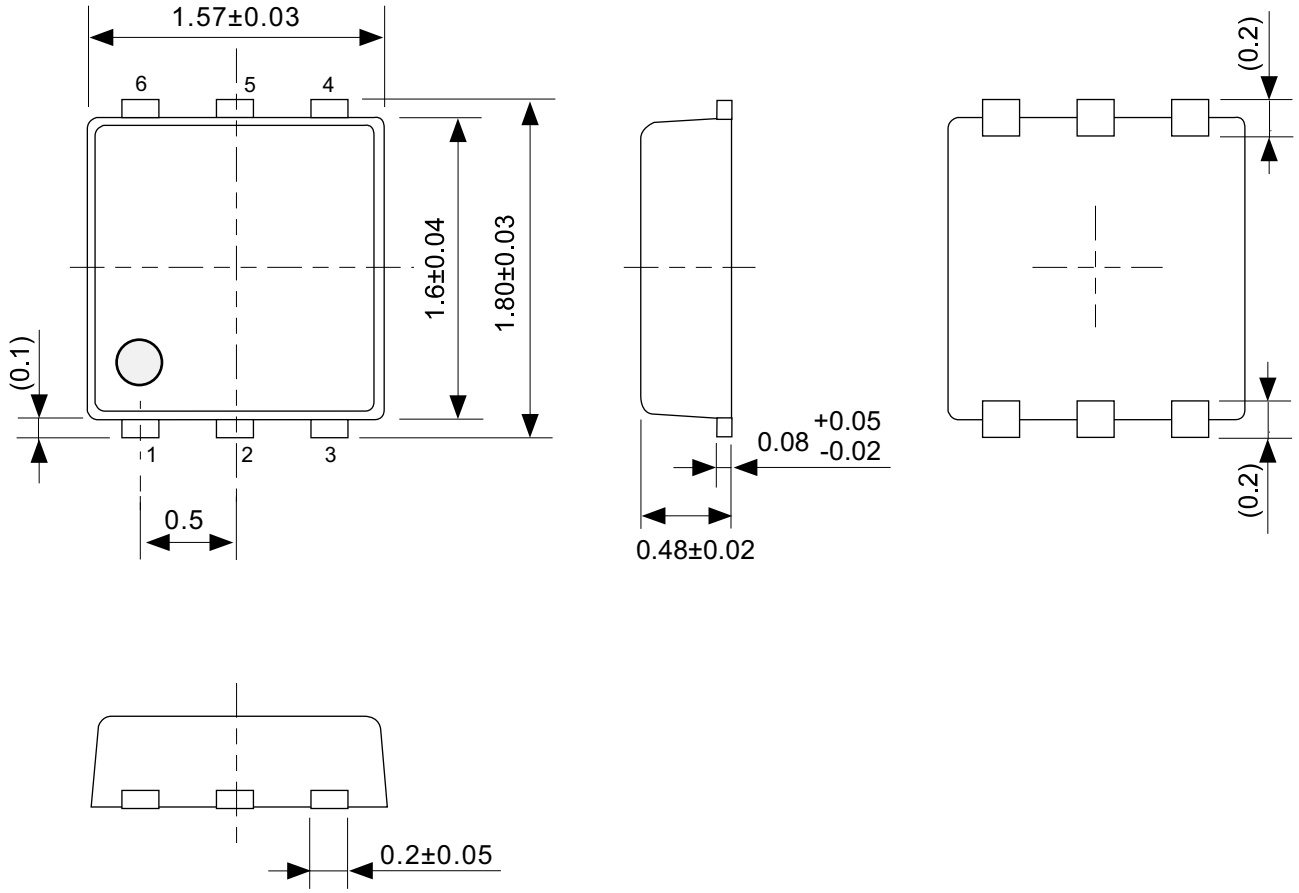
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



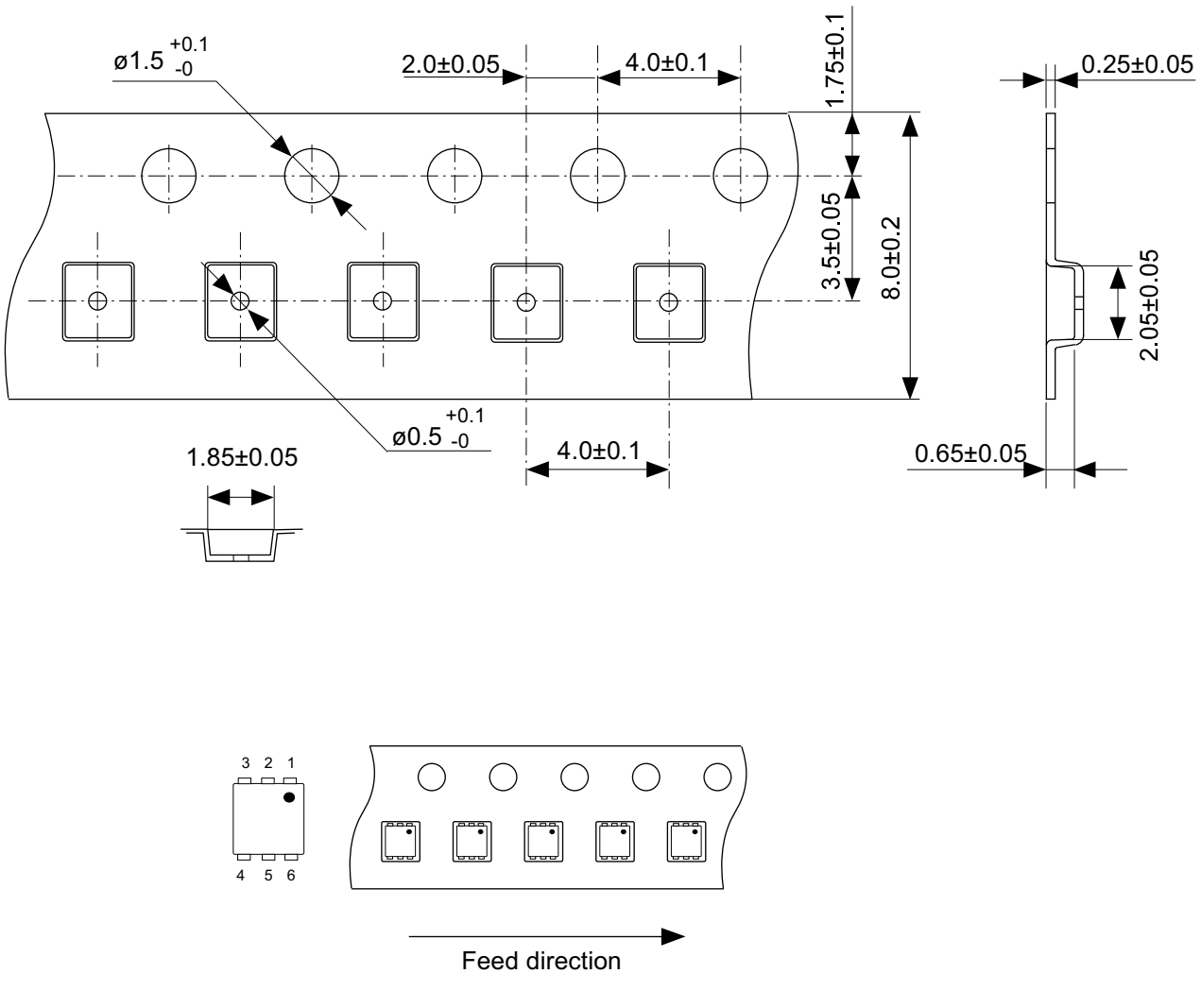
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SNT6A-A-Board-SD-1.0



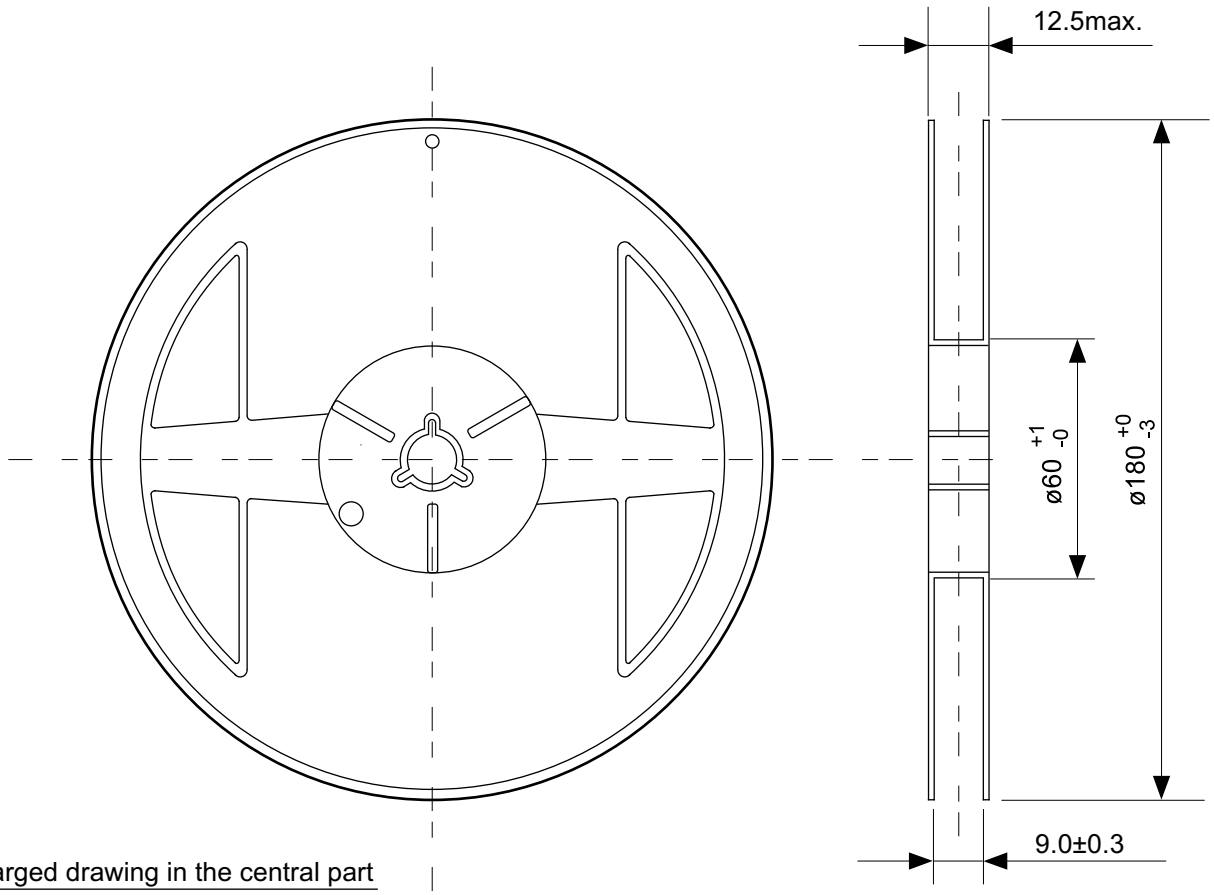
No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

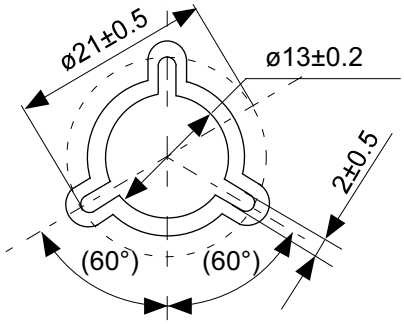


No. PG006-A-C-SD-2.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

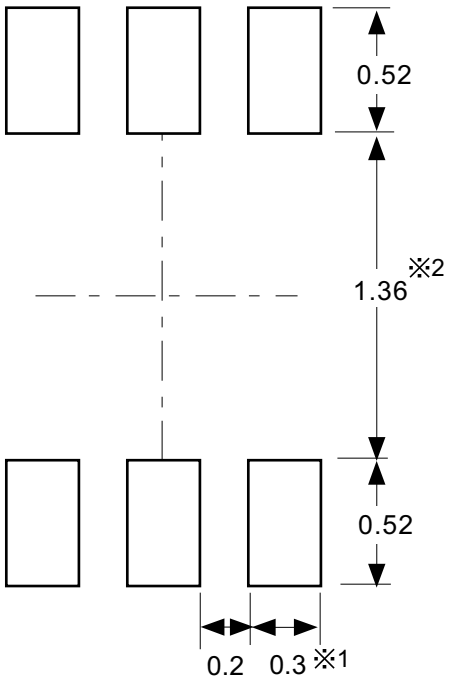


Enlarged drawing in the central part



No. PG006-A-R-SD-1.0

TITLE	SNT-6A-A-Reel		
No.	PG006-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から**0.03 mm** 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝**SNT**パッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.30 mm ~ 1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PG006-A-L-SD-4.1

TITLE	SNT-6A-A -Land Recommendation
No.	PG006-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ABLIC:
S-82L1AAA-I6T1U7