ABLIC

S-82H4 Series

BATTERY PROTECTION IC FOR 3-SERIAL OR 4-SERIAL CELL PACK WITH CONSTANT VOLTAGE OUTPUT PIN FOR REAL-TIME CLOCK (SECONDARY PROTECTION)

www.ablic.com

Rev.1.3_00

This IC is used for secondary protection of lithium-ion rechargeable batteries, and incorporates high-accuracy voltage detection circuits and delay circuits.
Short-circuiting between the VC1 and VC2 pins makes it possible to serially connect three cells.
Since this IC also comes with a constant voltage output circuit, it can be used as a constant-voltage power supply for an external RTC (Real-Time clock IC).

■ Features

- High-accuracy voltage detection circuit for each cell

Overcharge detection voltage n	3.600 V to 4.800 V (5 mV step)	Accuracy ±15 mV (Ta = +25°C)
		Accuracy ±25 mV (Ta = −10°C to +60°C)
Overcharge release voltage n*1	3.600 V to 4.800 V	Accuracy ±50 mV
VRTC pin shutdown voltage n	2.500 V to 2.800 V (100 mV step)	Accuracy ±50 mV

- Delay times for overcharge detection are generated only by an internal circuit (external capacitors are unnecessary)
  Overcharge detection delay time, VRTC pin shutdown delay time: 1 s, 2 s, 4 s, 6 s
- Overcharge timer reset function: Available, unavailable
- CO pin output voltage is limited to 7.5 V max.
- VRTC pin output voltage: 1.800 V to 3.300 V (100 mV step) Accuracy ±2% (Ta = +25°C)
- VRTC pin output current: 2 mA max.
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  During operation (V_{CU} − 1.0 V for each cell): 4.0 μA max.
  During VRTC pin shutdown (V_{RSD} − 1.0 V for each cell): 1.0 μA max.
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 mV to 400 mV in 50 mV step.)

Remark **1.** The order of battery connection of this IC is limited. Customers who desire a product that does not limit the order of battery connection should consider the S-82K3/K4 Series of products instead.
2. n = 1, 2, 3, 4

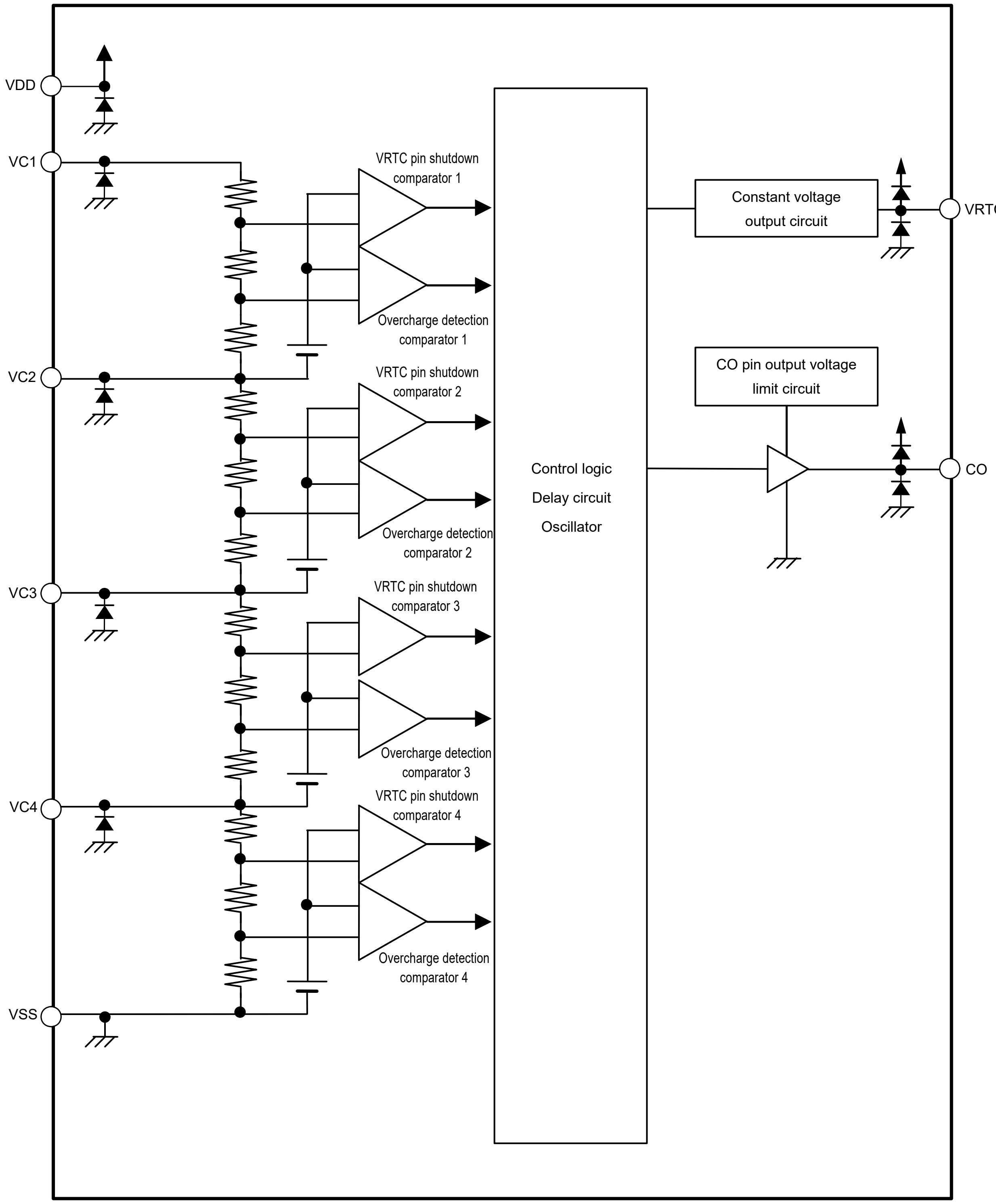
■ Application

- Lithium-ion rechargeable battery packs (for secondary protection)

■ Packages

- DFN-8(2020)A
- HSNT-8(1616)

■ Block Diagrams



Remark Diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-82H4 xxx - xxxx U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx: Package abbreviation and IC packing specifications*1
  - A8T8: DFN-8(2020)A, Tape
  - A8T2: HSNT-8(1616), Tape
- xxx: Serial code*2
  - Sequentially set from AAA to ZZZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
DFN-8(2020)A	IB008-A-P-SD	IB008-A-C-SD	IB008-A-R-SD	IB008-A-L-SD
HSNT-8(1616)	PY008-A-P-SD	PY008-A-C-SD	PY008-A-R-SD	PY008-A-L-SD

3. Product name list

3. 1 DFN-8(2020)A

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	VRTC Pin Output Voltage [V_{VRTC}]	VRTC Pin Shutdown Voltage [V_{RSD}]	VRTC Pin Recovery Voltage [V_{RST}]	Overcharge Detection Delay Time*1 [t_{CU}]	VRTC Pin Shutdown Delay Time*1 [t_{RSD}]	Overcharge Timer Reset Function*2
S-82H4AAA-A8T8U	4.600 V	4.300 V	3.300 V	2.500 V	2.700 V	6 s	6 s	Unavailable
S-82H4AAB-A8T8U	4.600 V	4.300 V	3.000 V	2.500 V	2.700 V	6 s	6 s	Unavailable
S-82H4AAC-A8T8U	4.650 V	4.350 V	3.300 V	2.500 V	2.700 V	6 s	6 s	Unavailable
S-82H4AAD-A8T8U	4.650 V	4.350 V	3.000 V	2.500 V	2.700 V	6 s	6 s	Unavailable
S-82H4AAE-A8T8U	4.550 V	4.300 V	3.300 V	2.500 V	2.700 V	6 s	6 s	Unavailable

***1.** Overcharge detection delay time, VRTC pin shutdown delay time: 1 s, 2 s, 4 s, 6 s
***2.** Overcharge timer reset function: Available, unavailable

Remark Please contact our sales representatives for products other than the above.

3. 2 HSNT-8(1616)

Table 3

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	VRTC Pin Output Voltage [V_{VRTC}]	VRTC Pin Shutdown Voltage [V_{RSD}]	VRTC Pin Recovery Voltage [V_{RST}]	Overcharge Detection Delay Time*1 [t_{CU}]	VRTC Pin Shutdown Delay Time*1 [t_{RSD}]	Overcharge Timer Reset Function*2
S-82H4AAA-A8T2U	4.600 V	4.300 V	3.300 V	2.500 V	2.700 V	6 s	6 s	Unavailable

***1.** Overcharge detection delay time, VRTC pin shutdown delay time: 1 s, 2 s, 4 s, 6 s
***2.** Overcharge timer reset function: Available, unavailable

Remark Please contact our sales representatives for products other than the above.

■ Pin Configuration

1. DFN-8(2020)A

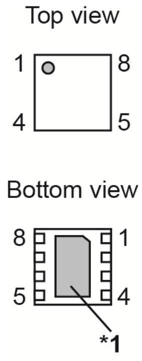


Figure 2

Table 4

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin
2	VC1	Positive power supply input pin Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VSS	Negative power supply input pin Negative voltage connection pin of battery 4
7	CO	FET gate connection pin for charge control
8	VRTC	Voltage output pin for Real-time Clock (RTC)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open or V_{C1}.
However, do not use it as the function of electrode.

2. HSNT-8(1616)

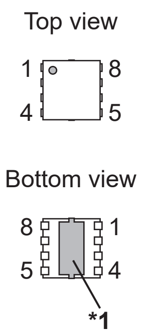


Figure 3

Table 5

Pin No.	Symbol	Description
1	VDD	Positive power supply input pin
2	VC1	Positive power supply input pin Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1 Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2 Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3 Positive voltage connection pin of battery 4
6	VSS	Negative power supply input pin Negative voltage connection pin of battery 4
7	CO	FET gate connection pin for charge control
8	VRTC	Voltage output pin for Real-time Clock (RTC)

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential open or V_{C1}.
However, do not use it as the function of electrode.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS1}	VDD	V_{SS} – 0.3 to V_{SS} + 28	V
Input voltage between VC1 pin and VSS pin	V_{DS2}	VC1	V_{SS} – 0.3 to V_{SS} + 28	V
Input pin voltage	V_{IN}	VC2, VC3, VC4	V_{SS} – 0.3 to V_{VC1} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
VRTC pin output voltage	V_{VRTC}	VRTC	V_{SS} – 0.3 to V_{SS} + 6	V
Operation ambient temperature	T_{opr}	–	–40 to +85	°C
Storage temperature	T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	DFN-8(2020)A	Board A	–	242	–	°C/W
			Board B	–	182	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-8(1616)	Board A	–	214	–	°C/W
			Board B	–	172	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n (n = 1, 2, 3, 4)	V_{CUn}	Ta = +25°C	V_{CU} − 0.015	V_{CU}	V_{CU} + 0.015	V	1
		Ta = −10°C to +60°C*1	V_{CU} − 0.020	V_{CU}	V_{CU} + 0.020	V	1
Overcharge release voltage n (n = 1, 2, 3, 4)	V_{CLn}	−	V_{CL} − 0.050	V_{CL}	V_{CL} + 0.050	V	1
VRTC pin shutdown voltage n (n = 1, 2, 3, 4)	V_{RSDn}	−	V_{RSD} − 0.050	V_{RSD}	V_{RSD} + 0.050	V	2
VRTC pin recovery voltage n (n = 1, 2, 3, 4)	V_{RSTn}	−	V_{RST} − 0.100	V_{RST}	V_{RST} + 0.100	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	−	3.6	−	24	V	−
Output Voltage							
CO pin output voltage "H"	V_{COH}	−	4.0	6.0	7.5	V	2
Input Current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−	2.0	4.0	μA	2
Current consumption during VRTC pin shutdown	I_{OPED}	V1 = V2 = V3 = V4 = V_{RSD} − 1.0 V	−	−	1.0	μA	2
VC1 pin input current	I_{VC1}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−	−	3.7	μA	2
VCn pin input current (n = 2, 3, 4)	I_{VCn}	V1 = V2 = V3 = V4 = V_{CU} − 1.0 V	−0.42	0	−	μA	2
Output Current							
CO pin source current	I_{COH}	−	−	−	−20	μA	2
CO pin sink current	I_{COL}	−	20	−	−	μA	2
Delay Time							
Overcharge detection delay time	t_{CU}	−	t_{CU} × 0.7	t_{CU}	t_{CU} × 1.3	s	2
Overcharge release delay time	t_{CL}	−	8	16	32	ms	2
Overcharge timer reset delay time	t_{TR}	With overcharge timer reset function	6	12	20	ms	−
Transition time to test mode	t_{TST}	−	−	−	10	ms	−
VRTC pin shutdown delay time	t_{RSD}	−	t_{RSD} × 0.7	t_{RSD}	t_{RSD} × 1.3	s	2
VRTC Pin Output							
VRTC pin output voltage	V_{VRTC}	I_{VRTC} = 10 μA, SW2 = ON	V_{VRTC} × 0.98	V_{VRTC}	V_{VRTC} × 1.02	V	2
VRTC pin output current	I_{VRTC}	−	−	−	2	mA	−

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuit

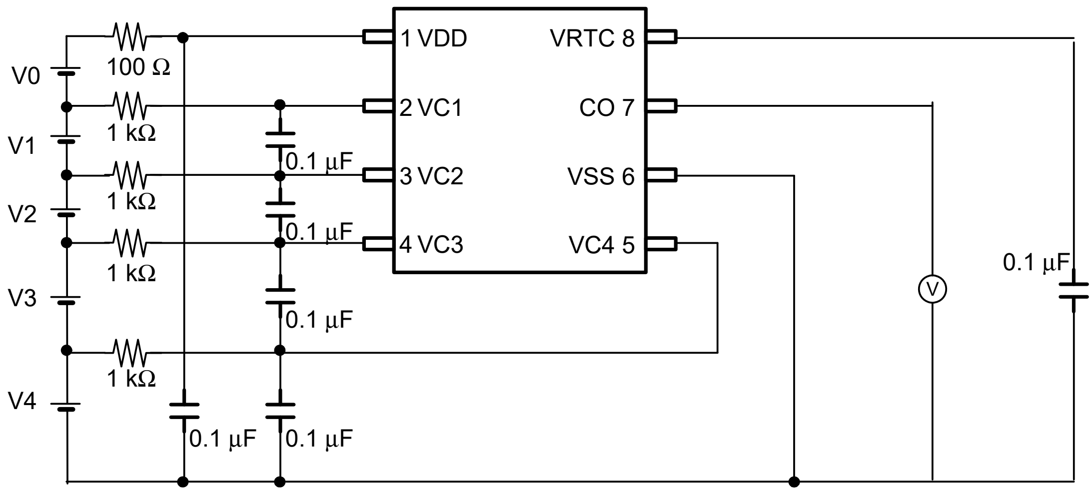


Figure 4 Test Circuit 1

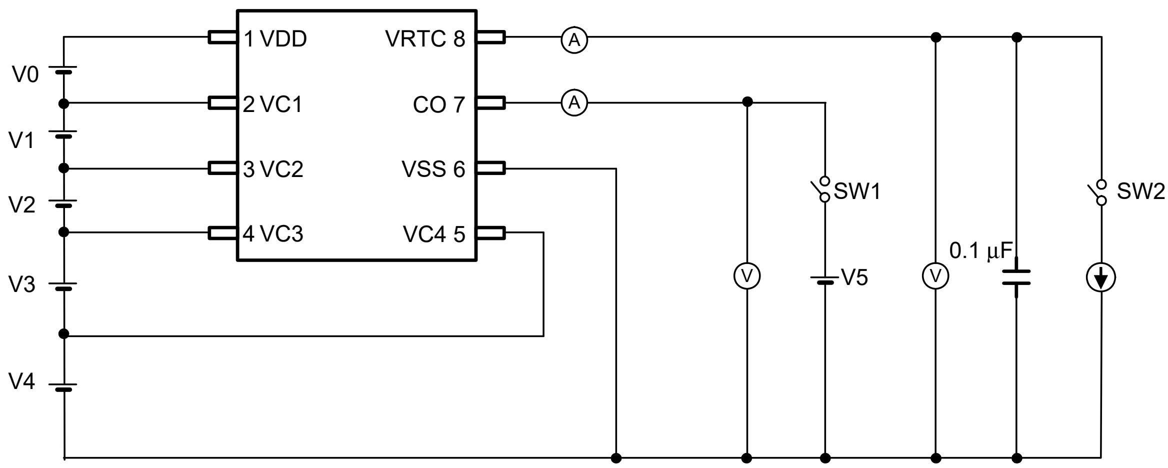


Figure 5 Test Circuit 2

In the initial status of the test circuit, SW1 and SW2 should be OFF.
This section provides explanations of test items using test circuit 1 and test circuit 2.

1. Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn}) (Test Circuit 1)

After setting V0 = 0 V, V1 = V2 = V3 = V4 = V_{CU} − 0.1 V, V1 is gradually increased. When the CO pin output inverts, the voltage V1 is defined as the overcharge detection voltage 1 (V_{CU1}). After that, V1 is then set to V_{CU} + 0.1 V, V2 = V3 = V4 = 3.5 V. V1 is gradually decreased. When the CO pin output inverts again, the voltage V1 is defined as the overcharge release voltage (V_{CL1}).

Overcharge detection voltage n (V_{CUn}) and overcharge release voltage n (V_{CLn}) can be determined in the same way as when n = 1.

Remark n = 1, 2, 3, 4

2. VRTC pin shutdown voltage n (V_{RSDn}), VRTC pin recovery voltage n (V_{RSTn}) (Test Circuit 2)

After setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V, V1 is gradually decreased. When the VRTC pin output becomes V_{SS}, the voltage V1 is defined as the VRTC pin shutdown voltage 1 (V_{RSD1}). After that, V1 is then set to V_{RSD} – 0.15 V, V2 = V3 = V4 = 3.5 V. V1 is gradually increased. When the VRTC pin output voltage becomes the VRTC pin output voltage (V_{VRTC}), the voltage V1 is defined as the VRTC pin recovery voltage 1 (V_{RST1}).
VRTC pin shutdown voltage n (V_{RSDn}) and VRTC pin recovery voltage n (V_{RSTn}) can be determined in the same way as when n = 1.

3. CO pin output voltage "H" (V_{COH}) (Test Circuit 2)

The CO pin output voltage "H" (V_{COH}) is the voltage between the CO pin and the VSS pin when V0 = 0 V, V1 = 4.9 V, V2 = V3 = V4 = 3.5 V.

4. CO pin source current (I_{COH}) (Test Circuit 2)

Set SW1 to ON after setting V0 = 0 V, V1 = 4.9 V, V2 = V3 = V4 = 3.5 V, V5 = V_{COH} – 0.5 V. The CO pin current is the CO pin source current (I_{COH}) at that time.

5. CO pin sink current (I_{COL}) (Test Circuit 2)

Set SW1 to ON after setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V, V5 = 0.5 V. The CO pin current is the CO pin sink current (I_{COL}) at that time.

6. Overcharge detection delay time (t_{CU}), overcharge release delay time (t_{CL}) (Test Circuit 2)

After setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V, V1 is increased to 4.9 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output inverts. After that, decrease V1 to 3.5 V. The overcharge release delay time (t_{CL}) is the time period until the CO pin output inverts.

7. VRTC pin shutdown delay time (t_{RSD}) (Test Circuit 2)

After setting V0 = 0 V, V1 = V2 = V3 = V4 = 3.5 V, V1 is decreased to 2.4 V. The VRTC pin shutdown delay time (t_{RSD}) is the time period until the VRTC pin output becomes V_{SS}.

Remark n = 1, 2, 3, 4

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Examples**".

1. Normal status

When all battery voltages are higher than the VRTC pin shutdown voltage (V_{RSDn}) but lower than overcharge detection voltage n (V_{CUn}), the CO pin outputs "L" and the VRTC pin outputs the VRTC pin output voltage (V_{VRTC}). This status is called the normal status.

2. Overcharge status

When the voltage of any of all batteries exceeds the overcharge detection voltage n (V_{CUn}) and this condition continues for the overcharge detection delay time (t_{CU}) or longer, the CO pin output inverts. This status is called the overcharge status. Charge control and secondary protection can be enabled by connecting an FET to the CO pin.
When all battery voltages fall below the overcharge release voltage (V_{CLn}) and this condition continues for the overcharge release delay time (t_{CL}) or longer, this IC returns to the normal status.

3. VRTC pin shutdown status

When the voltage of any of the batteries falls below the VRTC pin shutdown voltage n (V_{RSDn}) and this condition continues for the VRTC pin shutdown delay time (t_{RSD}) or longer, the VRTC pin output becomes V_{SS}. This status is called the VRTC pin shutdown status.
When all battery voltages exceed the VRTC pin recovery voltage n (V_{RSTn}), this IC returns to the normal status.

4. Overcharge timer reset function

During t_{CU}, which is from when the voltage of any of the batteries being charged exceeds V_{CUn} until charging stops, this IC has the following operations.
Even if an overcharge release noise, which temporarily forces the battery voltage below V_{CUn}, is input, t_{CU} is continuously counted as long as the overcharge release noise time is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the overcharge release noise time is t_{TR} or longer, counting of t_{CU} is reset once. After that, when V_{CUn} has been exceeded, counting of t_{CU} resumes.

Remark n = 1, 2, 3, 4

5. Test mode

In this IC, the overcharge detection delay time (t_{CU}) and VRTC pin shutdown delay time (t_{RSD}) can be shortened by entering the test mode.
The test mode can be set by retaining the VDD pin voltage 7.0 V or higher than the VC1 pin voltage for at least 10 ms (V1 = V2 = V3 = V4 = 3.5 V, Ta = +25°C). The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin.
When this IC becomes the detection status after the delay time following the detection of an overcharge or VRTC pin shutdown has elapsed, the latch for retaining the test mode is reset and this IC is released from the test mode.

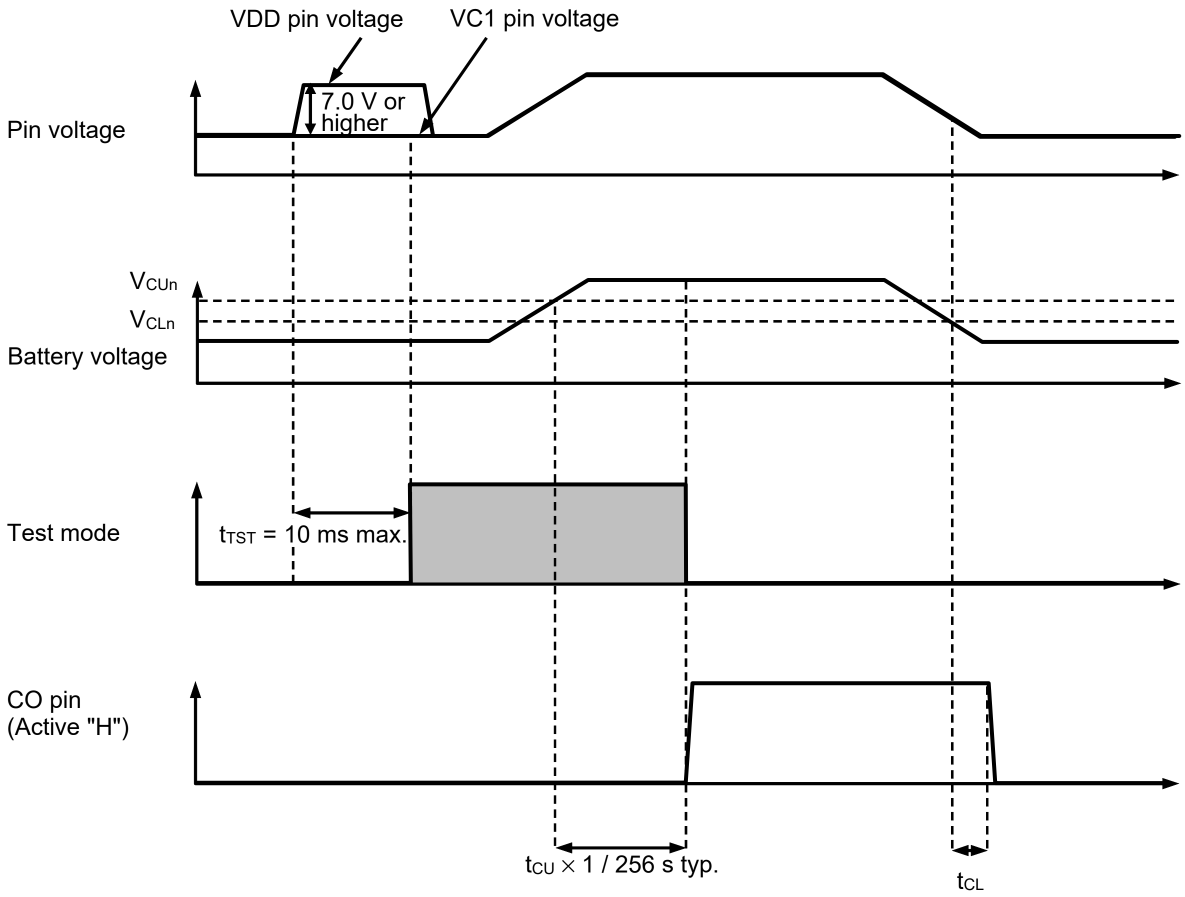


Figure 6

Caution 1. Set the test mode when no batteries are overcharged.
2. The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.

Remark n = 1, 2, 3, 4

■ Timing Charts

1. Overcharge detection operation (With overcharge timer reset function)

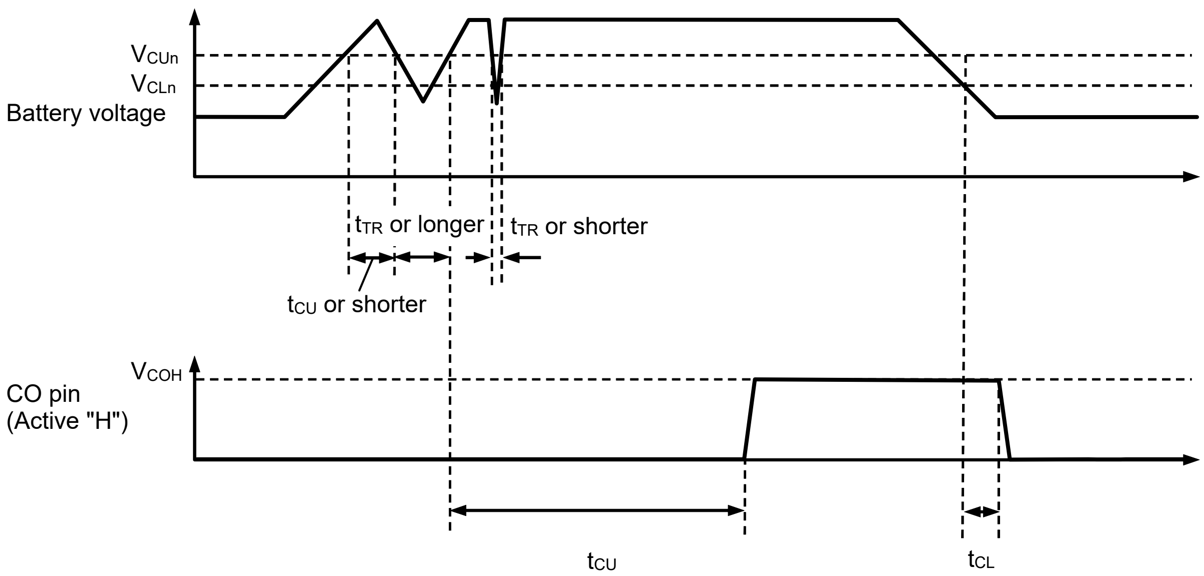


Figure 7

Remark n = 1, 2, 3, 4

2. VRTC pin shutdown operation

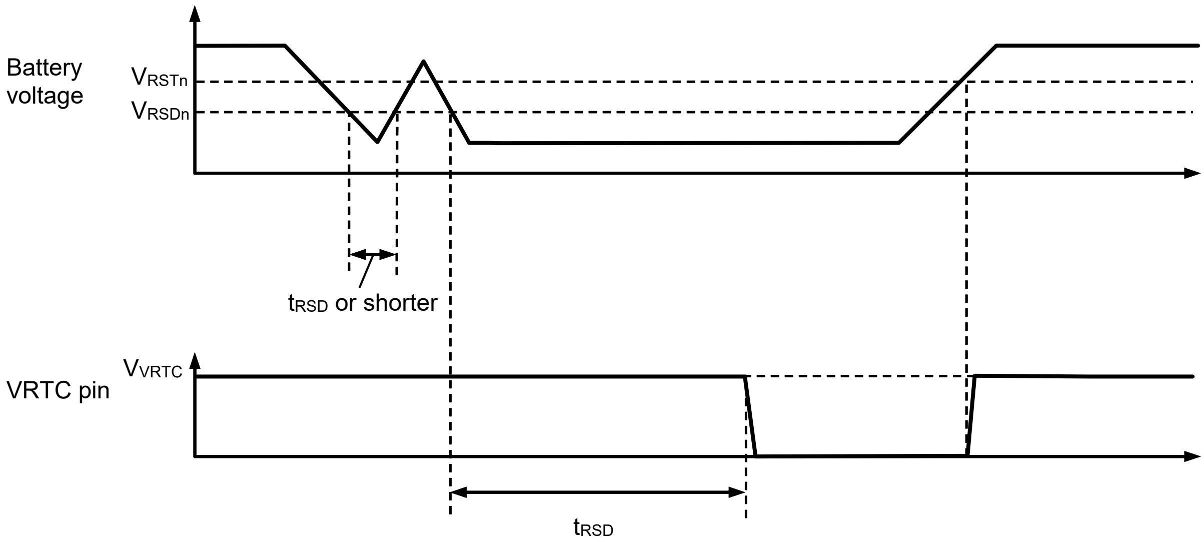


Figure 8

Remark n = 1, 2, 3, 4

3. Overcharge timer reset operation (With overcharge timer reset function)

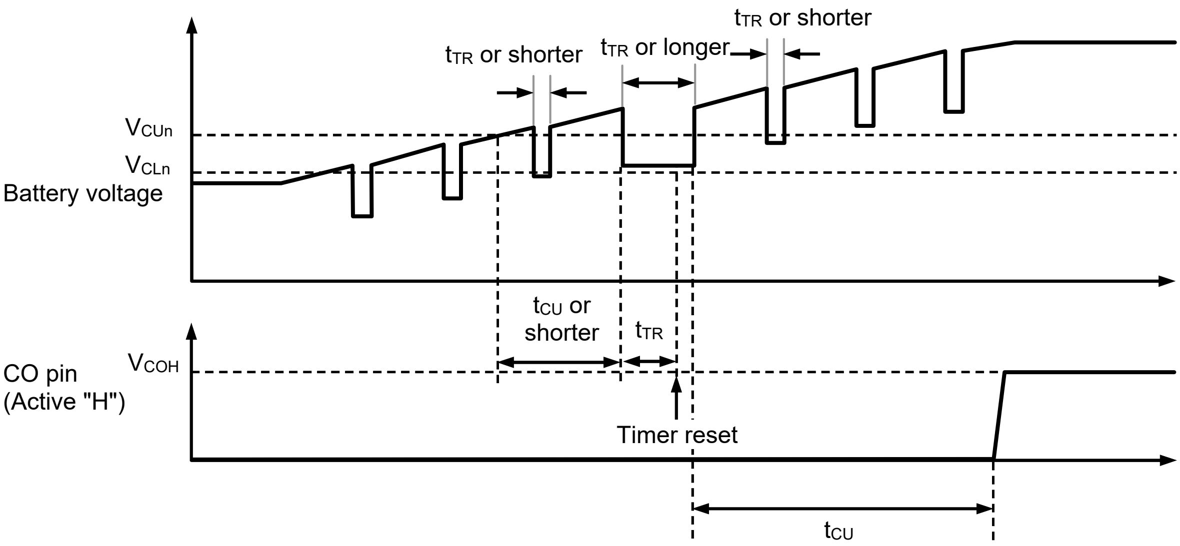
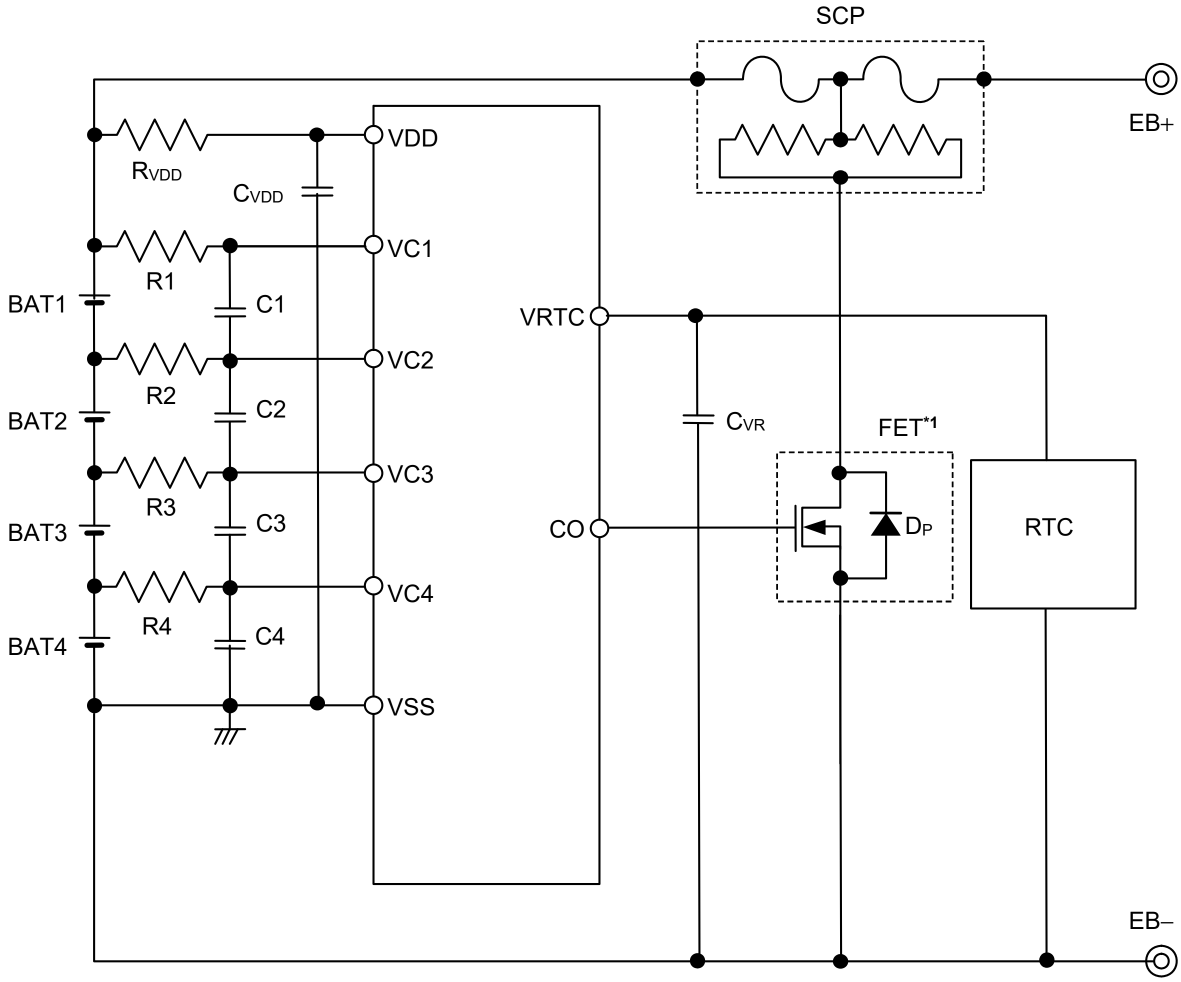


Figure 9

Remark n = 1, 2, 3, 4

■ Battery Protection IC Connection Examples

1. 4-serial cell



***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 10

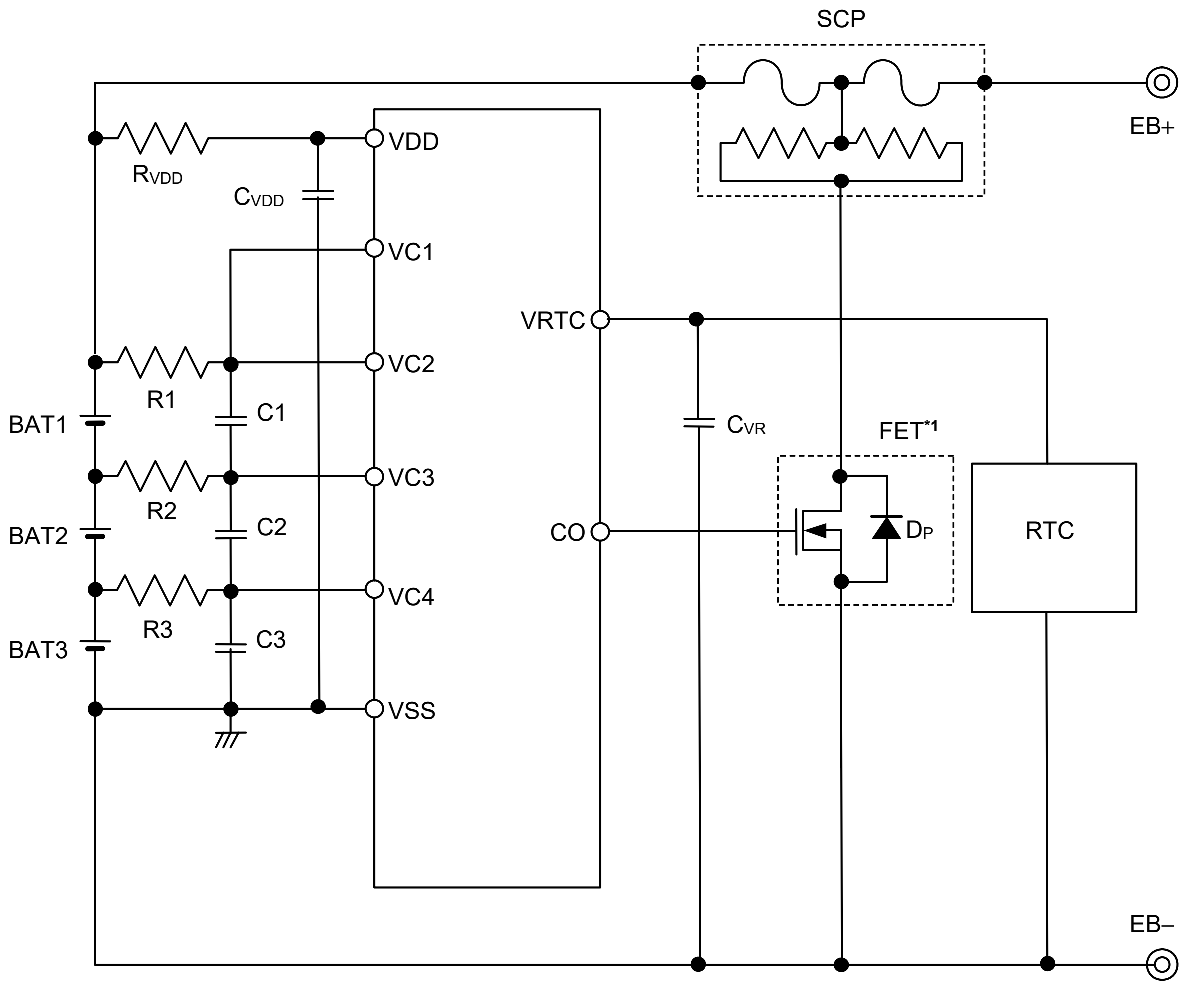
Table 9 Constants for External Components

No.	Part	Min.	Typ.*1	Max.	Unit
1	R1 to R4	1	1	1	kΩ
2	C1 to C4, C_{VDD}	0.1	0.1	1	μF
3	R_{VDD}	100	100	1000	Ω
4	C_{VR}	–	0.1	–	μF

***1.** Accuracy of overcharge detection voltage is guaranteed by typ. value in **Table 9**. Connecting components with other values will worsen the accuracy.

Caution
1. **The constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3. **Set the same constants to R1 to R4 and to C1 to C4 and C_{VDD}.**
4. **Since the CO pin may become the detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.**

2. 3-serial cell



***1.** This IC limits its CO pin output voltage to 7.5 V max., so a FET with the gate withstand voltage of 8 V can be used.

Figure 11

Table 10 Constants for External Components

No.	Part	Min.	Typ.*1	Max.	Unit
1	R1 to R3	1	1	1	kΩ
2	C1 to C3, C_{VDD}	0.1	0.1	1	μF
3	R_{VDD}	100	100	1000	Ω
4	C_{VR}	–	0.1	–	μF

***1.** Accuracy of overcharge detection voltage is guaranteed by typ. value in **Table 10**.
Connecting components with other values will worsen the accuracy.

Caution
1. **The constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3. **Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.**
4. **Since the CO pin may become the detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the protection fuse from cutoff.**

[For SCP, contact]

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https://www.dexerials.jp/en/

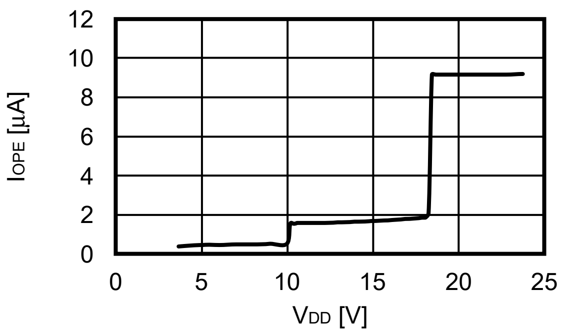
■ Precaution

- Do not connect batteries charged with V_{CL} or higher.
- If the connected batteries include a battery charged with V_{CL} or higher, this IC may become the overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of the CO pin detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Customers who desire a product that does not limit the order of battery connection should consider the S-82K3/K4 Series of products instead.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figures in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

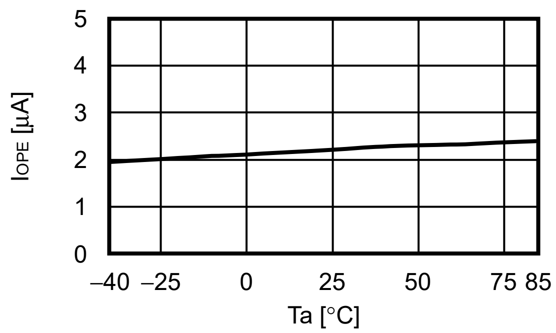
■ Characteristics (Typical Data)

1. Current consumption

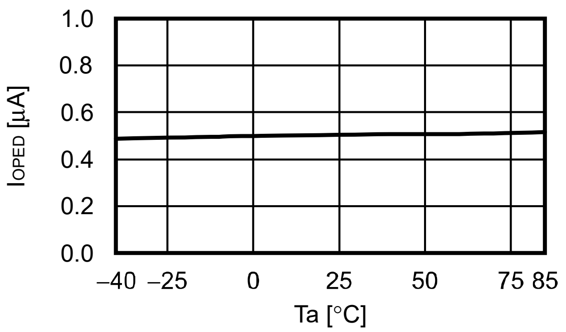
1. 1 I_{OPE} vs. V_{DD}



1. 2 I_{OPE} vs. Ta

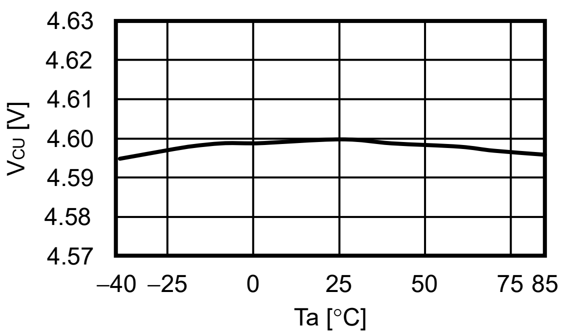


1. 3 I_{OPED} vs. Ta

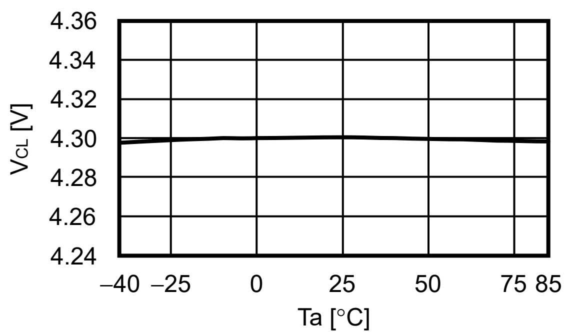


2. Detection voltage, release voltage

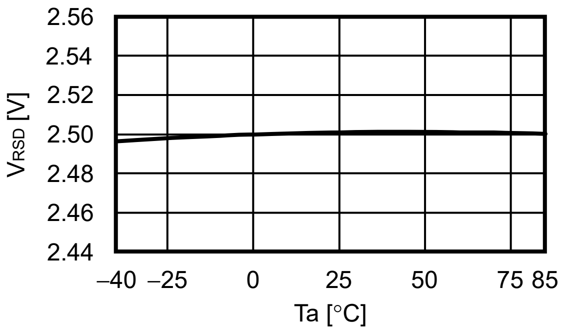
2. 1 V_{CU} vs. Ta



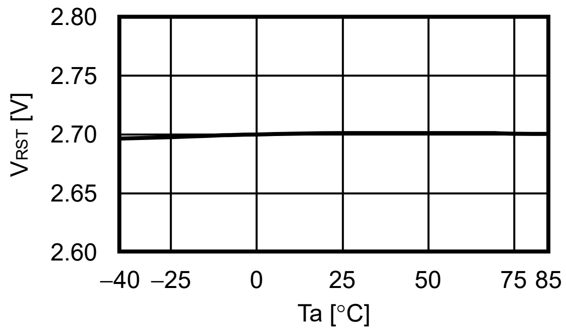
2. 2 V_{CL} vs. Ta



2. 3 V_{RSD} vs. Ta

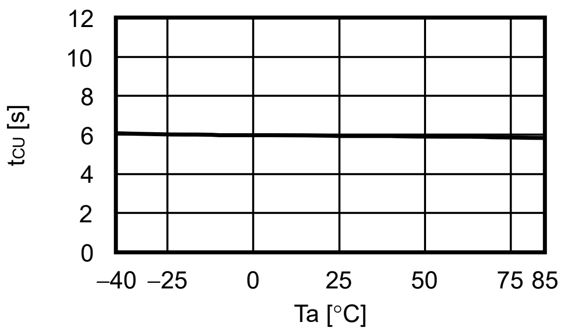


2. 4 V_{RST} vs. Ta

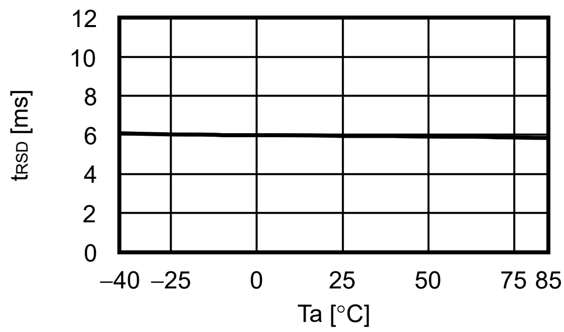


3. Delay time

3. 1 t_{CU} vs. Ta

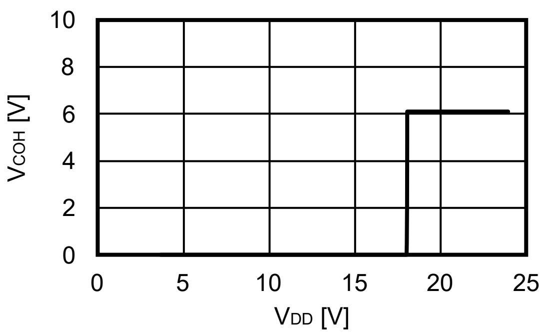


3. 2 t_{RSD} vs. Ta

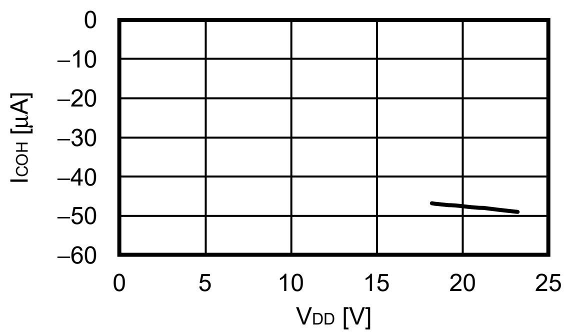


4. Output pin

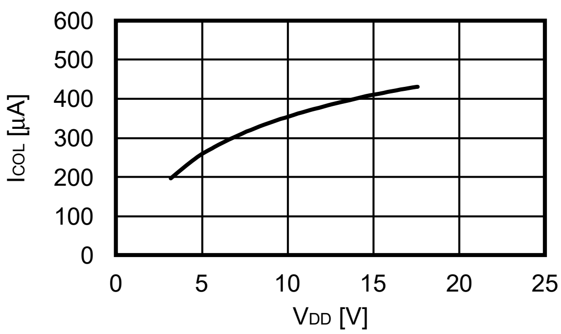
4. 1 V_{COH} vs. V_{DD}



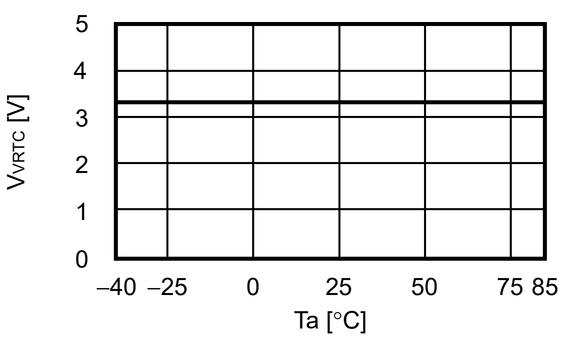
4. 2 I_{COH} vs. V_{DD}



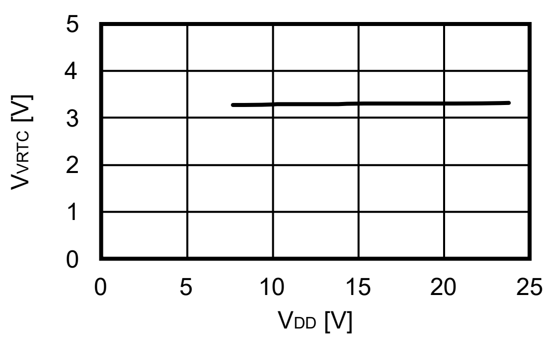
4. 3 I_{COL} vs. V_{DD}



4. 4 V_{VRTC} vs. Ta

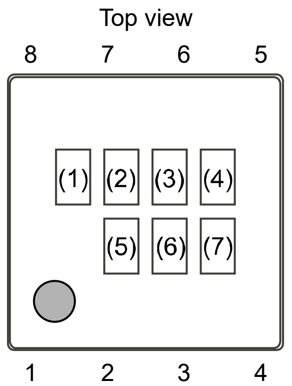


4. 5 V_{VRTC} vs. V_{DD}



■ Marking Specifications

1. DFN-8(2020)A

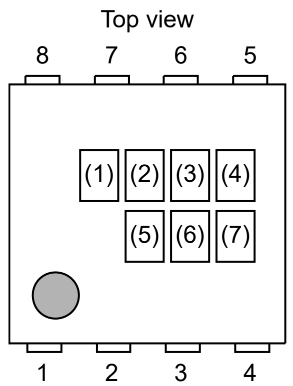


(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5) to (7): Lot number

Product name vs. Product code

Product name	Product code		
	(2)	(3)	(4)
S-82H4AAA-A8T8U	9	K	A
S-82H4AAB-A8T8U	9	K	B
S-82H4AAC-A8T8U	9	K	C
S-82H4AAD-A8T8U	9	K	D
S-82H4AAE-A8T8U	9	K	E

2. HSNT-8(1616)



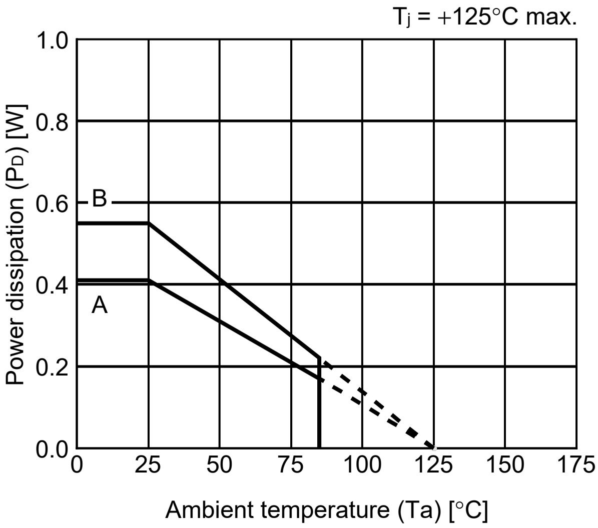
(1): Blank
(2) ~ (4): Product code (Refer to **Product name vs. Product code**)
(5) ~ (7): Lot number

Product name vs. Product code

Product name	Product code		
	(2)	(3)	(4)
S-82H4AAA-A8T2U	9	K	A

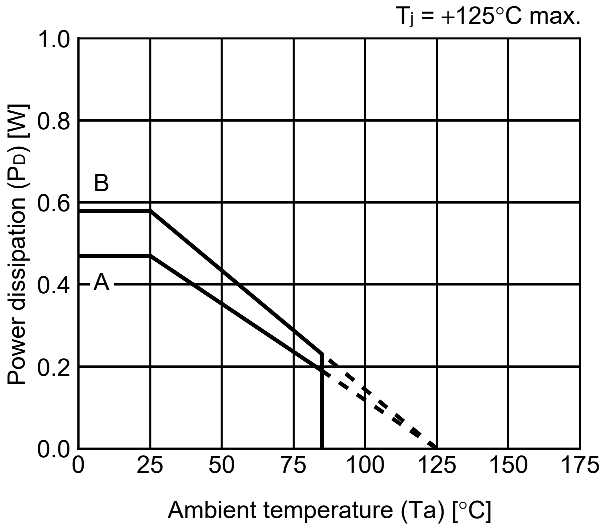
■ Power Dissipation

DFN-8(2020)A



Board	Power Dissipation (P_D)
A	0.41 W
B	0.55 W
C	–
D	–
E	–

HSNT-8(1616)

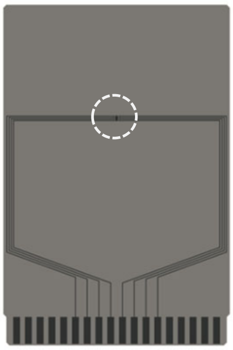


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

DFN-8(2020)A Test Board

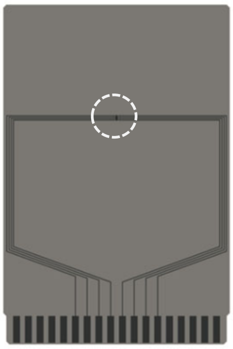
IC Mount Area

(1) Board A

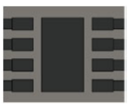


Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-



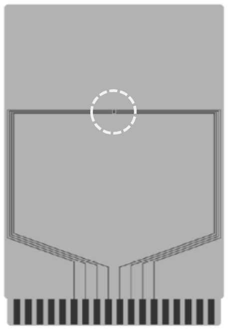
enlarged view

No. DFN8-E-Board-SD-1.0

HSNT-8(1616) Test Board

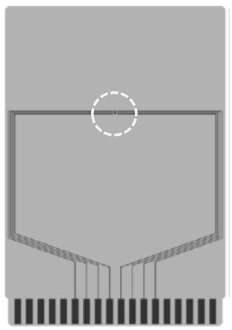
IC Mount Area

(1) Board A



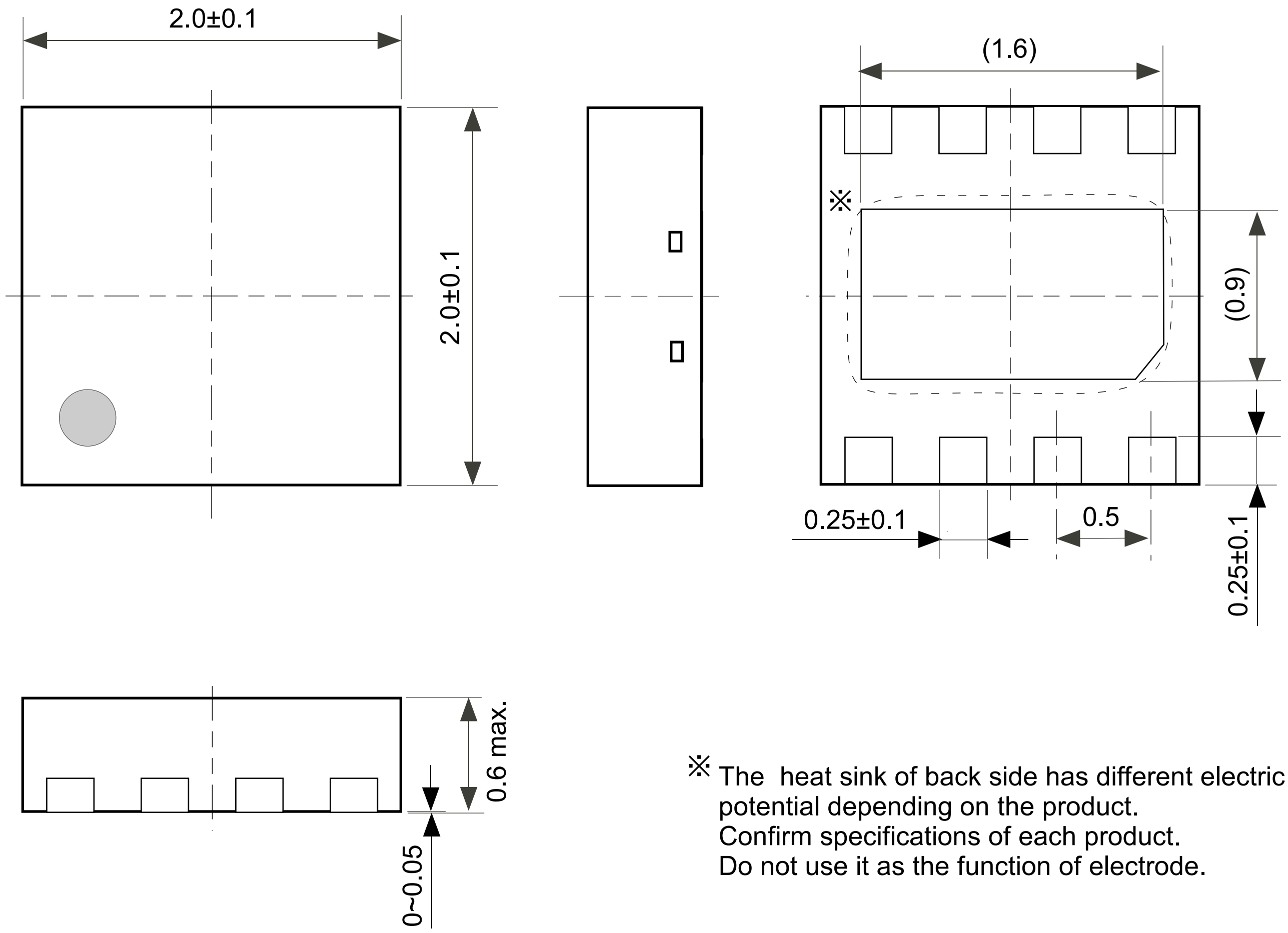
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. HSNT8-B-Board-SD-1.0

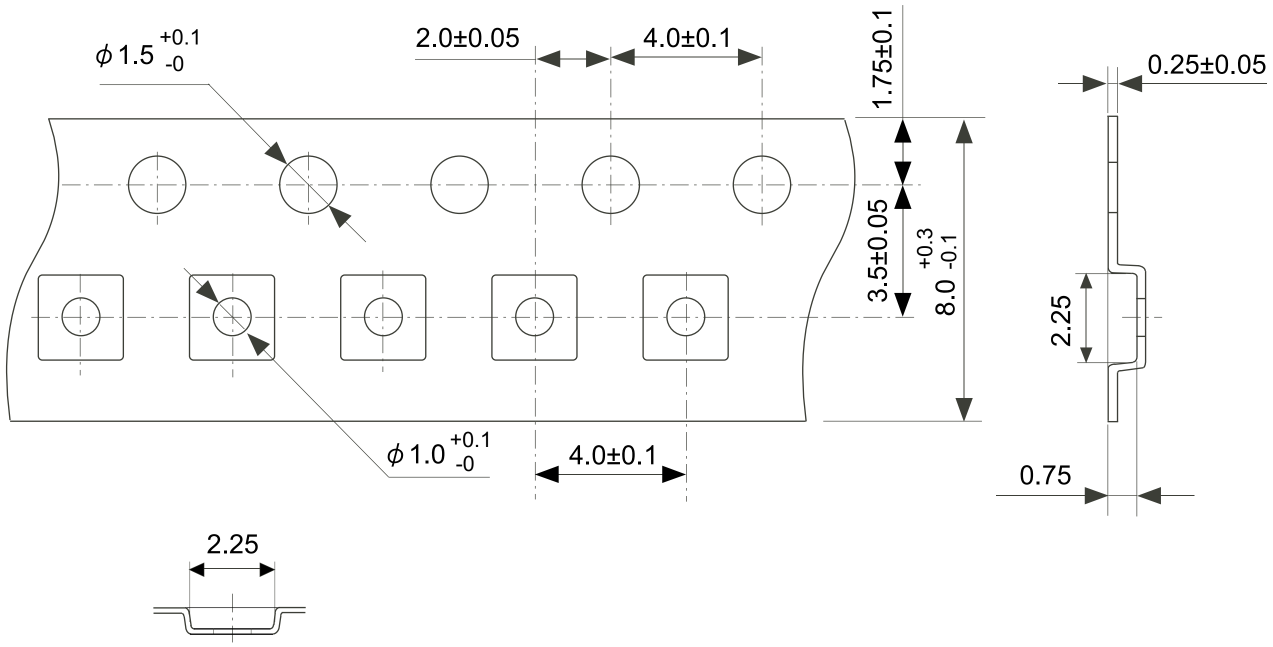


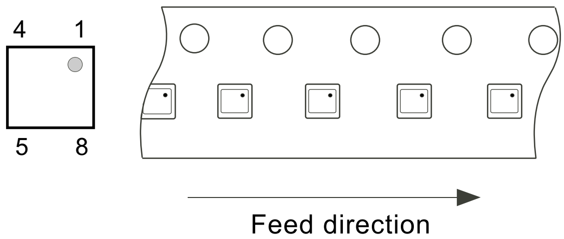
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. IB008-A-P-SD-1.0

TITLE	DFN-8-E-PKG Dimensions
No.	IB008-A-P-SD-1.0
ANGLE	
UNIT	mm

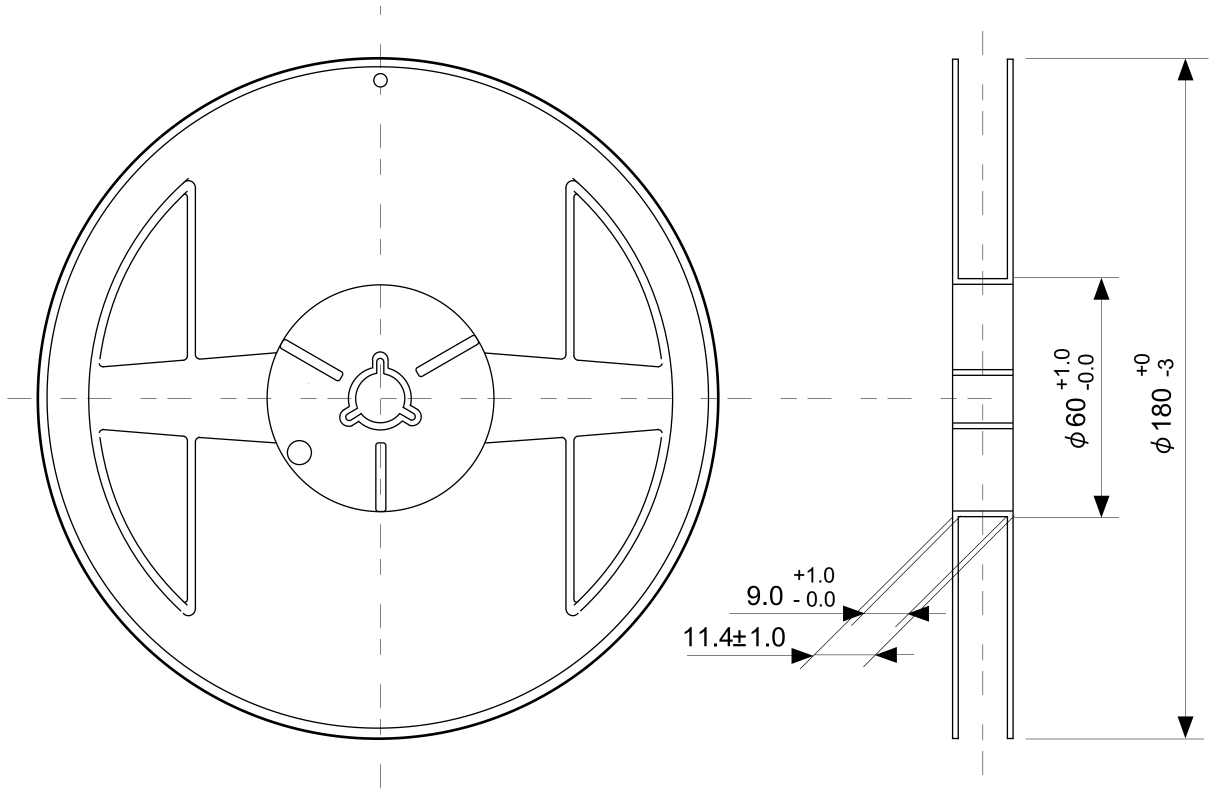
ABLIC Inc.



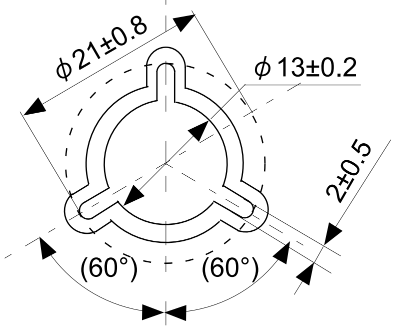


No. IB008-A-C-SD-1.0

TITLE	DFN-8-E-Carrier Tape
No.	IB008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	



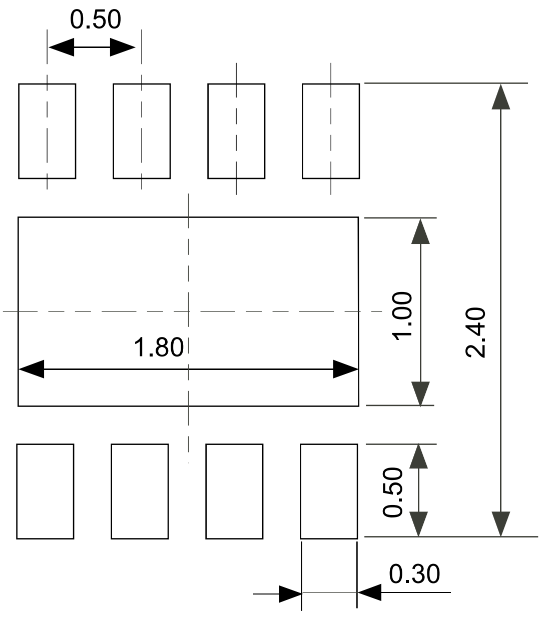
Enlarged drawing in the central part



No. IB008-A-R-SD-1.0

TITLE	DFN-8-E-Reel		
No.	IB008-A-R-SD-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

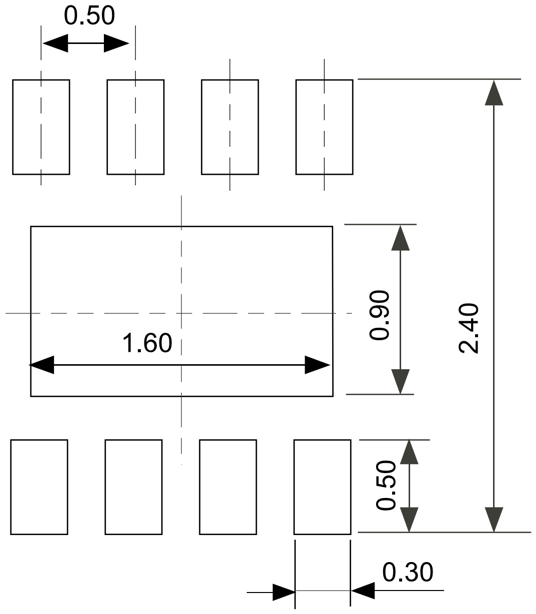
Land Pattern



Cauion It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意 放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



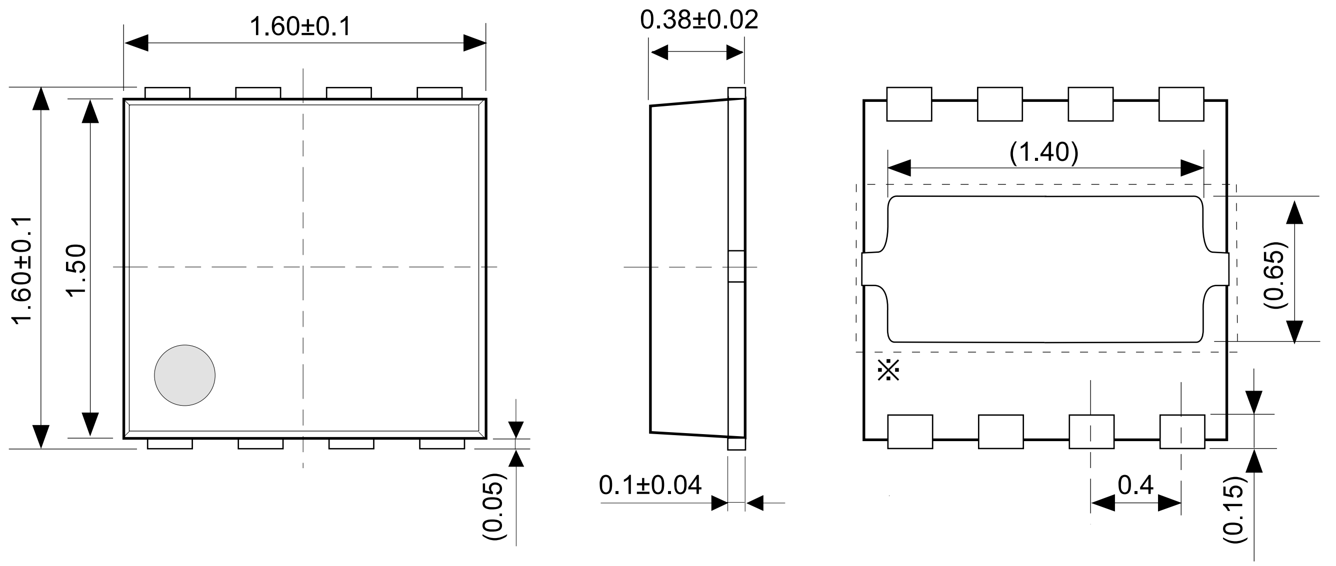
Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 80%.
③ Mask thickness: t0.12 mm

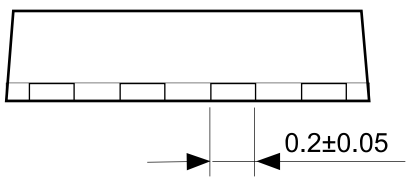
注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は80%です。
③マスク厚み：t0.12 mm

No. IB008-A-L-SD-1.0

TITLE	DFN-8-E -Land Recommendation
No.	IB008-A-L-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



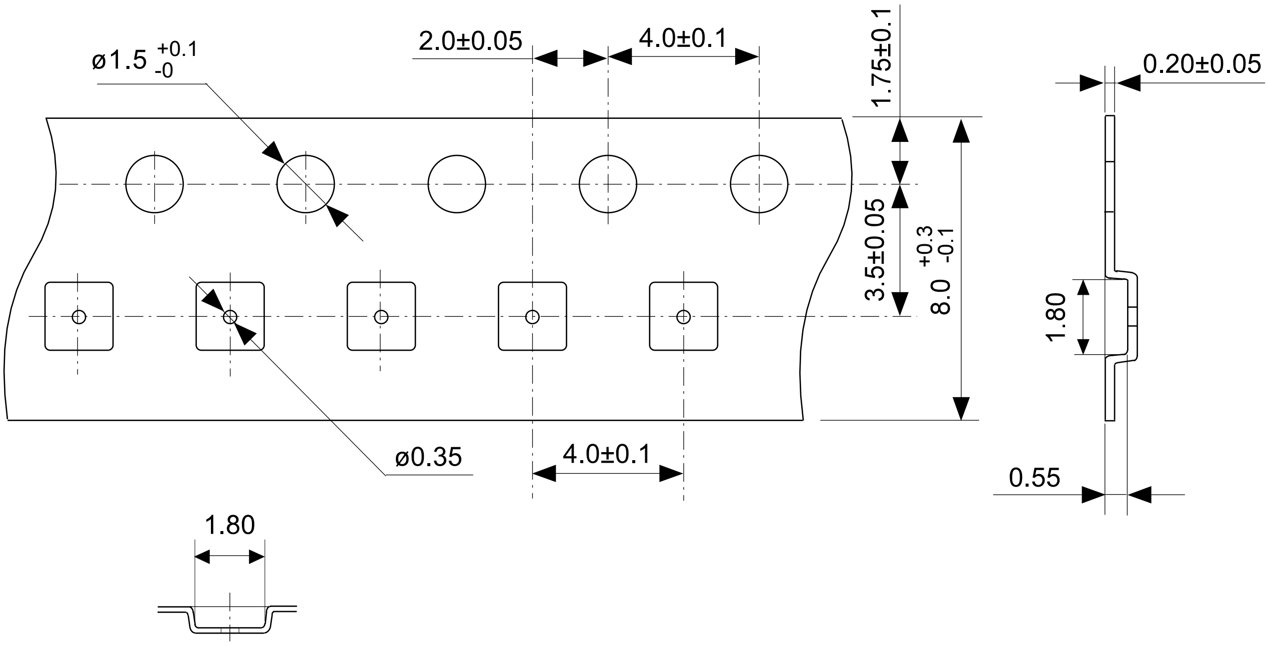


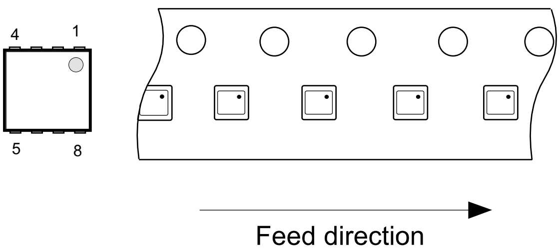
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PY008-A-P-SD-1.0

TITLE	HSNT-8-B-PKG Dimensions
No.	PY008-A-P-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

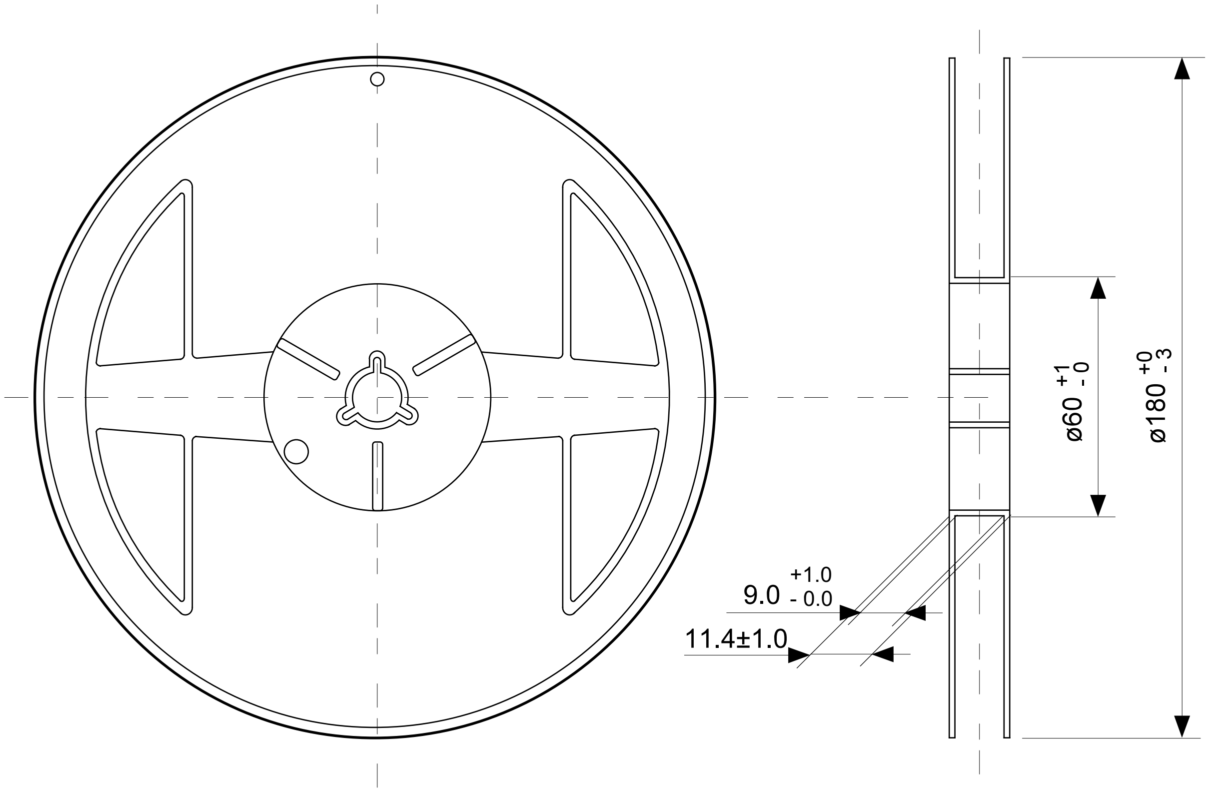




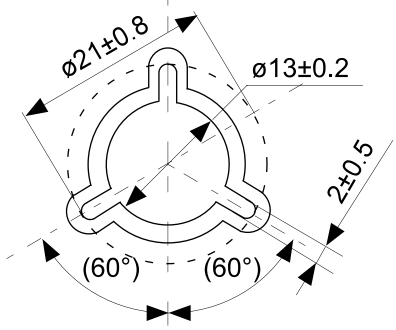
No. PY008-A-C-SD-1.0

TITLE	HSNT-8-B-Carrier Tape
No.	PY008-A-C-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.



Enlarged drawing in the central part

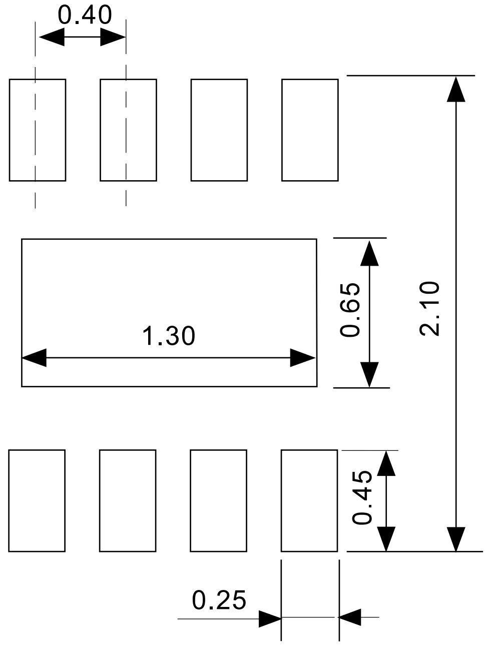


No. PY008-A-R-SD-1.0

TITLE	HSNT-8-B-Reel		
No.	PY008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		

ABLIC Inc.

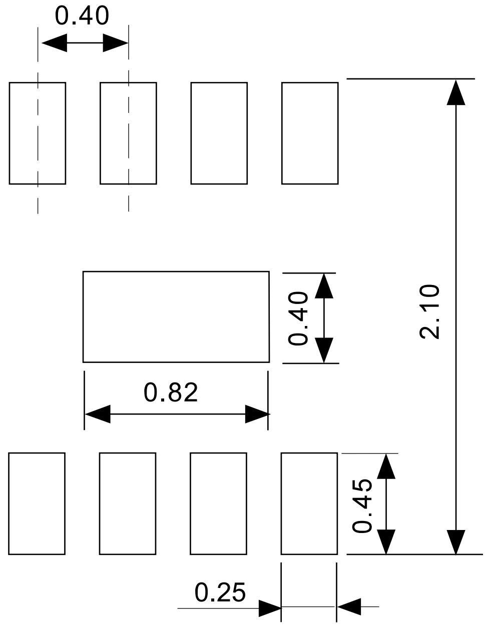
Land Pattern



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.

注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Metal Mask Pattern



Caution ① Mask aperture ratio of the lead mounting part is 100%.
② Mask aperture ratio of the heat sink mounting part is 40%.
③ Mask thickness: t0.12 mm

注意 ①リード実装部のマスク開口率は100%です。
②放熱板実装のマスク開口率は40%です。
③マスク厚み：t0.12 mm

No. PY008-A-L-SD-1.0

TITLE	HSNT-8-B -Land Recommendation
No.	PY008-A-L-SD-1.0
ANGLE	
UNIT	mm

ABLIC Inc.

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