S-82C4A/5A Series

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BATTERY PROTECTION IC FOR 4-SERIAL OR 5-SERIAL CELL PACK

Rev.1.1_00

This IC is a protection IC for lithium-ion rechargeable batteries, which includes temperature protection circuits, high-accuracy voltage detection circuits, and delay circuits. Temperature protection is possible by connecting an NTC thermistor to the dedicated connection pin. It is suitable for protecting 4-serial or 5-serial cell lithium-ion rechargeable battery packs from overcharge, overdischarge, and overcurrent.

■ Features

- High-accuracy voltage detection for each cell

Overcharge detection voltage n	3.900 V to 4.500 V (25 mV step)	Accuracy ±20 mV
Overcharge release voltage n	3.500 V to 4.500 V[*1]	Accuracy ±50 mV
Overdischarge detection voltage n	2.000 V to 3.200 V (100 mV step)	Accuracy ±50 mV
Overdischarge release voltage n	2.000 V to 3.400 V[*2]	Accuracy ±100 mV

- Three-level discharge overcurrent detection

Discharge overcurrent 1 detection voltage	10 mV to 200 mV (5 mV step)	Accuracy ±5 mV
Discharge overcurrent 2 detection voltage	20 mV to 300 mV (5 mV step)	Accuracy ±10 mV
Load short-circuiting detection voltage	50 mV to 400 mV (10 mV step)	Accuracy ±20 mV

- Charge overcurrent detection

Charge overcurrent detection voltage	−200 mV to −10 mV (5 mV step)	Accuracy ±5 mV

- Discharge overcurrent 1 detection delay time is settable by an external capacitor (The other delay time are internally fixed)
- Power saving control by a control pin

• 0 V battery charge:	Enabled, inhibited
• Power-down function:	Available, unavailable
• Release condition of discharge overcurrent status:	Load disconnection, charger connection

- Output voltage of CO and DO pin is limited to VC2 pin voltage. (S-82C5A Series)
- Detecting temperature is possible with connecting an NTC thermistor at four different points of high-and-low temperatures during charging and of high-and-low temperatures during charge-discharge.

High temperature charge-discharge inhibition temperature	+40°C to +85°C (1°C step)	Accuracy ±3°C[*3]
High temperature charge inhibition temperature	+40°C to +85°C (1°C step)	Accuracy ±3°C[*3]
Low temperature charge inhibition temperature	−40°C to +10°C (1°C step)	Accuracy ±3°C[*3]
Low temperature charge-discharge inhibition temperature	−40°C to +10°C (1°C step)	Accuracy ±3°C[*3]

• High-withstand voltage:	Absolute maximum rating 28.0 V
• Wide operating voltage range:	5.0 V to 24.0 V
• Wide operation temperature range:	Ta = −40°C to +85°C
• Low current consumption	
During operation:	5.0 μA typ., 10 μA max. (Ta = +25°C)
During power-down:	0.1 μA max. (Ta = +25°C)
During power-saving:	0.1 μA max. (Ta = +25°C)

- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage n can be selected from a range of 0 V to 0.4 V in 50 mV steps.)

***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n can be selected from a range of 0 V to 0.7 V in 100 mV steps.)

***3.** Temperature detection accuracy varies with NTC thermistor specifications.
When an NTC thermistor listed in **Table 2** is connected, the detection temperature and accuracy can be achieved.

Remark n = 1, 2, 3, 4, 5

■ Applications

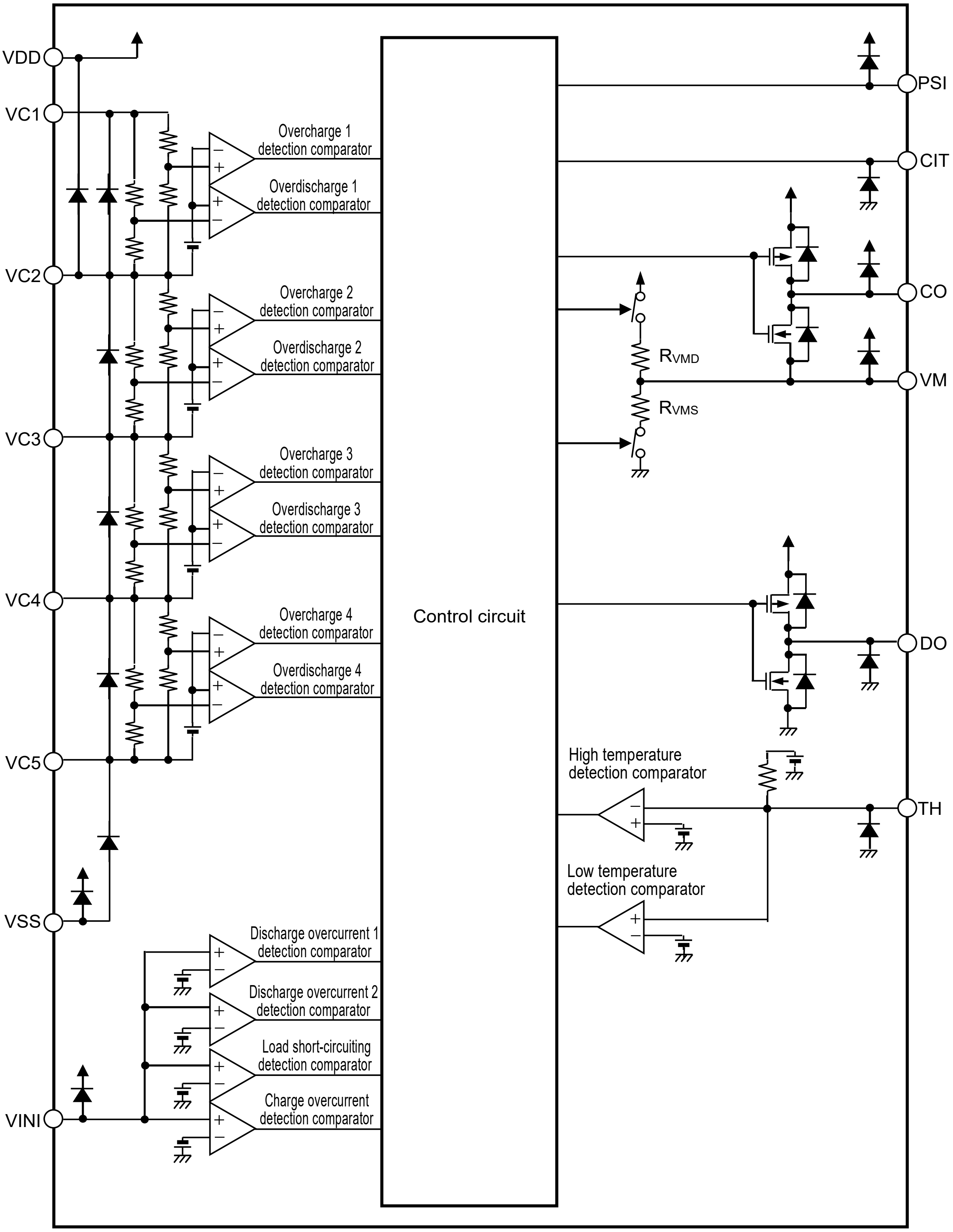
- Lithium-ion rechargeable battery packs

■ Package

- 16-Pin TSSOP

■ Block Diagram

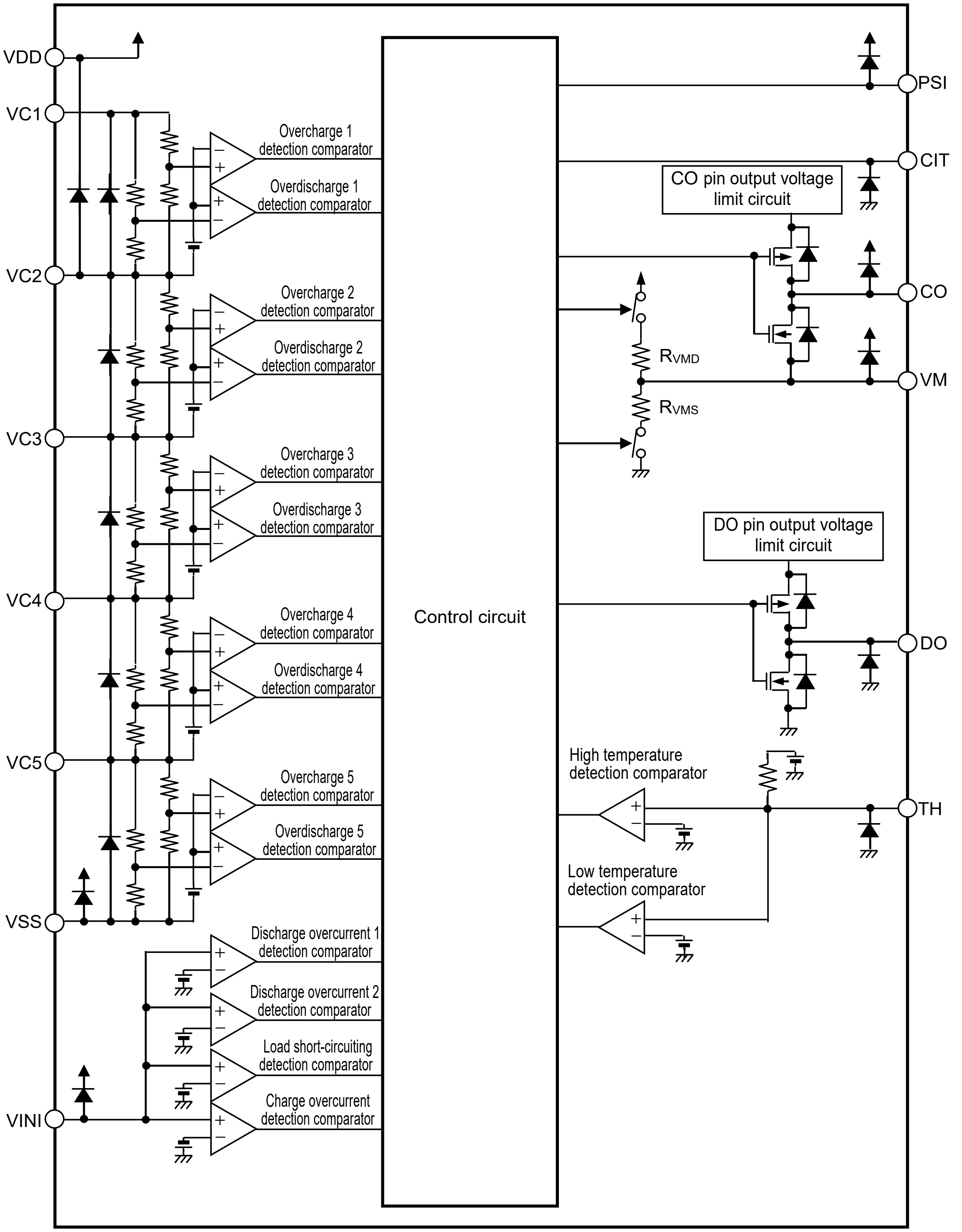
1. S-82C4A Series



Remark Diodes in the figure are parasitic diodes.

Figure 1

2. S-82C5A Series



Remark Diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product name

S-82C x A xx - TCT1 U 7

Environmental code
U: Lead-free (Sn 100%), halogen-free

Package abbreviation and IC packing specifications*1
TCT1: 16-Pin TSSOP, Tape

Serial code*2
Sequentially set from AA to ZZ

Number of cells in series
4: 4-serial cell
5: 5-serial cell

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-S1

3. Product name list

3. 1 S-82C5A Series

Table 2 (1 / 3)

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Overdischarge Detection Voltage [V_{DL}]	Overdischarge Release Voltage [V_{DU}]	Discharge Overcurrent 1 Detection Voltage [V_{DIOV1}]	Discharge Overcurrent 2 Detection Voltage [V_{DIOV2}]	Load Short-circuiting Detection Voltage [V_{SHORT}]	Charge Overcurrent Detection Voltage [V_{CIOV}]
S-82C5AAA-TCT1U7	4.400 V	4.200 V	2.500 V	3.000 V	10 mV	20 mV	50 mV	−10 mV

Table 2 (2 / 3)

Product Name	Delay Time Combination[*1]	0 V Battery Charge	Power-down Function	Release Condition of Discharge Overcurrent Status[*2]
S-82C5AAA-TCT1U7	(1)	Inhibited	Available	Load disconnection

Table 2 (3 / 3)

Product Name	High Temperature Charge -discharge Inhibition Temperature[*3] [T_{HCD}]	High Temperature Charge Inhibition Temperature[*3] [T_{HC}]	Low Temperature Charge Inhibition Temperature[*3] [T_{LC}]	Low Temperature Charge -discharge Inhibition Temperature[*3] [T_{LCD}]	Hysteresis Temperature[*4] [T_{HYS}]	Sampling Wait Time[*5] [t_{SLEEP}]	Continuous Detection / Release Count[*6] [N]	Resistance[*7] [R_{NTC}]	B-value[*7] [B]
S-82C5AAA-TCT1U7	82°C	40°C	10°C	−37°C	10°C	512 ms	2	100 kΩ ±1%	4250 K ±1%

***1.** Refer to **Table 3** about the details of the delay time combinations.
***2.** Release condition of discharge overcurrent status: Load disconnection, charger connection
***3.** Satisfy $T_{HCD} > T_{HC} > T_{LC} > T_{LCD}$ when selecting them.
***4.** Hysteresis Temperature: 5°C, 10°C
***5.** Sampling wait time: 256 ms, 512 ms, 1.0 s
***6.** Continuous detection / release count: 1, 2, 3, 4, 5, 6
***7.** Temperature detection accuracy varies with NTC thermistor specifications.
When an NTC thermistor listed in **Table 2** is connected, the detection temperature and accuracy can be achieved.

Remark Please contact our sales representatives for products other than the above.

Table 3

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent 2 Detection Delay Time [t_{DIOV2}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]
(1)	1.0 s	128 ms	16 ms	16 ms

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales representatives.

Table 4

Delay Time	Symbol	Selection Range							Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s	2.0 s	–	–	–	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms	128 ms	256 ms	512 ms	1.0 s	–	Select a value from the left.
Discharge overcurrent 2 detection delay time	t_{DIOV2}	4 ms	8 ms	16 ms	32 ms	64 ms	–	–	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms	16 ms	32 ms	64 ms	128 ms	256 ms	Select a value from the left.

■ Pin Configuration

1. 16-Pin TSSOP

Top view

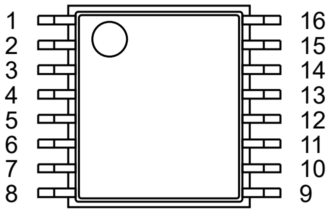


Figure 3

Table 5

Pin No.	Symbol	Description
1	VC1	Connection pin for battery 1's positive voltage
2	VC2	Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage
3	VC3	Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage
4	VC4	Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage
5	VC5	Connection pin for battery 4's negative voltage, Connection pin for battery 5's positive voltage
6	VSS	Input pin for negative power supply, Connection pin for battery 5's negative voltage
7	VINI	Voltage detection pin between VSS pin and VINI pin
8	CIT	Capacitor connection pin for discharge overcurrent 1 detection delay time
9	NC[*1]	No connection
10	TH	Input pin for temperature detection
11	PSI	Control pin for power-saving
12	DO	Connection pin of discharge control FET gate (CMOS output)
13	NC[*1]	No connection
14	CO	Connection pin of charge control FET gate (CMOS output)
15	VM	Voltage detection pin between VSS pin and VM pin
16	VDD	Input pin for positive power supply, Connection pin for battery 1's positive voltage

***1.** The NC pin is electrically open. The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	$V_{SS} - 0.3$ to $V_{SS} + 28.0$	V
Input pin voltage 1	V_{IN1}	VC1	$V_{VC2} - 0.3$ to $V_{VC2} + 6.0$	V
		VC3	$V_{VC4} - 0.3$ to $V_{DD} + 0.3 \leq V_{VC4} + 6.0$	V
		VC4	$V_{VC5} - 0.3$ to $V_{DD} + 0.3 \leq V_{VC5} + 6.0$	V
Input pin voltage 2	V_{IN2}	VC2	$V_{DD} - 6.0 \leq V_{VC3} - 0.3$ to $V_{DD} + 0.3 \leq V_{VC3} + 6.0$	V
Input pin voltage 3	V_{IN3}	VC5	$V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 6.0$	V
Input pin voltage 4	V_{IN4}	TH, CIT	$V_{SS} - 0.3$ to $V_{SS} + 6.0$	V
Input pin voltage 5	V_{IN5}	PSI, VM, VINI	$V_{DD} - 28.0$ to $V_{DD} + 0.3$	V
Output pin voltage 1	V_{OUT1}	DO	$V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 28.0$	V
Output pin voltage 2	V_{OUT2}	CO	$V_{DD} - 28.0 \leq V_{VM} - 0.3$ to $V_{DD} + 0.3$	V
Operation ambient temperature	T_{opr}	–	−40 to +85	°C
Storage temperature	T_{stg}	–	−55 to +125	°C

Caution **The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance[*1]	θ_{JA}	16-Pin TSSOP	Board A	–	88	–	°C/W
			Board B	–	74	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "**■ Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 8 (1 / 2)

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage n	V_{CUn}	–	$V_{CU} - 0.020$	V_{CU}	$V_{CU} + 0.020$	V	1
Overcharge release voltage n	V_{CLn}	–	$V_{CL} - 0.050$	V_{CL}	$V_{CL} + 0.050$	V	1
Overdischarge detection voltage n	V_{DLn}	–	$V_{DL} - 0.050$	V_{DL}	$V_{DL} + 0.050$	V	1
Overdischarge release voltage n	V_{DUn}	–	$V_{DU} - 0.100$	V_{DU}	$V_{DU} + 0.100$	V	1
Discharge overcurrent 1 detection voltage	V_{DIOV1}	–	$V_{DIO1V} - 5$	V_{DIOV1}	$V_{DIOV1} + 5$	mV	1
Discharge overcurrent 2 detection voltage	V_{DIOV2}	–	$V_{DIOV2} - 10$	V_{DIOV2}	$V_{DIOV2} + 10$	mV	1
Load short-circuiting detection voltage	V_{SHORT}	–	$V_{SHORT} - 20$	V_{SHORT}	$V_{SHORT} + 20$	mV	1
Charge overcurrent detection voltage	V_{CIOV}	–	$V_{CIOV} - 5$	V_{CIOV}	$V_{CIOV} + 5$	mV	1
Delay Time							
CIT pin charge current	I_{CIT}	–	80	120	170	nA	1
CIT pin detection voltage	V_{CIT}	–	1.1	1.2	1.3	V	1
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	1
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.7$	t_{DL}	$t_{DL} \times 1.3$	–	1
Discharge overcurrent 2 detection delay time	t_{DIOV2}	–	$t_{DIOV2} \times 0.7$	t_{DIOV2}	$t_{DIOV2} \times 1.3$	–	1
Load short-circuiting detection delay time	t_{SHORT}	Internally fixed delay time	100	300	600	μs	1
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.7$	t_{CIOV}	$t_{CIOV} \times 1.3$	–	1
PSI pin response time	t_{PSI}	–	1.4	2.0	2.6	ms	1
0 V Battery Charge							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge enabled	–	0.8	1.5	V	1
0 V battery charge inhibition battery voltage n	V_{0INH}	0 V battery charge inhibited	1.0	1.2	1.5	V	1

Remark n = 1, 2, 3, 4, 5

Table 8 (2 / 2)

(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Internal Resistance							
Resistance between VDD pin and VM pin	R_{VMD}	–	0.5	1	1.5	MΩ	1
Resistance between VM pin and VSS pin	R_{VMS}	–	7.5	15	30	kΩ	1
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	Fixed output voltage of DO pin and CO pin	5.0	–	24.0	V	1
External control input pin							
PSI pin reverse voltage "H"	V_{PSIH}	–	0.8	1.0	1.3	V	1
PSI pin reverse voltage "L"	V_{PSIL}	–	0.5	0.8	1.0	V	1
Input Current							
Current consumption during operation	I_{OPE}	–	–	5	10	μA	1
Current consumption during power-down	I_{PDN}	–	–	–	0.1	μA	1
Current consumption during power-saving	I_{PSV}	–	–	–	0.1	μA	1
VC1 pin current	I_{VC1}	–	–	0.25	0.4	μA	1
VC2 pin current	I_{VC2}	–	–0.4	0.05	0.4	μA	1
VC3 pin current	I_{VC3}	–	–0.4	–0.1	0.4	μA	1
VC4 pin current	I_{VC4}	–	–0.4	–0.1	0.4	μA	1
VC5 pin current	I_{VC5}	–	–0.4	–0.1	0.4	μA	1
PSI pin current "H"	I_{PSIH}	–	–400	–200	–100	nA	1
PSI pin current "L"	I_{PSIL}	–	100	200	400	nA	1
Output pin							
CO pin voltage "H"	V_{COH}	4-serial cell	–	–	V_{DD}	V	1
		5-serial cell	–	$V_{VC2} - 0.5$	V_{VC2}	V	1
DO pin voltage "H"	V_{DOH}	4-serial cell	–	–	V_{DD}	V	1
		5-serial cell	–	$V_{VC2} - 0.5$	V_{VC2}	V	1
CO pin source current	I_{COH}	–	10	–	–	μA	1
CO pin sink current	I_{COL}	–	180	200	–	μA	1
DO pin source current	I_{DOH}	–	10	–	–	μA	1
DO pin sink current	I_{DOL}	–	1700	2000	–	μA	1
Temperature detection							
High temperature charge-discharge inhibition temperature	T_{HCD}	–	$T_{HCD} - 3$	T_{HCD}	$T_{HCD} + 3$	°C	1
High temperature charge inhibition temperature	T_{HC}	–	$T_{HC} - 3$	T_{HC}	$T_{HC} + 3$	°C	1
Low temperature charge inhibition temperature	T_{LC}	–	$T_{LC} - 3$	T_{LC}	$T_{LC} + 3$	°C	1
Low temperature charge-discharge inhibition temperature	T_{LCD}	–	$T_{LCD} - 3$	T_{LCD}	$T_{LCD} + 3$	°C	1
Hysteresis temperature	T_{HYS}	–	$T_{HYS} - 2$	T_{HYS}	$T_{HYS} + 2$	°C	1
Continuous detection / release count	N	–	–	N	–	–	1
Charge inhibition judgment voltage	V_{CHG}	–	1	3	5	mV	1

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged as follows.

L: [V_{CO}, V_{DO}] ≤ V_{DS} × 0.1 V
H: [V_{CO}, V_{DO}] > V_{DS} × 0.1 V

Remark V_{DS}: Input voltage between VDD pin and VSS pin (V1 + V2 + V3 + V4 + V5)

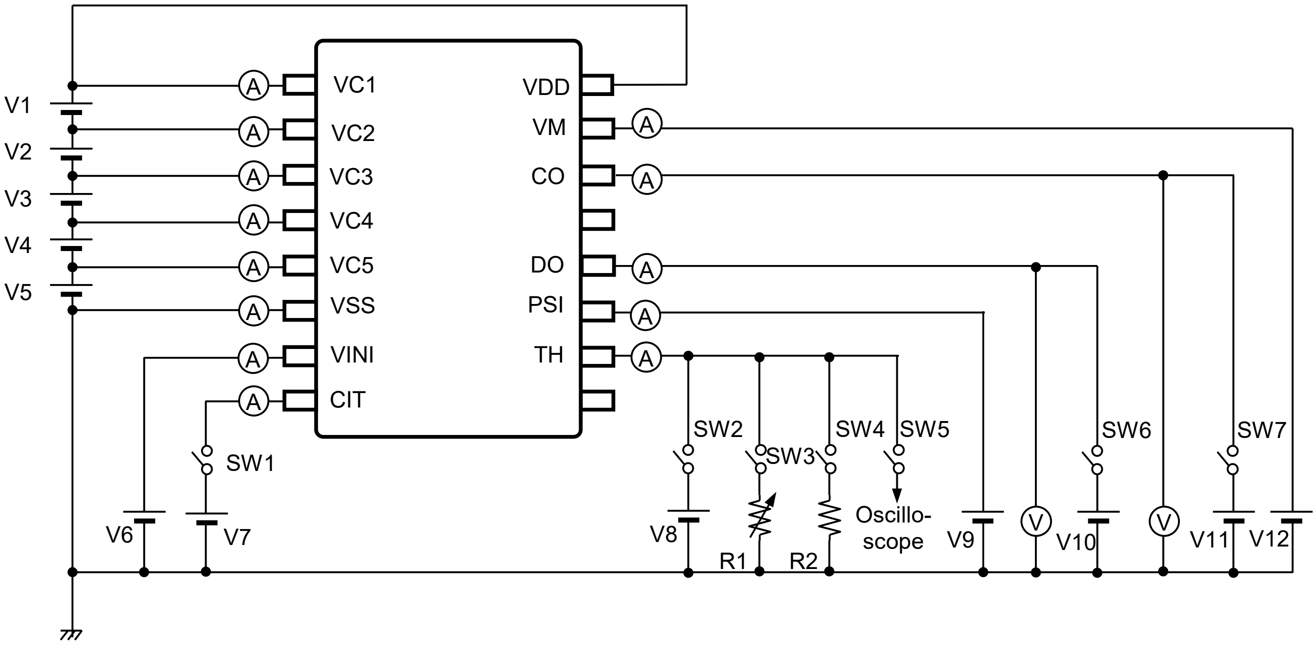


Figure 4 Test circuit 1

This section provides explanations of Test items using Test circuit 1.
Perform each test after setting as shown in **Table 9**.

Table 9 Initial Setting of Test Circuit 1 (1 / 2)

Symbol	V1	V2	V3	V4	V5	V6	V7	V8	V9	V10	V11	V12
Setting	3.5 V	3.5 V	3.5 V	3.5 V	3.5 V	0 V	0 V	0.25 V	V_{DS}	–	–	0 V

Table 9 Initial Setting of Test Circuit 1 (2 / 2)

Symbol	SW1	SW2	SW3	SW4	SW5	SW6	SW7	R1	R2
Setting	ON	ON	OFF	OFF	OFF	OFF	OFF	NTC	1 kΩ

1. Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn})

Overcharge detection voltage 1 (V_{CU1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting V1 = V2 = V3 = V4 = V5 = V_{CUn} – 0.05 V. Overcharge release voltage 1 (V_{CL1}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased after setting V2 = V3 = V4 = V5 = V_{CLn} – 0.05 V, V12 = 0.2 V.
Overcharge detection voltage n (V_{CUn}) and overcharge release voltage n (V_{CLn}) (n = 2 to 5) can be determined in the same way as when n = 1.

2. Overdischarge detection voltage n (V_{DLn}), overdischarge release voltage n (V_{DUn})

Overdischarge detection voltage 1 (V_{DL1}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased. Overdischarge release voltage 1 (V_{DU1}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased after setting V12 = 0.2 V. Overdischarge detection voltage n (V_{DLn}) and overdischarge release voltage n (V_{DUn}) (n = 2 to 5) can be determined in the same way as when n = 1.

3. Discharge overcurrent 1 detection voltage (V_{DIOV1})

Discharge overcurrent 1 detection voltage (V_{DIOV1}) is defined as the voltage V6 at which CIT pin current changes from the direction of flowing into the IC to the direction of flowing out from the IC when the voltage V6 is gradually increased after setting V7 = 0.01 V.

4. Discharge overcurrent 2 detection voltage (V_{DIOV2})

Discharge overcurrent 2 detection voltage (V_{DIOV2}) is defined as the voltage V6 at which V_{DO} goes from "H" to "L" when the voltage V6 is gradually increased after setting V12 = 0.5 V.

5. Load short-circuiting detection voltage (V_{SHORT})

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V6 at which delay time from when V6 is increased after setting V12 = 0.5 V to when V_{DO} goes from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}).

6. Charge overcurrent detection voltage (V_{CIOV})

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V6 at which V_{CO} goes from "H" to "L" when the voltage V6 is gradually decreased after setting V12 = −0.1 V.

7. CIT pin charge current (I_{CIT}), CIT pin detection voltage (V_{CIT})

CIT pin charge current (I_{CIT}) is defined as the CIT pin current when setting V6 = (V_{DIOV1} + V_{DIOV2}) / 2.
CIT pin detection voltage (V_{CIT}) is defined as the voltage V7 at which V_{DO} goes from "H" to "L" when the voltage V7 is then gradually increased.

8. Overcharge detection delay time (t_{CU})

Overcharge detection delay time (t_{CU}) is the time period from when the voltage V1 exceeds V_{CU1} after setting V1 = V2 = V3 = V4 = V5 = 3.5 V till when V_{CO} goes from "H" to"L".

9. Overdischarge detection delay time (t_{DL})

Overdischarge detection delay time (t_{DL}) is the time period from when the voltage V1 falls below V_{DL1} after setting V1 = V2 = V3 = V4 = V5 = 3.5 V till when V_{DO} goes from "H" to "L".

10. Discharge overcurrent 2 detection delay time (t_{DIOV2})

Discharge overcurrent 2 detection delay time (t_{DIOV2}) is the time period from when the voltage V6 exceeds V_{DIOV2} after setting V12 = 0.5 V till when V_{DO} changes from "H" to "L".

11. Load short-circuiting detection delay time (t_{SHORT})

Load short-circuiting detection delay time (t_{SHORT}) is the time period from when the voltage V6 exceeds V_{SHORT} after setting V12 = 0.5 V till when V_{DO} changes from "H" to "L".

12. Charge overcurrent detection delay time (t_{CIOV})

Charge overcurrent detection delay time (t_{CIOV}) is the time period from when the voltage V6 falls below V_{CIOV} after setting V12 = −0.1 V till when V_{CO} changes from "H" to "L".

13. PSI pin response time (t_{PSI})

PSI pin response time (t_{PSI}) is the time period from when the voltage V9 is changed to 0 V till when V_{DO} changes from "H" to "L".

14. 0 V battery charge starting charger voltage (V_{0CHA}) (0 V battery charge enabled)

This IC reaches the overdischarge status after setting V1 = V_{DL1} − 0.1V. Then set V1 = V2 = V3 = V4 = V5 = 0 V and V8 = 0 V. 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V12 at which I_{CO} exceeds 1.0 μA when the voltage V12 is then gradually decreased after setting SW7 ON, and V11 = V12 = −0.5 V.

15. 0 V battery charge inhibition battery voltage n (V_{0INHn}) (0 V battery charge inhibited)

0 V battery charge inhibition battery voltage 1 (V_{0INH1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting V1 = V2 = V3 = V4 = V5 = V_{DLn} – 0.1 V.
0 V battery charge inhibition battery voltage n (V_{0INHn}) (n = 2 to 5) can be determined in the same way as when n = 1.

16. Resistance between VM pin and VDD pin (R_{VMD})

Resistance between VM pin and VDD pin (R_{VMD}) is defined by $R_{VMD} = (V_{DS} + 0.1) / I_{VM}$ using I_{VM} when setting V1 = V2 = V3 = V4 = V5 = 1.5 V and V12= −0.1 V.

17. Resistance between VM pin and VSS pin (R_{VMS})

Resistance between VM pin and VSS pin (R_{VMS}) is defined by R_{VMS} = V12 / I_{VM} using I_{VM} when setting V6 = 1.0 V and V12 = 2.0 V.

18. PSI pin reverse voltage "H" (V_{PSIH})

PSI pin reverse voltage "H" (V_{PSIH}) is defined as the voltage V9 at which V_{DO} goes from "L" to "H" when the voltage V9 is gradually increased after setting V9 = 0 V.

19. PSI pin reverse voltage "L" (V_{PSIL})

PSI pin reverse voltage "L" (V_{PSIL}) is defined as the voltage V9 at which V_{DO} goes from "H" to "L" when the voltage V9 is gradually decreased.

20. Current consumption during operation (I_{OPE})

Current consumption during operation (I_{OPE}) is defined as the sum of VSS pin current, VM pin current and VINI pin current after setting SW2 OFF, SW3 ON and SW1 OFF.

21. Current consumption during power-down (I_{PDN})

Current consumption during power-down (I_{PDN}) is defined as I_{VSS} under the setting conditions of V1 = V2 = V3 = V4 = V5 = 1.5 V, V8 = 0 V and V12 = V_{DS}.

22. Current consumption during power-saving (I_{PSV})

Current consumption during power-saving (I_{PSV}) is defined as I_{VSS} under the setting conditions of V8 = 0 V, V12 = V_{DS} and V9 = 0 V.

23. PSI pin current "H" (I_{PSIH}), PSI pin current "L" (I_{PSIL})

PSI pin current "H" (I_{PSIH}) is defined as I_{PSI} when setting V9 = V_{DS} − 1 V after setting V9 = V_{DS}.
PSI pin current "L" (I_{PSIL}) is defined as I_{PSI} when setting V9 = ($V_{PSIH} + V_{PSIL}$) / 2 after setting V9 = 0 V.

24. CO pin voltage "H" (V_{COH}), CO pin source current (I_{COH})

CO pin voltage "H" (V_{COH}) is defined as CO pin voltage (V_{CO}) in the settings shown in **Table 9**. CO pin source current (I_{COH}) is defined as I_{CO} when setting V11 = V_{COH} − 0.5 V and SW7 ON.

25. CO pin sink current (I_{COL})

CO pin sink current (I_{COL}) is defined as I_{CO} when setting V1 = V_{CU1} + 0.1 V, V11 = 0.5 V and SW7 ON.

26. DO pin voltage "H" (V_{DOH}), DO pin source current (I_{DOH})

DO pin voltage "H" (V_{DOH}) is defined as DO pin voltage (V_{DO}) in the settings shown in **Table 9**. DO pin source current (I_{DOH}) is defined as I_{DO} when setting V10 = V_{DOH} – 0.5 V and SW6 ON.

27. DO pin sink current (I_{DOL})

DO pin sink current (I_{DOL}) is defined as I_{DO} when setting V1 = V_{DL1} – 0.1 V, V10 = 0.5 V and SW6 ON.

28. High temperature charge-discharge inhibition temperature (T_{HCD}), high temperature charge-discharge inhibition release temperature (T_{RHCD})

Set the SW2 OFF and the SW3 ON, decrease R1 = R_{NTC} [kΩ] gradually, and then substitute R1 when V_{CO} and V_{DO} go from "H" to "L" into equation (1). Temperature T [°C] obtained from the calculation result is defined as high temperature charge-discharge inhibition temperature (T_{HCD}). Subsequently, increase R1 gradually, and substitute R1 when V_{CO} and V_{DO} go from "L" to "H" into equation (1). Temperature T [°C] obtained from the calculation result is defined as high temperature charge-discharge inhibition release temperature (T_{RHCD}). The difference between T_{HCD} and T_{RHCD} is defined as hysteresis temperature (T_{HYS}). When this IC has the setting of high temperature charge inhibition temperature (T_{HC}) as well, only V_{DO} is switched as long as the detection temperature of an NTC thermistor is maintained at high temperature charge inhibition release temperature (T_{RHC}) or higher.

29. High temperature charge inhibition temperature (T_{HC}), high temperature charge inhibition release temperature (T_{RHC})

Set the SW2 OFF and the SW3 ON, decrease R1 = R_{NTC} [kΩ] gradually, and then substitute R1 when V_{CO} goes from "H" to "L" into equation (1). Temperature T [°C] obtained from the calculation result is defined as high temperature charge inhibition temperature (T_{HC}). Subsequently, increase R1 gradually, and substitute R1 when V_{CO} goes from "L" to "H" into equation (1). Temperature T [°C] obtained from the calculation result is defined as high temperature charge inhibition release temperature (T_{RHC}). The difference between T_{HC} and T_{RHC} is defined as hysteresis temperature (T_{HYS}).

30. Low temperature charge inhibition temperature (T_{LC}), low temperature charge inhibition release temperature (T_{RLC})

Set the SW2 OFF and the SW3 ON, increase R1 = R_{NTC} [kΩ] gradually, and then substitute R1 when V_{CO} goes from "H" to "L" into equation (1). Temperature T [°C] obtained from the calculation result is defined as low temperature charge inhibition temperature (T_{LC}). Subsequently, decrease R1 gradually, and substitute R1 when V_{CO} goes from "L" to "H" into equation (1). Temperature T [°C] obtained from the calculation result is defined as low temperature charge inhibition release temperature (T_{RLC}). The difference between T_{RLC} and T_{LC} is defined as hysteresis temperature (T_{HYS}).

31. Low temperature charge-discharge inhibition temperature (T_{LCD}), low temperature charge-discharge inhibition release temperature (T_{RLCD})

Set the SW2 OFF and the SW3 ON, increase R1 = R_{NTC} [kΩ] gradually, and then substitute R1 when V_{CO} and V_{DO} go from "H" to "L" into equation (1). Temperature T [°C] obtained from the calculation result is defined as low temperature charge-discharge inhibition temperature (T_{LCD}). Subsequently, decrease R1 gradually, and substitute R1 when V_{DO} goes from "L" to "H" into equation (1). Temperature T [°C] obtained from the calculation result is defined as low temperature charge-discharge inhibition release temperature (T_{RLCD}). The difference between T_{RLCD} and T_{LCD} is defined as hysteresis temperature (T_{HYS}). When this IC has the temperature setting of low temperature charge inhibition temperature (T_{LC}) as well, only V_{DO} is switched as long as the detection temperature of an NTC thermistor is maintained at low temperature charge inhibition release temperature (T_{RLC}) or lower.

$$T\ [°C] = \frac{1}{\frac{1}{B\ [K]} \times \log_e\left(\frac{R_1\ [k\Omega]}{R_{NTC}\ [k\Omega]}\right) + \frac{1}{25\ [°C] + 273.15}} - 273.15 \qquad (1)$$

$$R_{TDET}\ [k\Omega] = R_{NTC}\ [k\Omega]\ \exp\left\{B\ [K]\left(\frac{1}{T_{DET}\ [°C] + 273.15} - \frac{1}{25\ [°C] + 273.15}\right)\right\} \qquad (2)$$

Remark Refer to **Table 6** for R_{NTC} [kΩ] and B [K].
Resistance R_{TDET} [kΩ] of an NTC thermistor at T_{DET} [°C] can be calculated by the equation (2).

32. Sampling wait time (t_{SLEEP})

After setting SW2 OFF and setting SW3 and SW5 ON, time period when the output is "L" between continuous voltage pulses output from the TH pin (V_{TH}) is defined as sampling wait time (t_{SLEEP}).

33. Continuous detection / release count (N)

After setting SW2 OFF and setting SW3 and SW5 ON, SW4 is switched from OFF to ON. The number of pulses from the SW4 switching until V_{CO} goes to "L" is continuous detection / release count (N).

34. Charger detection voltage (V_{CHG})

After setting SW2 OFF and SW3 ON, R1 = R_{NTC} [kΩ] is set to resistance corresponding to temperature between high charge inhibition temperature (T_{HC}) and high charge-discharge inhibition temperature (T_{HCD}). Charger detection voltage (V_{CHG}) is defined as the voltage V12 at which V_{CO} goes from "H" to "L" when the voltage V12 is gradually decreased after setting V12 = 0.5 V.

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Example**".

1. Normal status

The status when the CO pin output voltage (V_{CO}) = "H" and DO pin output voltage (V_{DO}) = "H" is the normal status. CO pin voltage "H" (V_{COH}) is the voltage V_{CO} when the V_{CO} is "H". DO pin voltage "H" (V_{DOH}) is the voltage V_{DO} when the V_{DO} is "H".
All the conditions mentioned below should be satisfied for returning to the normal status.

- The voltage of each of the batteries is in the range from the overcharge detection voltage n (V_{CUn}) to overdischarge detection voltage n (V_{DLn}).
- The VINI pin voltage is in the range of the charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent 1 detection voltage (V_{DIOV1}).
- The PSI pin voltage is higher than the PSI pin reverse voltage "H" (V_{PSIH}).
- The temperature of an NTC thermistor is in the range between low temperature charge inhibition temperature (T_{LC}) and high temperature charge inhibition temperature (T_{HC}).

Caution After a battery is connected, there may be cases when discharging cannot be performed. In this case, this IC returns to the normal status when any of the following conditions is satisfied.

(1) Connecting a charger
(2) Shorting between the VM pin and the VSS pin
(3) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0$ V $\rightarrow V_{DS}$

2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n (V_{CUn}) and the status continues for the overcharge detection delay time (t_{CU})*1 or longer, the CO pin changes to VM pin voltage. This is the overcharge status. In this case, the charge control FET is turned off and charging is stopped.

The overcharge status is released if either condition mentioned below is satisfied.

(1) $V_{VM} < 0.3$ V typ., and voltage of all batteries $\leq V_{CLn}$
(2) $V_{VM} \geq 0.3$ V typ., and voltage of all batteries $\leq V_{CUn}$

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{CUn}: Overcharge detection voltage n (n = 1, 2, 3, 4, 5)
V_{CLn}: Overcharge release voltage n (n = 1, 2, 3, 4, 5)

3. Overdischarge status

When the voltage of any of the batteries decreases to the overdischarge detection voltage n (V_{DLn}) or lower and the status continues for the overdischarge detection delay time (t_{DL})*1 or longer, the DO pin changes to the V_{SS} level. This is the overdischarge status. The discharge control FET is turned off and discharging is stopped.

The overdischarge status is released if either condition mentioned below is satisfied.

(1) $V_{VM} \le 0$ V typ., and voltage of all batteries $\ge V_{DLn}$
(2) $V_{VM} > 0$ V typ., and voltage of all battery $\ge V_{DUn}$

***1.** Refer to "**6. Delay time setting**" for details.

Remark V_{VM}: VM pin voltage
V_{DLn}: Overdischarge detection voltage n (n = 1, 2, 3, 4, 5)
V_{DUn}: Overdischarge release voltage n (n = 1, 2, 3, 4, 5)

3. 1 With power-down function

When this IC reaches the overdischarge status, the VM pin is pulled up to the V_{DD} level by a resistance between VM pin and VDD pin (R_{VMD}). If the VM pin voltage changes to 0.7 V typ. or higher, the power-down function starts to operate and most operations in this IC halt. The CO pin changes to VM pin voltage. In this case, the charge control FET is turned off and charging is stopped.
By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

4. Discharge overcurrent status

When the discharge current increases to a certain value or more, the VINI pin voltage increases to the level of discharge overcurrent 1 detection voltage (V_{DIOV1}) or higher. If the condition continues for the discharge overcurrent 1 detection delay time (t_{DIOV1})*1 or longer, the DO pin changes to the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off and discharging is stopped.
Discharge overcurrent is detected at the following three levels: V_{DIOV1}, V_{DIOV2}, and V_{SHORT}. When discharge overcurrent 2 detection voltage (V_{DIOV2}) and load short-circuiting detection voltage (V_{SHORT}) are detected, the same operations as V_{DIOV1} detection are performed.

4. 1 Release condition of discharge overcurrent status "Load disconnection"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in this IC. However, the VM pin voltage is the V_{DD} level due to the load as long as the load is connected. When the load is disconnected, the VM pin voltage returns to the Vss level. When the VM pin voltage returns to V_{DS} / 3 or lower, this IC releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

4. 2 Release condition of discharge overcurrent status "Charger connection"

Under the discharge overcurrent status, VDD pin and VM pin are shorted by R_{VMD} in this IC. When a battery is connected to a charger and VM pin voltage returns to V_{DIOV1} or lower, this IC releases the discharge overcurrent status.
R_{VMS} is not connected in the discharge overcurrent status.

5. Charge overcurrent status

When the charge current increases to a certain value or more, the VINI pin voltage decreases to the level of charge overcurrent detection voltage (V_{CIOV}) or lower. If the status continues for the charge overcurrent detection delay time (t_{CIOV})[*1] or longer, the CO pin voltage changes to the VM pin voltage. This is the charge overcurrent status. In this case, the charge control FET is turned off and charging is stopped. The VM pin is pulled up to the V_{DD} level by a resistance between VM pin and VDD pin (R_{VMD}).

The charge overcurrent status is released if the VM pin voltage increases 0.3 V typ. or higher.

***1.** Refer to "**6. Delay time setting**" for details.

6. Delay time setting

Users are able to set delay time for the period from when this IC detects change in the voltage of any of the batteries or the VINI pin until when it outputs to the CO pin or DO pin. The discharge overcurrent 1 detection delay time (t_{DIOV1}) is determined by constant current in this IC and an external capacitor. The other detection delay times are fixed internally.

6. 1 Other than discharge overcurrent 1 detection delay time (t_{DIOV1})

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV2} and t_{SHORT} start when V_{DIOV2} is detected. When V_{SHORT} is detected over t_{SHORT} after the detection of V_{DIOV2}, this IC turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

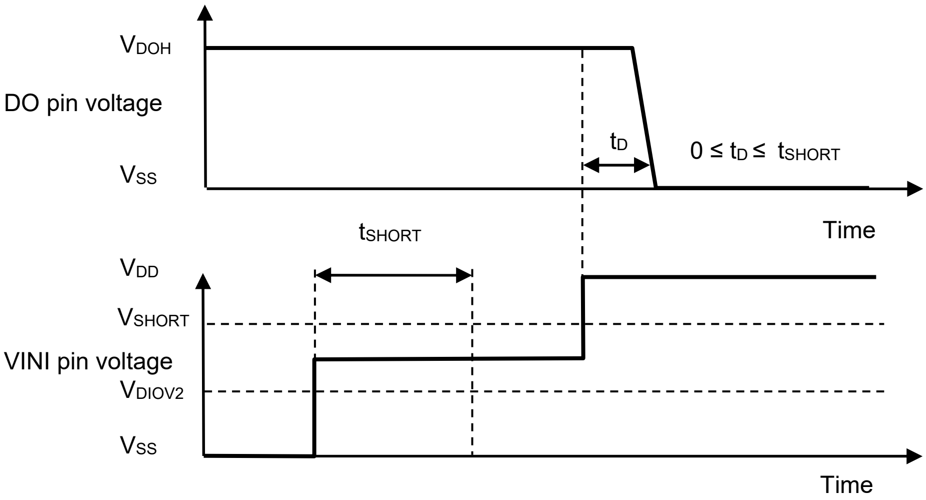


Figure 5

6. 2 Discharge overcurrent 1 detection delay time (t_{DIOV1})

In the discharge overcurrent 1 detection, when the VINI pin voltage increases to discharge overcurrent 1 detection voltage (V_{DIOV1}) or higher, the internal circuit of this IC starts charging to an external capacitor connected to the CIT pin via the CIT pin current (I_{CIT}) = 120 nA typ. When the CIT pin voltage increases to the CIT pin detection voltage (V_{CIT}) or higher, the DO pin voltage changes to Vss level. This period is discharge overcurrent 1 detection delay time (t_{DIOV1}).

t_{DIOV1} is calculated by the following formula.
t_{DIOV1} [s] = C_{CIT} [F] × V_{CIT} [V] / I_{CIT} [A]

If C_{CIT} = 0.01 μF, t_{DIOV1} is calculated as follows:
t_{DIOV1} [s] = 0.01 μF × 1.2 V typ. / 120 nA typ. = 100 ms typ.

7. 0 V Battery charge function

Regarding how to charge a self-discharged battery (0 V battery), users are able to select either function mentioned below.

(1) 0 V battery charge enabled
A 0 V battery is charged when charger voltage is higher than the 0 V battery charge starting charger voltage (V_{0CHA}).
(2) 0 V battery charge inhibited
A 0 V battery is not charged when the voltage of any of the batteries is the 0 V battery charge inhibition battery voltage n (V_{0INHn}) or lower.

Caution When the VDD pin voltage is lower than the minimum value of operation voltage between the VDD pin and VSS pin (V_{DSOP}), this IC's operation is not assured.

Remark n = 1, 2, 3, 4, 5

8. PSI pin

When the PSI pin is activated, the power-saving function starts to operate, and most operations halt. In this case, the CO pin changes to the VM pin level, and DO pin changes to the V_{SS} level.

Table 10 Status Set by PSI Pin

PSI pin	CO pin	DO pin
$V_{PSIH} \leq$ PSI pin voltage $\leq V_{DD}$ level	"H"	"H"
$V_{PSIL} <$ PSI pin voltage $< V_{PSIH}$	Maintains the status	Maintains the status
V_{SS} level $\leq$ PSI pin voltage $\leq V_{PSIL}$	VM pin level	V_{SS} level

This IC is initialized and becomes the normal status by deactivating the PSI pin after activating PSI pin and enabling the power-saving function. As a result, each detection operation is carried out after returning to the normal status.

9. Temperature protection status (high temperature charge-discharge inhibition status, high temperature charge inhibition status, low temperature charge inhibition status, low temperature charge-discharge inhibition status)

This IC carries out intermittent operation in the normal status.
This IC monitors the temperature of an NTC thermistor for the sampling time (t_{AWAKE}) of 8 ms typ. after sampling wait time (t_{SLEEP}).

9. 1 High temperature charge-discharge inhibition status

When the temperature of an NTC thermistor is equal to or higher than high temperature charge-discharge inhibition temperature (T_{HCD}) and the condition continues until the number of the temperature sampling reaches continuous detection / release count (N), this IC becomes the high temperature charge-discharge inhibition status.
Under the high temperature charge-discharge inhibition status, both the charge control FET and discharge control FET are turned off, and charging and discharging are stopped.
This IC releases the high temperature charge-discharge inhibition status when the temperature of the NTC thermistor falls below T_{HCD} by hysteresis temperature (T_{HYS}) and the condition continues until the number of the temperature sampling reaches N.

9. 2 High temperature charge inhibition status

When the temperature of an NTC thermistor is equal to or higher than high temperature charge inhibition temperature (T_{HC}) and the condition continues until the number of the temperature sampling reaches N, this IC becomes the high temperature charge inhibition status.

- When a battery is not connected to a charger and the VM pin voltage > 3 mV typ., the charge control FET is not turned off.
- When a battery is connected to a charger and 3 mV typ. ≥ the VM pin voltage, the charge control FET is turned off and charging is stopped.

This IC releases the high temperature charge inhibition status when the temperature of the NTC thermistor falls below T_{HC} by T_{HYS} and the condition continues until the number of the temperature sampling reaches N.

9. 3 Low temperature charge inhibition status

When the temperature of an NTC thermistor is equal to or lower than low temperature charge inhibition temperature (T_{LC}) and the condition continues until the number of the temperature sampling reaches N, this IC becomes the low temperature charge inhibition status.

- When a battery is not connected to a charger and the VM pin voltage > 3 mV typ., the charge control FET is not turned off.
- When a battery is connected to a charger and 3 mV typ. ≥ the VM pin voltage, the charge control FET is turned off and charging is stopped.

This IC releases the low temperature charge inhibition status when the temperature of the NTC thermistor exceeds T_{LC} by T_{HYS} and the condition continues until the number of the temperature sampling reaches N.

9. 4 Low temperature charge-discharge inhibition status

When the temperature of an NTC thermistor is equal to or lower than low temperature charge-discharge inhibition temperature (T_{LCD}) and the condition continues until the number of the temperature sampling reaches N, this IC becomes the low temperature charge-discharge inhibition status.
Under the low temperature charge-discharge inhibition status, both the charge control FET and discharge control FET are turned off, and charging and discharging are stopped.
This IC releases the low temperature charge-discharge inhibition status when the temperature of the NTC thermistor exceeds T_{LCD} by T_{HYS} and the condition continues until the number of the temperature sampling reaches N.

■ Timing Charts

1. Overcharge detection, overdischarge detection

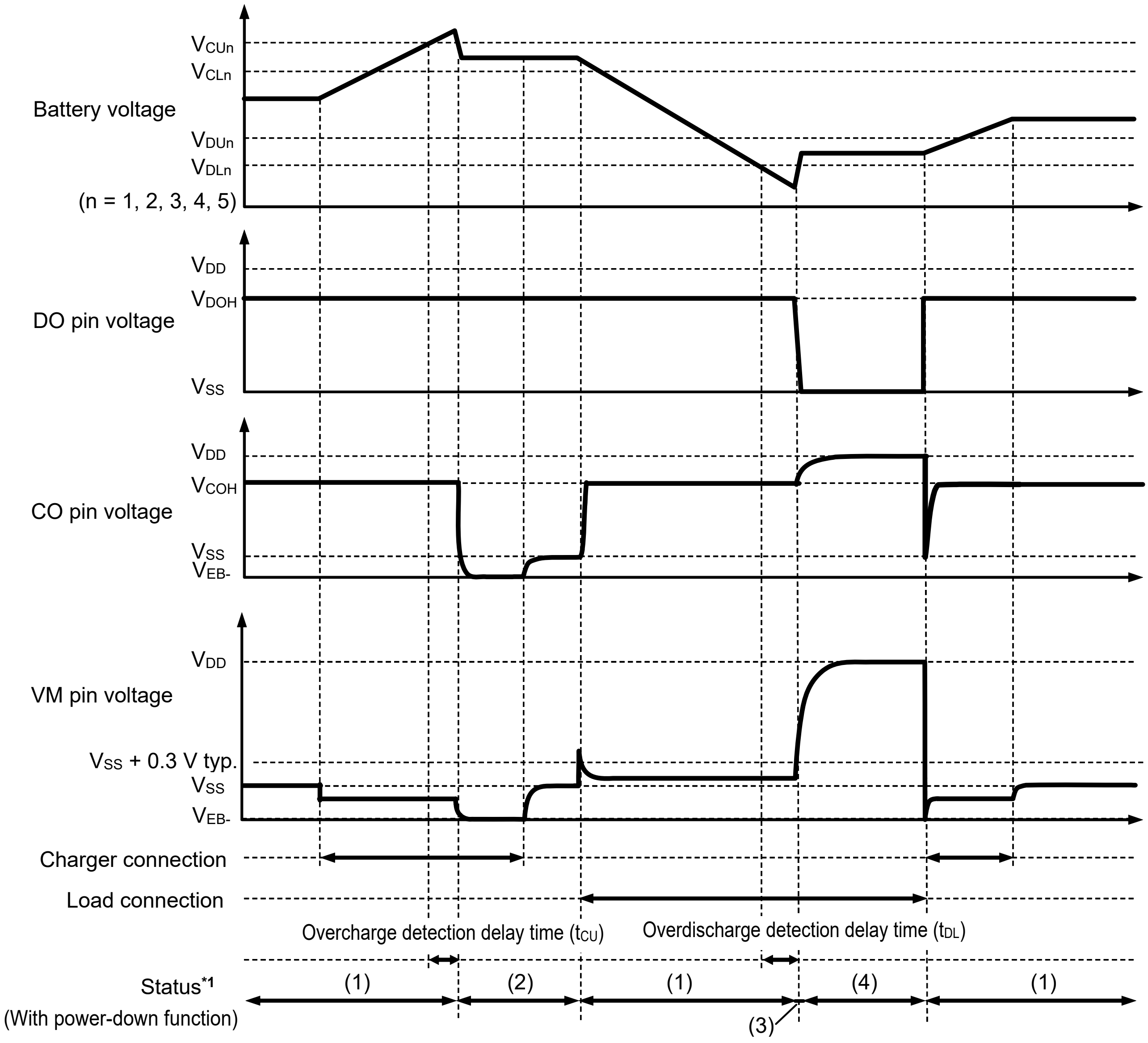


Figure 6

***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status
(4) : Power-down status

2. Discharge overcurrent detection

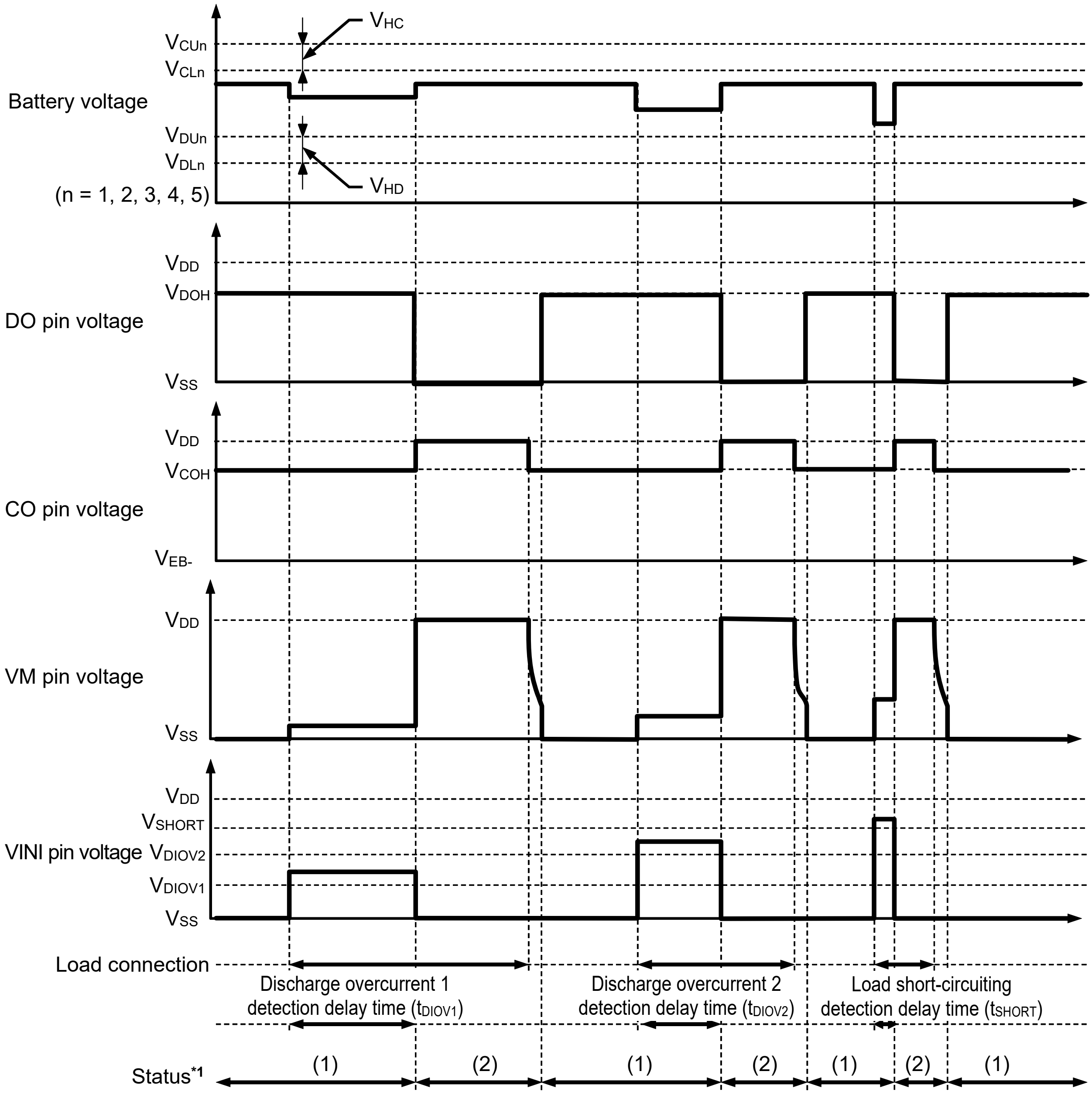


Figure 7

***1.** (1) : Normal status
(2) : Discharge overcurrent status

3. Charge overcurrent detection

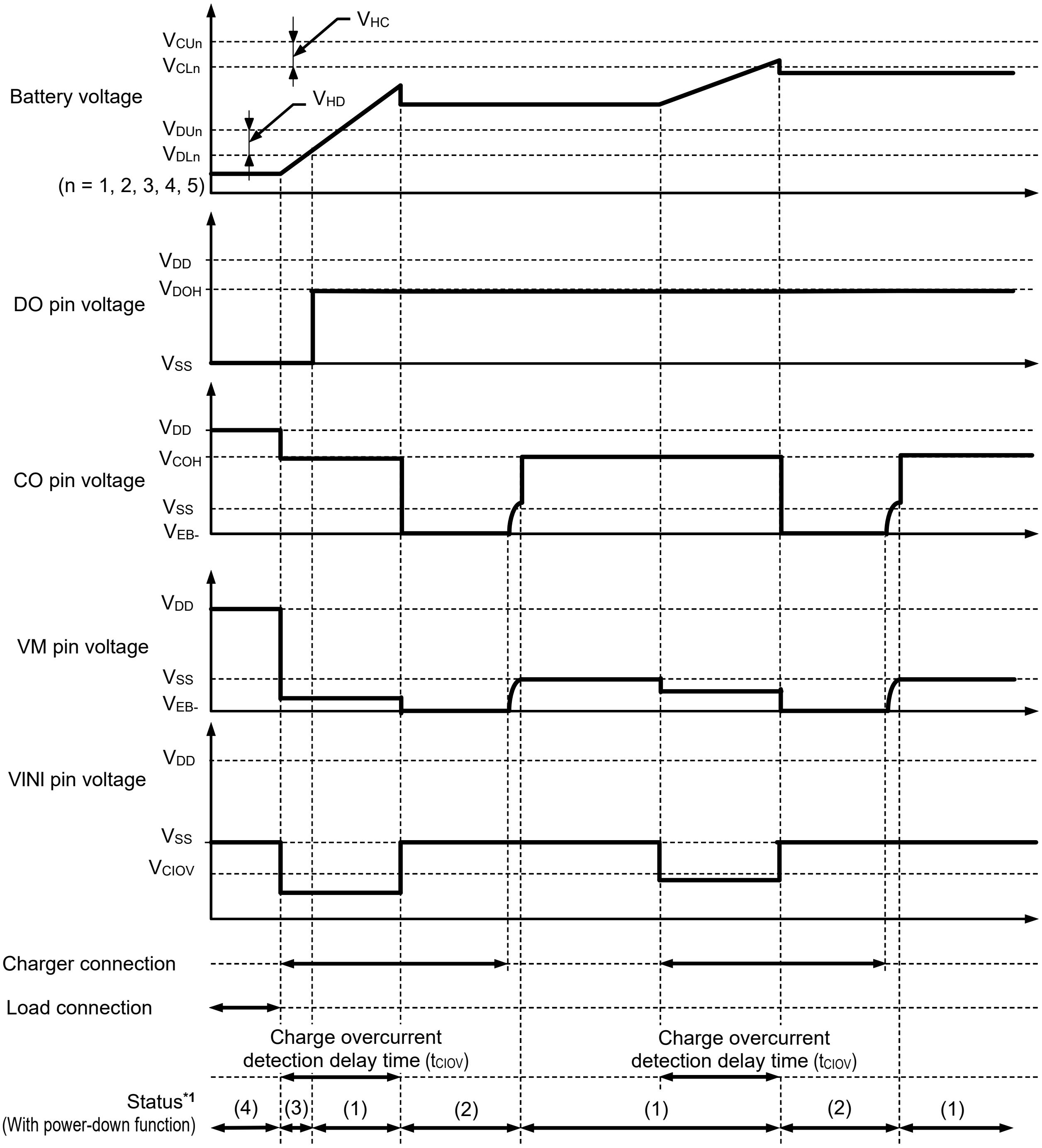


Figure 8

***1.** (1) : Normal status
(2) : Charge overcurrent status
(3) : Overdischarge status
(4) : Power-down status

4. Temperature protection operation

4. 1 High temperature charge inhibition temperature detection (Continuous detection / release count = 2)

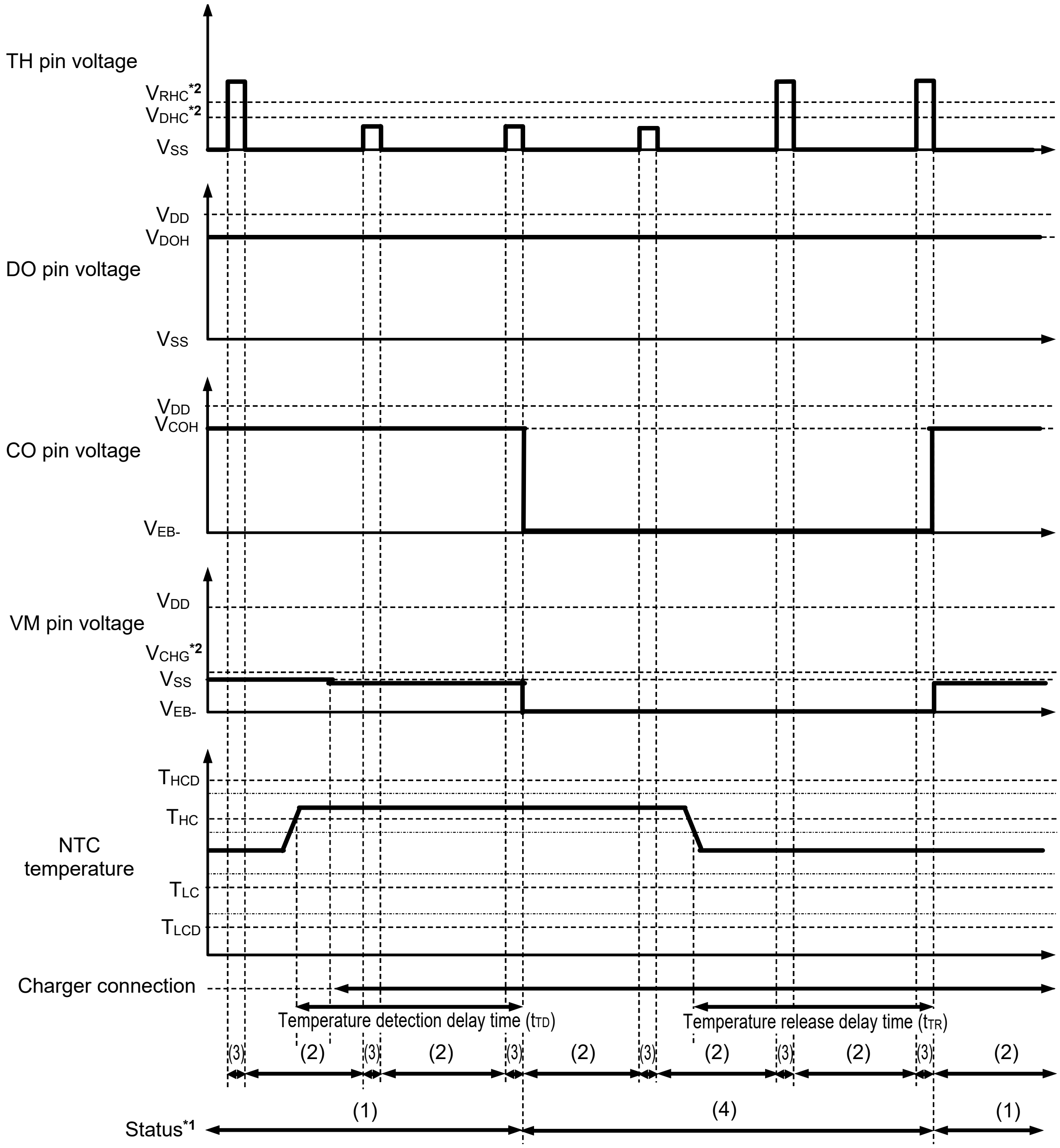


Figure 9

***1.** (1) : Normal status
(2) : Temperature detection sleep time
(3) : Temperature detection awake time
(4) : Temperature protection status

***2.** V_{DHC}: High temperature charge inhibition temperature detection voltage
V_{RHC}: High temperature charge inhibition temperature release voltage
V_{CHG}: Charger detection voltage

4. 2 High temperature charge-discharge inhibition temperature detection (Continuous detection / release count = 2)

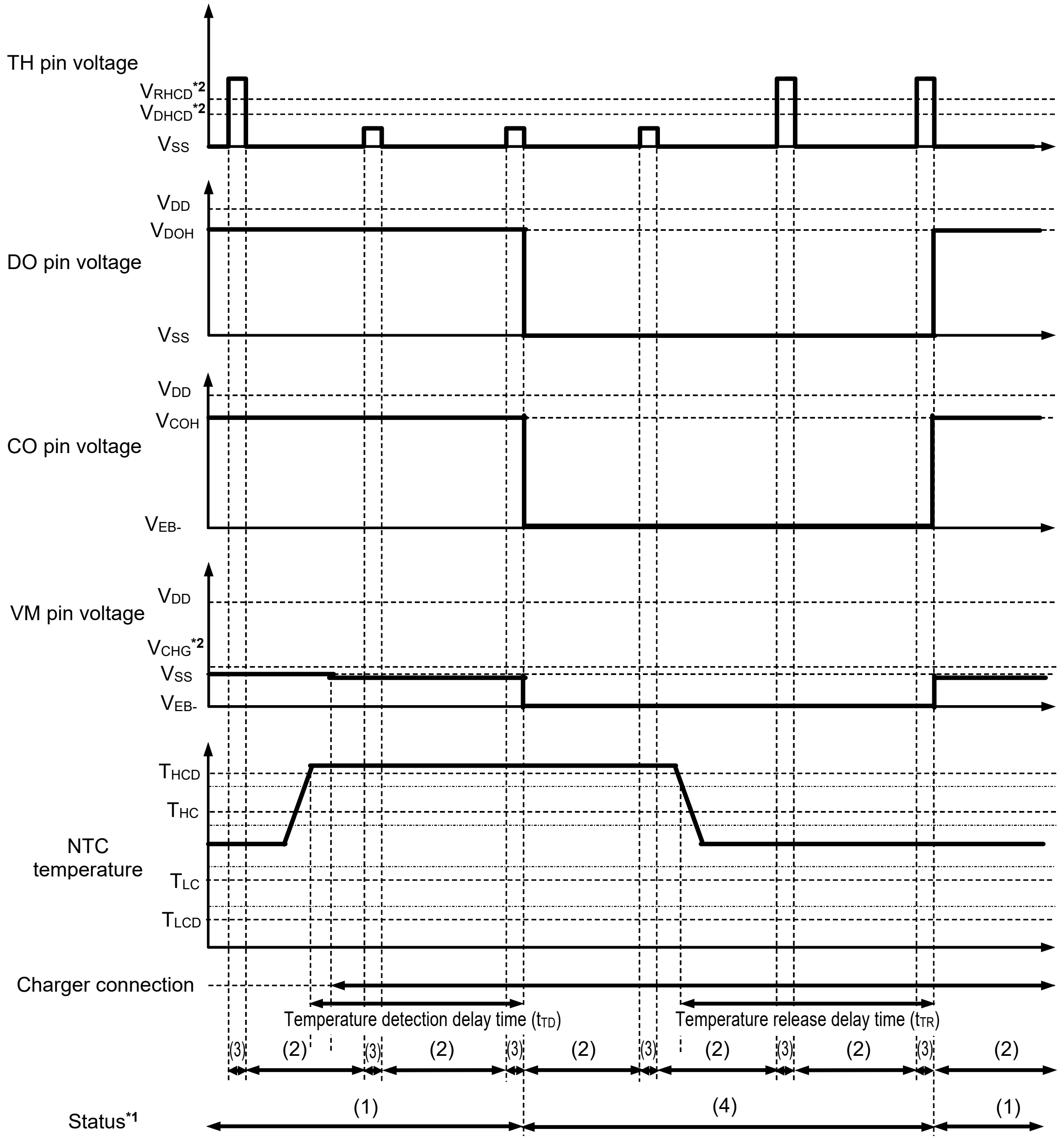


Figure 10

***1.** (1) : Normal status
(2) : Temperature detection sleep time
(3) : Temperature detection awake time
(4) : Temperature protection status

***2.** V_{DHCD}: High temperature charge-discharge inhibition temperature detection voltage
V_{RHCD}: High temperature charge-discharge inhibition temperature release voltage
V_{CHG}: Charger detection voltage

■ Connection Examples of Battery Protection IC

1. S-82C4A Series (4-serial cell)

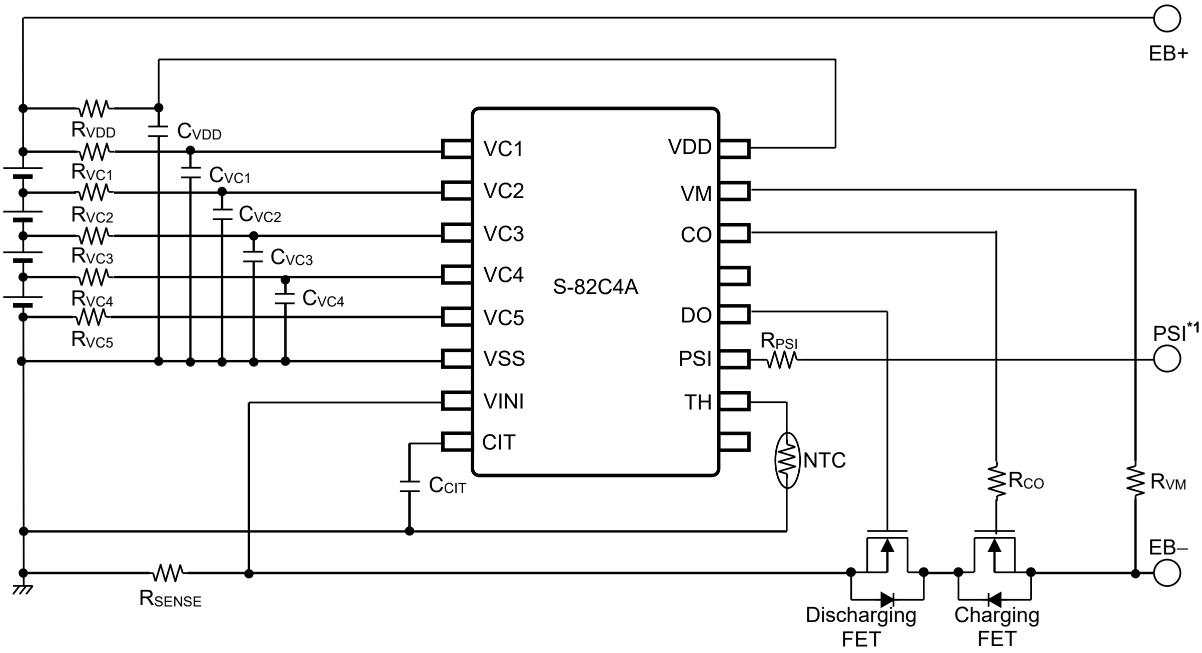


Figure 11

*1. If you do not use the power-saving function, connect the PSI pin to the VDD pin.

Remark Regarding the recommended values for external components, refer to "**Table 11 Constants for External Components**".

2. S-82C5A Series (5-serial cell)

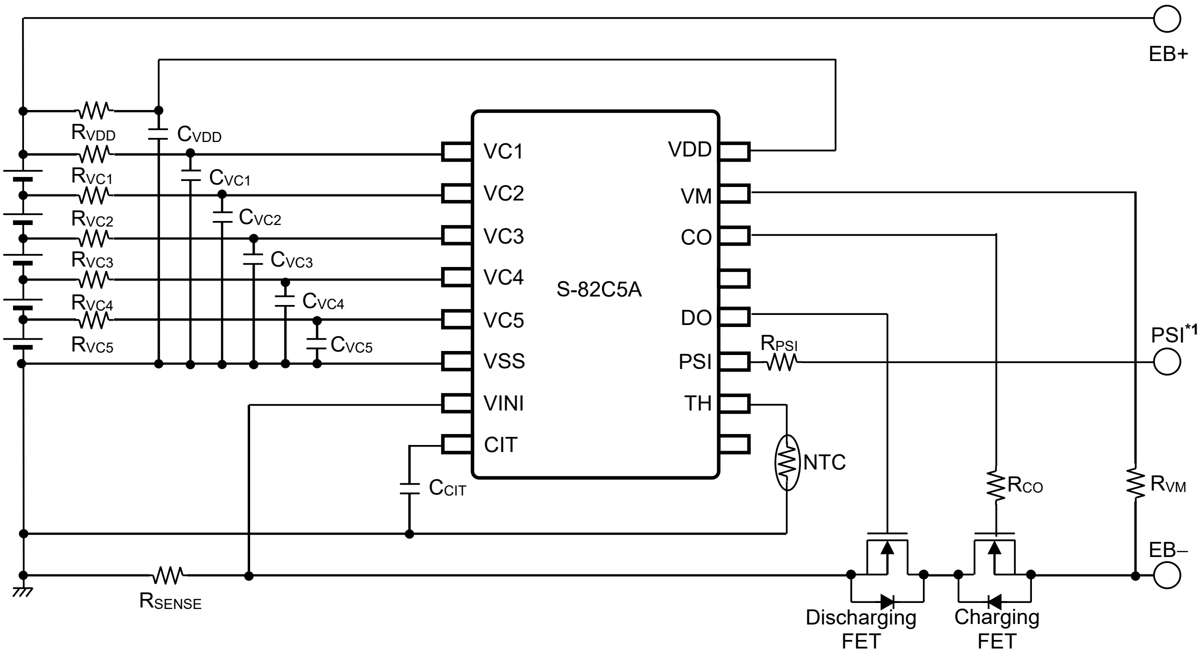


Figure 12

*1. If you do not use the power-saving function, connect the PSI pin to the VDD pin.

Remark Regarding the recommended values for external components, refer to "**Table 11 Constants for External Components**".

Table 11 Constants for External Components

Symbol	Typ.	Unit
R_{VDD}	100	Ω
R_{VCn} (n = 1, 2, 3, 4, 5)	1	kΩ
R_{PSI}	1	kΩ
R_{CO}	1	kΩ
R_{VM}	1	kΩ
NTC	10 or 100	kΩ
R_{SENSE}	–	mΩ
C_{VDD}	1	μF
C_{VCn} (n = 1, 2, 3, 4, 5)	0.1	μF
C_{CIT}	0.01 or more	μF

Caution 1. The constants may be changed without notice.

2. Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants when setting the filter constants between the VDD pin and VSS pin. Contact our sales representatives if setting the constants between the VDD pin and VSS pin to anything other than the recommended values.

3. It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.

- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed after a battery is connected. In this case, this IC returns to the normal status when any of the following conditions is satisfied.

  (1) Connecting a charger
  (2) Shorting between the VM pin and the VSS pin
  (3) Changing the PSI pin voltage to be V_{DS} → 0 V → V_{DS}

- If an overcharged battery and an overdischarged battery intermix, this IC will change to the overcharge and overdischarge statuses. Therefore, in this case, both charging and discharging are impossible.

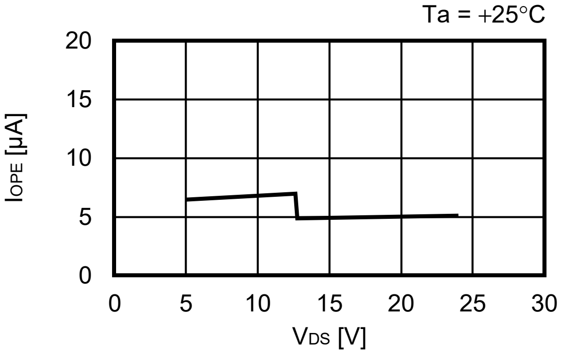
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

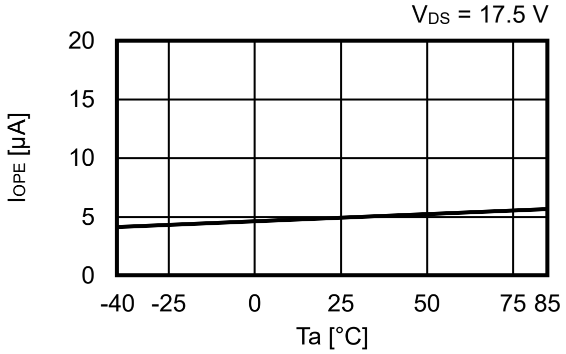
■ Characteristics (Typical Data)

1. Current consumption

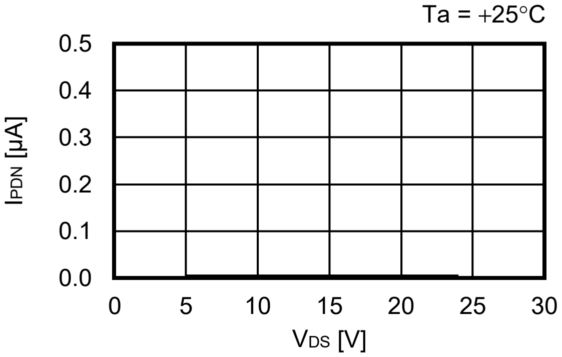
1. 1 I_{OPE} vs. V_{DS}



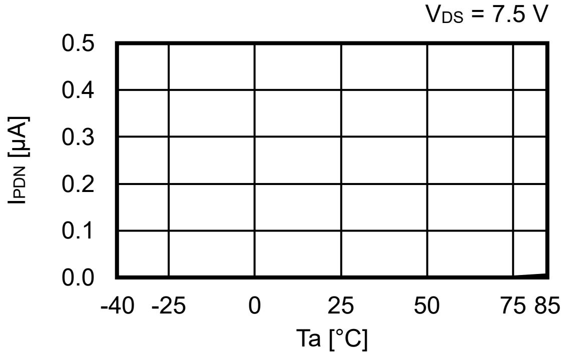
1. 2 I_{OPE} vs. Ta



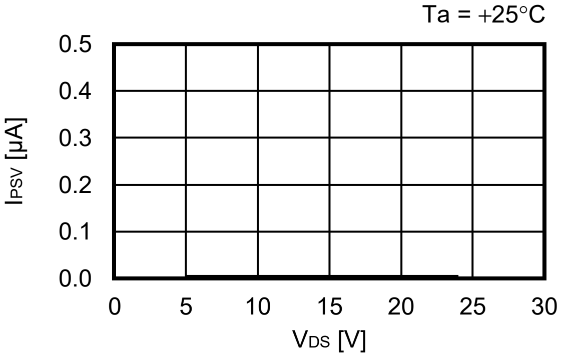
1. 3 I_{PDN} vs. V_{DS}



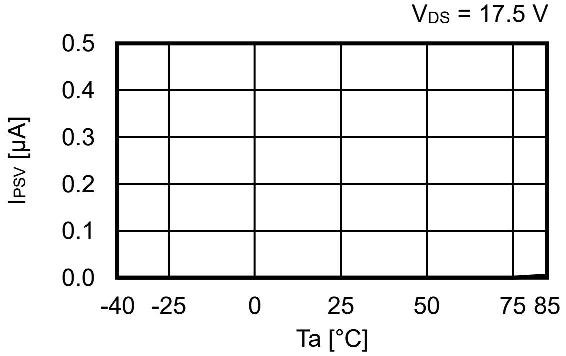
1. 4 I_{PDN} vs. Ta



1. 5 I_{PSV} vs. V_{DS}

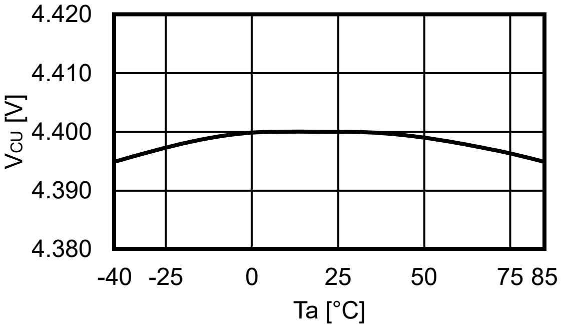


1. 6 I_{PSV} vs. Ta

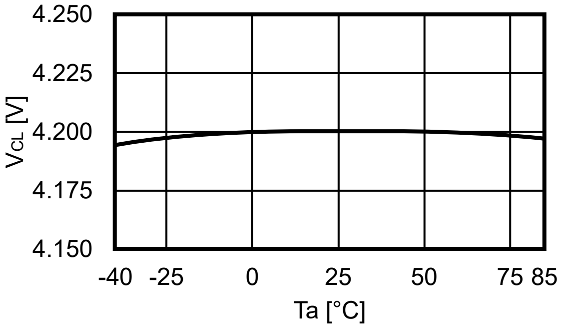


2. Detection voltage, release voltage

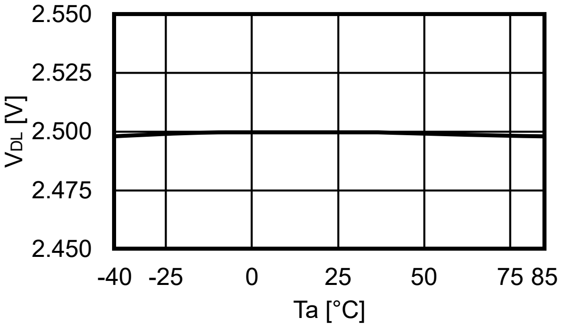
2. 1 V_{CU} vs. Ta



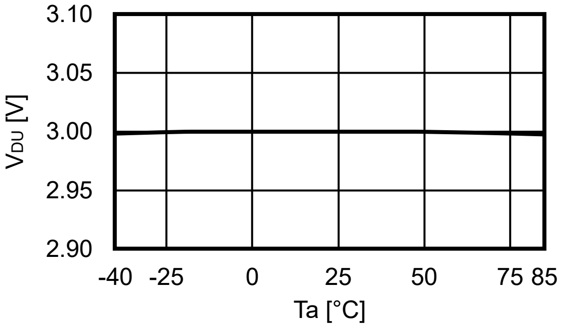
2. 2 V_{CL} vs. Ta



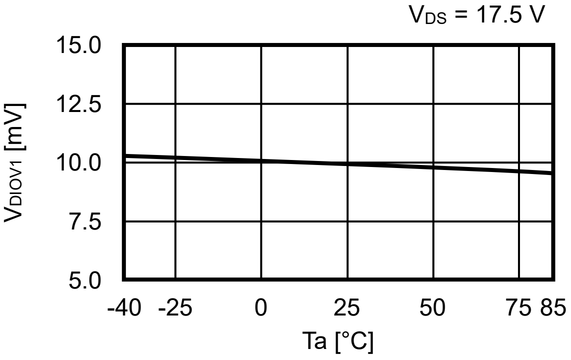
2. 3 V_{DL} vs. Ta



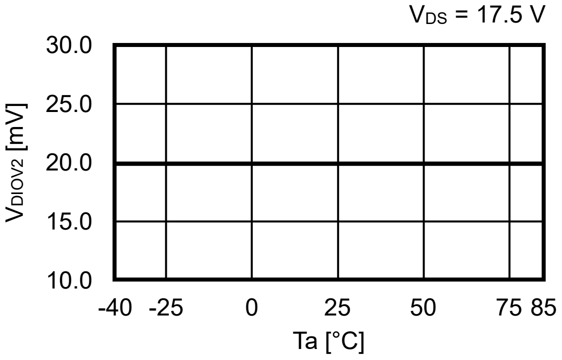
2. 4 V_{DU} vs. Ta



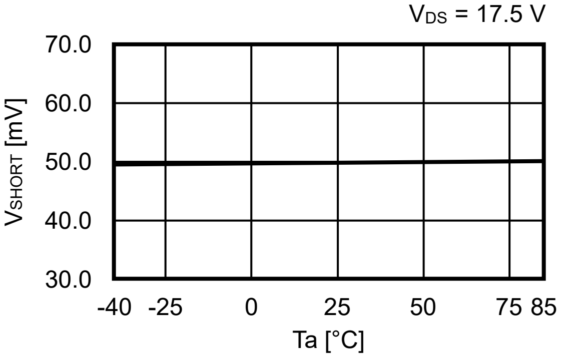
2. 5 V_{DIOV1} vs. Ta



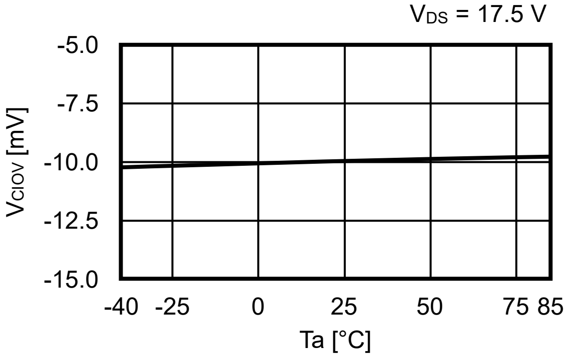
2. 6 V_{DIOV2} vs. Ta



2. 7 V_{SHORT} vs. Ta

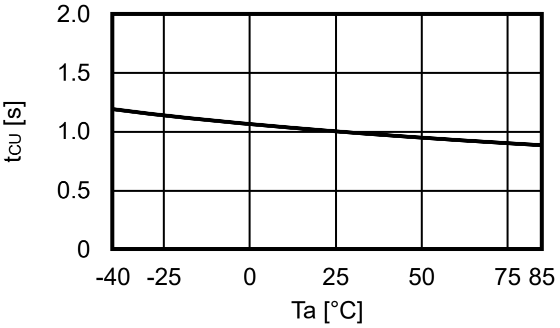


2. 8 V_{CIOV} vs. Ta

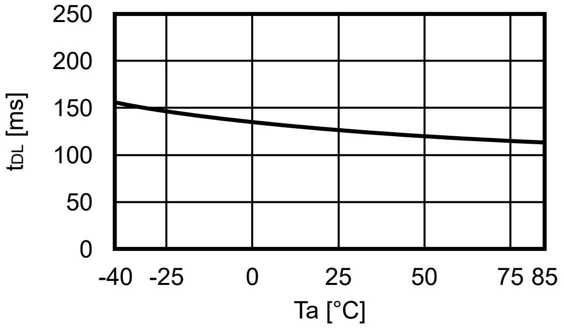


3. Delay time function

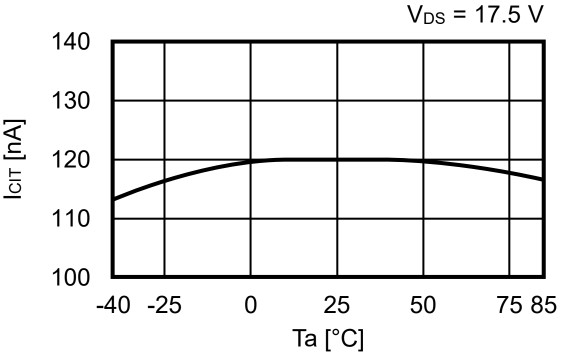
3. 1 t_{CU} vs. Ta



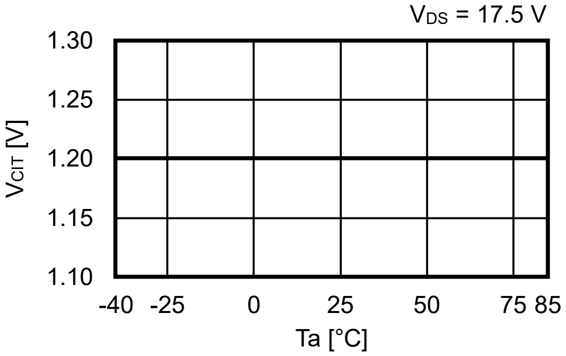
3. 2 t_{DL} vs. Ta



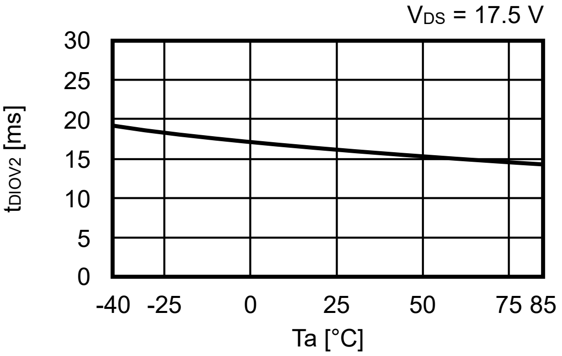
3. 3 I_{CIT} vs. Ta



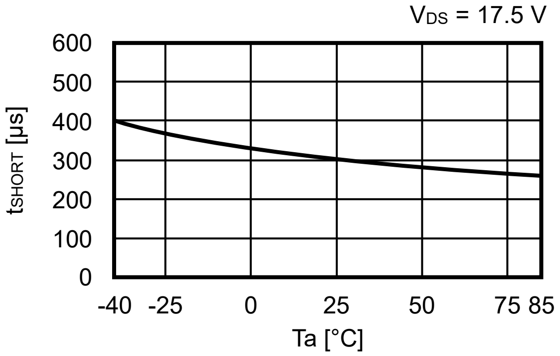
3. 4 V_{CIT} vs. Ta



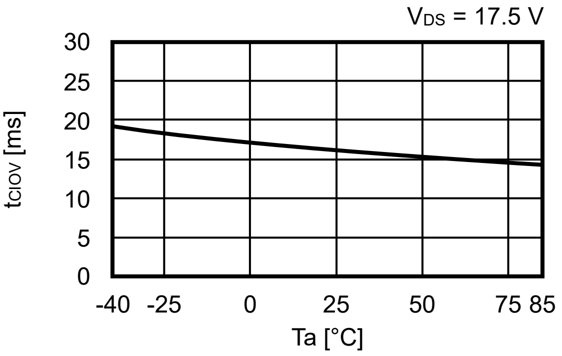
3. 5 t_{DIOV2} vs. Ta



3. 6 t_{SHORT} vs. Ta

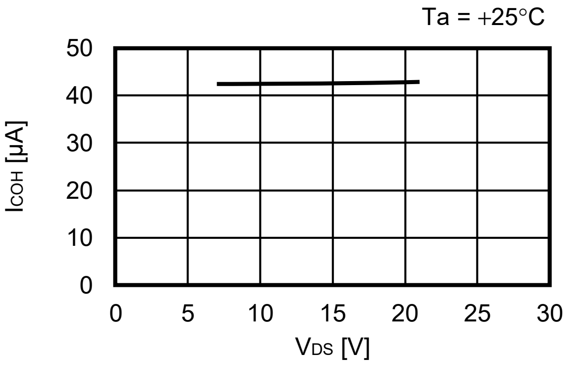


3. 7 t_{CIOV} vs. Ta

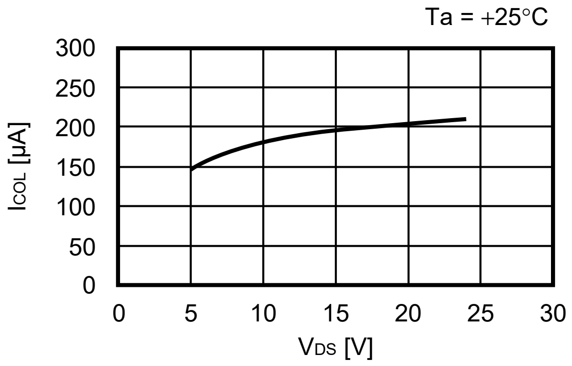


4. Output pin

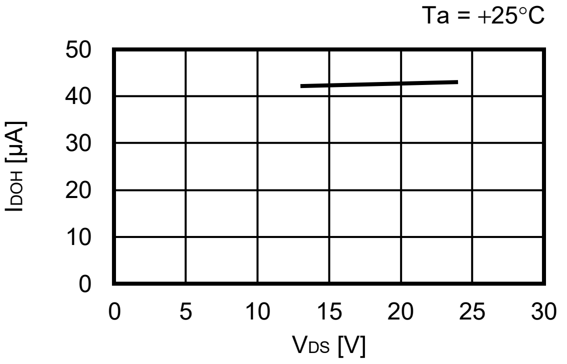
4. 1 I_{COH} vs. V_{DS}



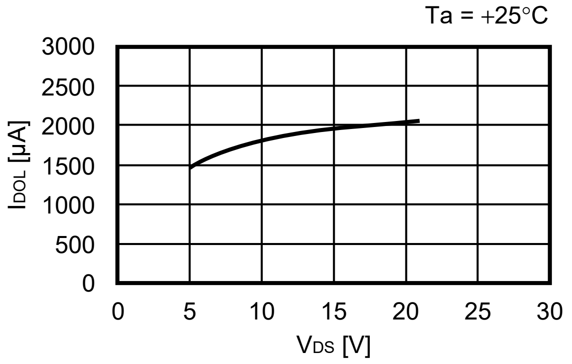
4. 2 I_{COL} vs. V_{DS}



4. 3 I_{DOH} vs. V_{DS}

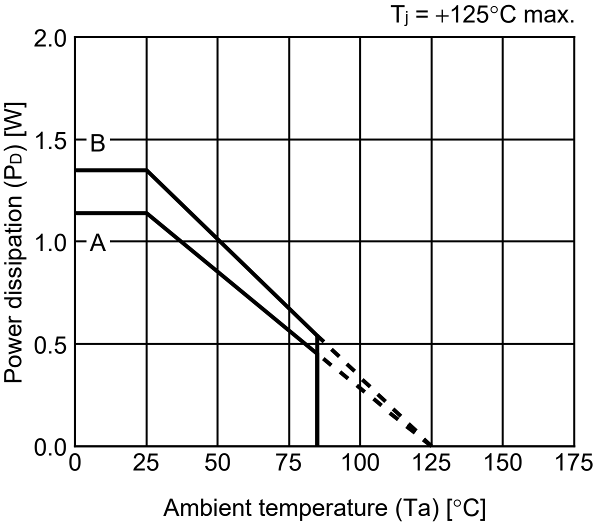


4. 4 I_{DOL} vs. V_{DS}



■ Power Dissipation

16-Pin TSSOP

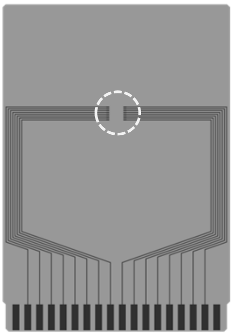


Board	Power Dissipation (P_D)
A	1.14 W
B	1.35 W
C	–
D	–
E	–

16-Pin TSSOP Test Board

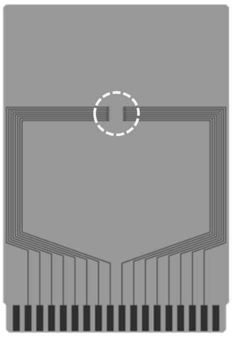
◌ IC Mount Area

(1) Board A

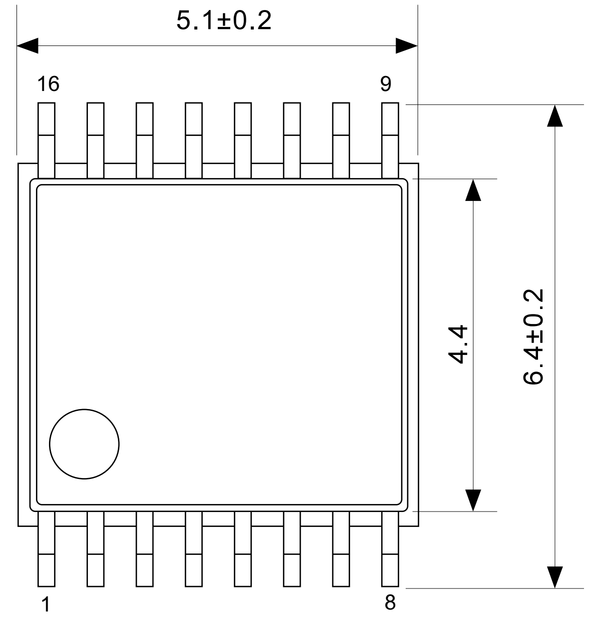


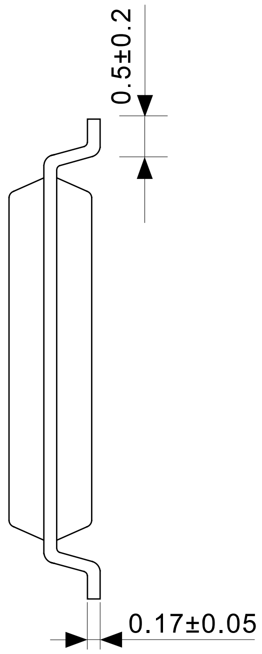
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

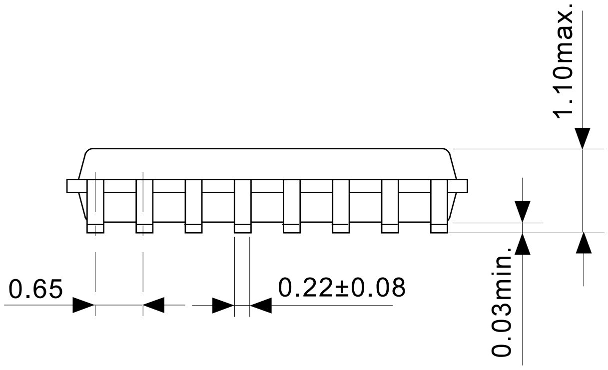
(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-







No. FT016-A-P-SD-1.2

TITLE	TSSOP16-A-PKG Dimensions
No.	FT016-A-P-SD-1.2
ANGLE	
UNIT	mm

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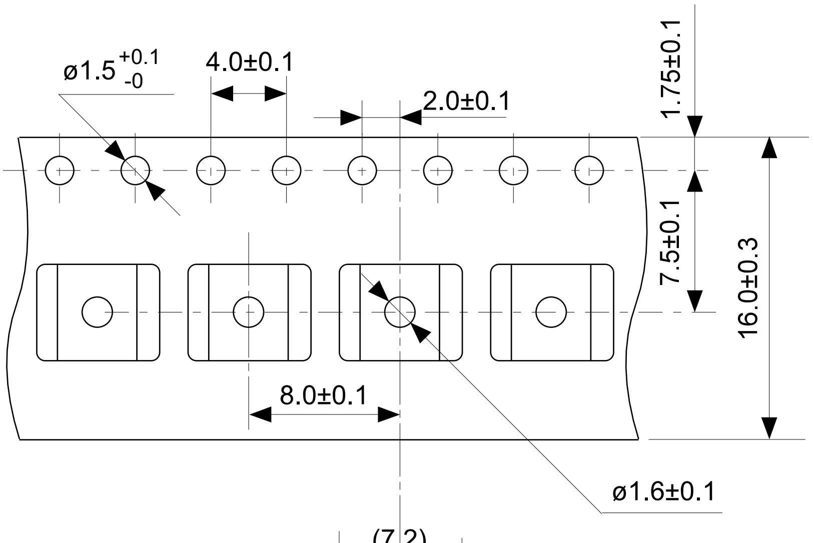

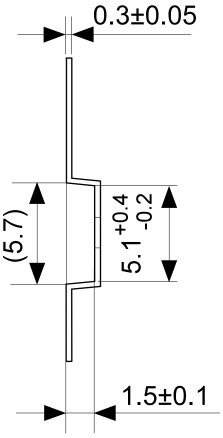

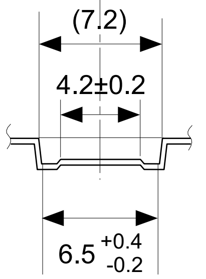

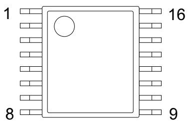

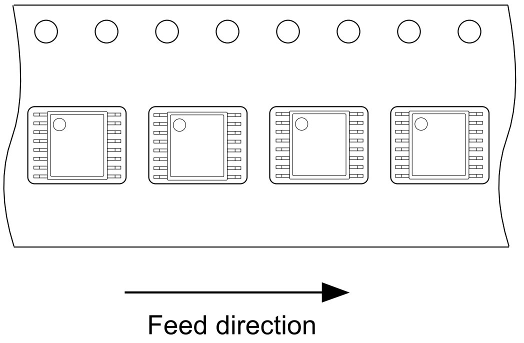

No. FT016-A-C-SD-1.1

TITLE	TSSOP16-A-Carrier Tape
No.	FT016-A-C-SD-1.1
ANGLE	
UNIT	mm

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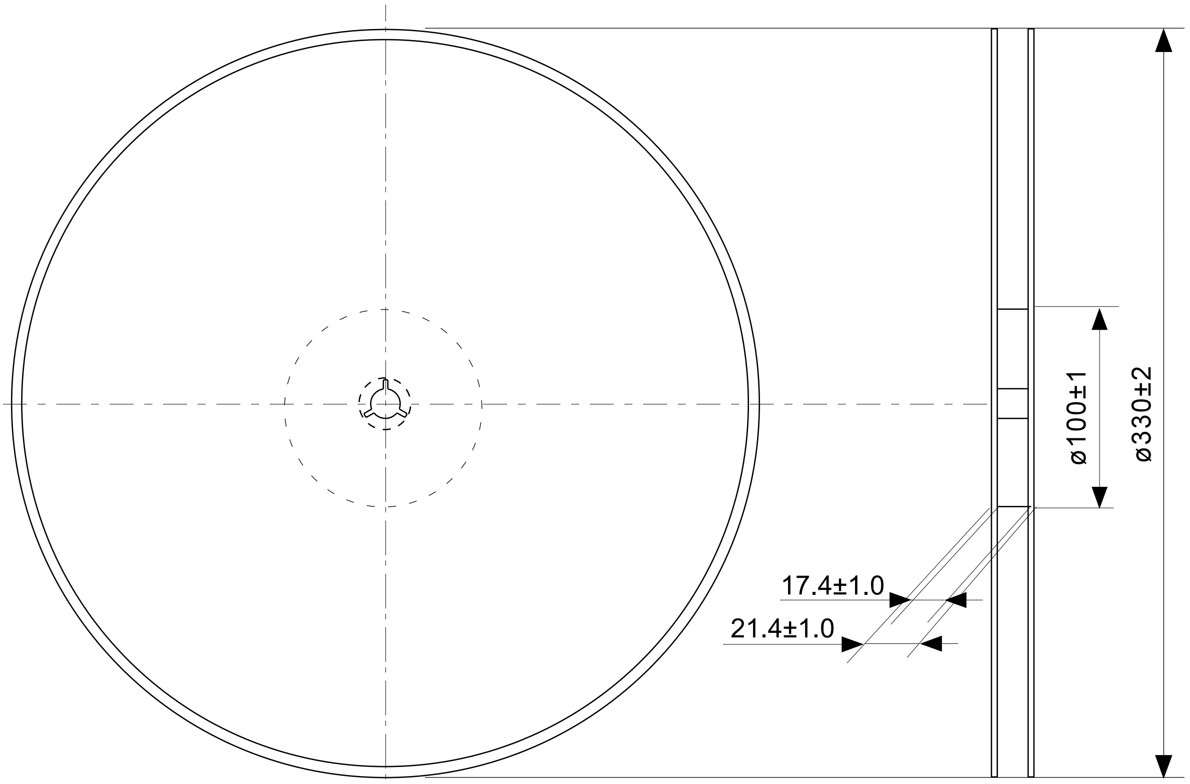
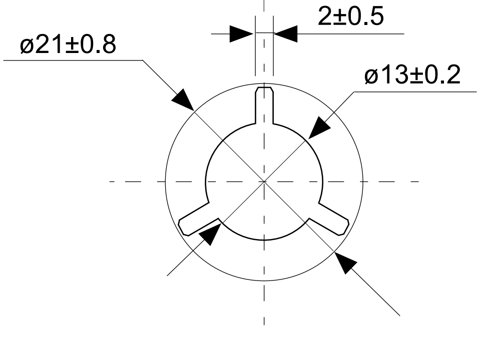


Enlarged drawing in the central part



No. FT016-A-R-S1-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-S1-2.0		
ANGLE		QTY.	4,000
UNIT	mm		

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2.4-2019.07

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