

The ABLIC Inc. HDL6M05584 is an octal, 3-level RTZ, high-voltage, high-speed ultrasound pulser. The HDL6M05584 comprises logic interfaces, level translators, MOSFET gate drive buffers with floating voltage regulators, high-voltage, high-current MOSFETs, and active T/R switches.

Functions

- Octal 3-level pulser with active T/R switch with 2-input per channel

Features

- 0 to $\pm 100V$ output voltage
- $\pm 2A$ source and sink peak current for pulsing (V_{PP}/V_{NN})
- $\pm 1A$ source and sink peak current for active ground clamp
- 250Ω ($\pm 0.1A$) active ground clamp without blocking diode for anti-leakage (Analog SW type)
- Embedded floating voltage regulators
- Symmetrical positive and negative pulse waveforms for low 2nd order harmonic distortion
- Up to 200MHz LVDS/LVCMOS clock (transparent mode available)
- 15Ω active T/R switch with 2-bit turn-on timing control
- 20MHz output frequency @ $\pm 60V$ output, 220pF load
- 1.8V to 5V CMOS logic interface
- Noise-cut diodes at each high-voltage output
- Embedded high-voltage clamp diodes
- 4-mode output current control
- Automatic thermal protection with indicator
- Power-up/down reset function for free power sequencing and for fail-safe in abrupt power drop
- Latch-up free, low crosstalk between channels by SOI CMOS technology
- 64-lead 9x9mm QFN package (RoHS compliant)

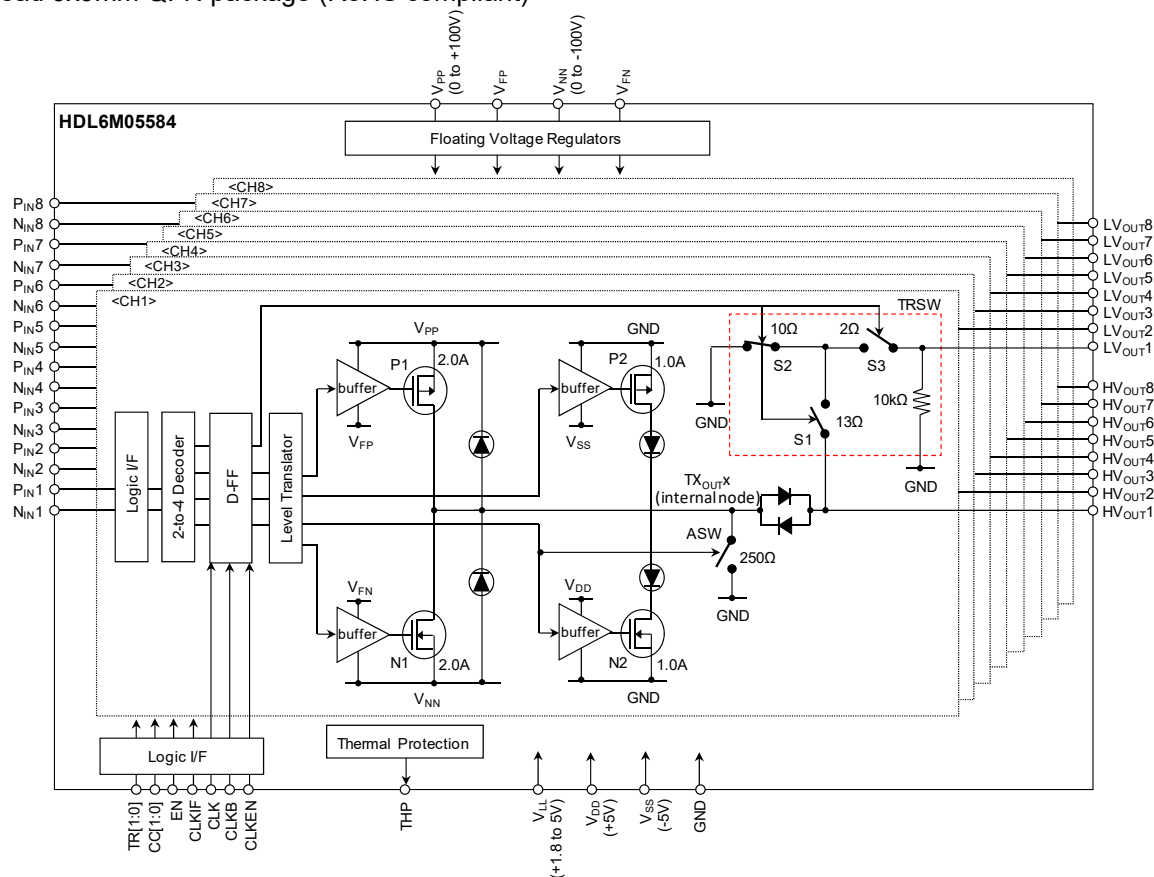


Fig.1 Block diagram

1. Absolute Maximum Ratings

T_A=25°C unless otherwise noted.

Table 1 Absolute Maximum Ratings

No.	Items	Symbol	Value	Units	Condition
1	Logic supply voltage	V _{LL}	-0.4 to +7	V	
2	Positive supply voltage	V _{DD}	-0.4 to +7	V	
3	Negative supply voltage	V _{SS}	-7 to +0.4	V	
4	Positive high-voltage supplies	V _{PP}	-0.5 to +105	V	
5	Negative high-voltage supplies	V _{NN}	-105 to +0.5	V	
6	High-voltage outputs (x=1~8)	HV _{OUTX}	-105 to +105	V	
7	Low-voltage outputs (x=1~8)	LV _{OUTX}	-1 to +1	V	
8	THP (Thermal Protection) output	THP	-0.4 to +7	V	
9	All Logic input voltages (x=1~8)	P _{INX} , N _{INX} , EN, CLKEN, CLK, CLKB, CLKIF, CC[1:0], TR[1:0]	-0.4 to +7	V	
10	Operating junction temperature	T _{Jop}	-20 to +150	°C	
11	Operating free-air Temperature	T _A	0 to +75	°C	
12	Storage temperature	T _{STG}	-55 to +150	°C	
13	Maximum power dissipation	P _{Dmax}	4	W	

NOTE: Stresses beyond the absolute maximum ratings may cause permanent damage to the product.

2. Operating Supply Voltages, Logic Inputs, and Power sequencing

2.1 Operating Supply Voltages

Table 2 Operating Supply Voltages

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	Logic supply voltage	V _{LL}	2.4	2.5 to 3.3	3.6	V	Clock mode
			1.7	1.8 to 5	V _{DD}	V	Transparent mode
2	Positive supply voltage	V _{DD}	4.75	5	5.25	V	
3	Negative supply voltage	V _{SS}	-5.25	-5	-4.75	V	
4	Positive high-voltage supplies	V _{PP}	0	-	100	V	
5	Negative high-voltage supplies	V _{NN}	-100	-	0	V	
6	IC substrate voltage *	V _{SUB}	-	0	-	V	
7	V _{PP} , V _{NN} slew rate	SR _{MAX}	-	-	25	V/ms	

NOTE: * The package exposed pad internally connected to the chip substrate must be soldered to the ground.

2.2 Logic Inputs

Clock (CLK) mode synchronizes data inputs P_{INX}, N_{INX} (x=1~8) with a differential LVDS/CMOS clock. Transparent (TP) mode without using clock is also available.

CLK mode:

Set CLKEN=0. P_{INX} and N_{INX} are decoded, clocked, level-translated, then sent to high-voltage output stage.

Differential clock input has two modes as shown below.

- LVDS CLK mode: set CLKIF=0. Connect 100Ω between CLK and CLKB. See Table 3 and 4 for the logic inputs, CLK, and CLKB.
- CMOS CLK mode: set CLKIF=1. See Table 3 for all the logic inputs.

TP mode:

Set CLKEN=CLKIF=1, CLK=CLKB=0. P_{INX} and N_{INX} are decoded, level-translated, then sent to high-voltage output stage. See Table 3 for all the logic inputs.

Table 3 Logic Inputs

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level logic input voltage	V _{IH}	0.8V _{LL}	-	V _{LL}	V	
2	Low-level logic input voltage	V _{IL}	0	-	0.2V _{LL}	V	
3	Logic input capacitance	C _{IN}	-	3	-	pF	
4	Logic input high current *1	I _{IH}	-10	-	10	μA	
5	Logic input low current *2	I _{IL}	-10	-	10	μA	
6	Input rise/fall time	t _r , t _f	-	-	800	ps	CLK≥100MHz CMOS CLK mode
			-	-	2.0	ns	CLK<100MHz 10~90% CLK, CLKB, P _{INX} , N _{INX}
7	Input clock frequency	f _{CLK}	-	-	200	MHz	CMOS CLK mode, CLK, CLKB,
8	Duty cycle	D _{CLK}	40	50	60	%	f _{CLK} =1/T, D _{CLK} =t/T, See Fig.3
9	Data Setup time	t _{SU}	1.4	-	-	ns	CLK mode, P _{INX} , N _{INX} to CLK/CLKB
10	Data Hold time	t _{HLD}	1.4	-	-	ns	See Fig.3

NOTE:

*1) TR[1:0] have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-down resistor.

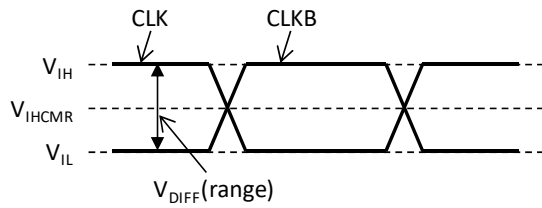
*2) EN, CC[1:0], CLKEN, and CLKIF have 50μA leakage at V_{LL}=2.5V due to 50kΩ internal pull-up resistor.

Table 4 LVDS Clock Inputs (CLK, CLKB)

No	Items	Symbol	Min	Typ	Max	Units	Condition
1	High-level input voltage	V _{IH}	1.265	-	-	V	V _{IHCMR} (Typ)+V _{DIFF} (Min)/2
2	Low-level input voltage	V _{IL}	-	-	1.135	V	V _{IHCMR} (Typ)-V _{DIFF} (Min)/2
3	Differential input voltage range	V _{DIFF} (range)	0.13	0.35	0.49	±V	same as CLK,CLKB voltage swing See Fig.2
4	Differential input voltage peak to peak swing	V _{DIFF} (p-p)	0.26	0.7	0.98	V _{pp}	CLK-CLKB differential peak-to-peak voltage swing, See Fig.2
5	Input voltage common mode range	V _{IHCMR}	0.84	1.2	1.56	V	
6	Differential input impedance	R _{IN}	85	100	115	Ω	
7	High-level input current	I _{IH}	-	-	5.8	mA	
8	Low-level input current	I _{IL}	-	-	5.8	mA	
9	Input rise/fall time	t _r , t _f	-	-	600	ps	20% to 80% of V _{DIFF}
10	Input clock frequency	f _{CLK}	-	-	200	MHz	LVDS CLK mode, CLK, CLKB,
11	Duty cycle	D _{CLK}	40	50	60	%	f _{CLK} =1/T, D _{CLK} =t/T, See Fig.3

NOTE: Please refer to table 3 for the logic inputs other than CLK, CLKB in LVDS CLK mode.

Differential input voltage range ($V_{\text{DIFF}}(\text{range})$)



Differential input voltage peak to peak swing ($V_{\text{DIFF}}(\text{p-p})$)

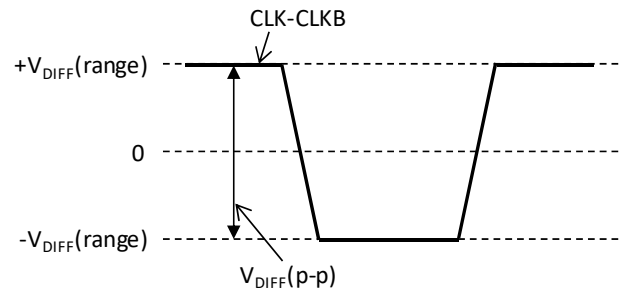
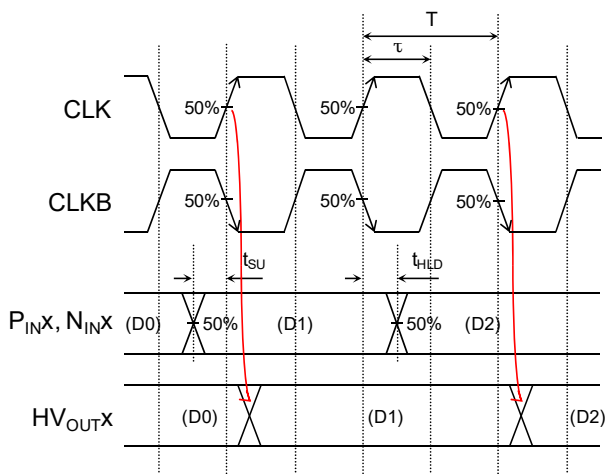


Fig.2 LVDS clock inputs

LVDS/CMOS CLK mode (CLKEN=0)



TP mode (CLKEN=1)

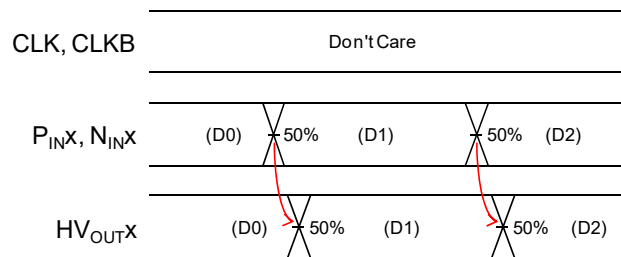


Fig.3 Setup/Hold Time

2.3 Power Supply Sequencing

Embedded low-voltage (LV) power-up/down reset function provides free power supply sequencing.

It also provides fail-safe system in abrupt LV power supply drop.

When any one of LV power supplies is turned off during operation, all internal circuits will be immediately reset, and both inputs and outputs will be disabled.

Once all LV power supplies are restored, both inputs and outputs will be enabled.

3. Typical Application Circuit

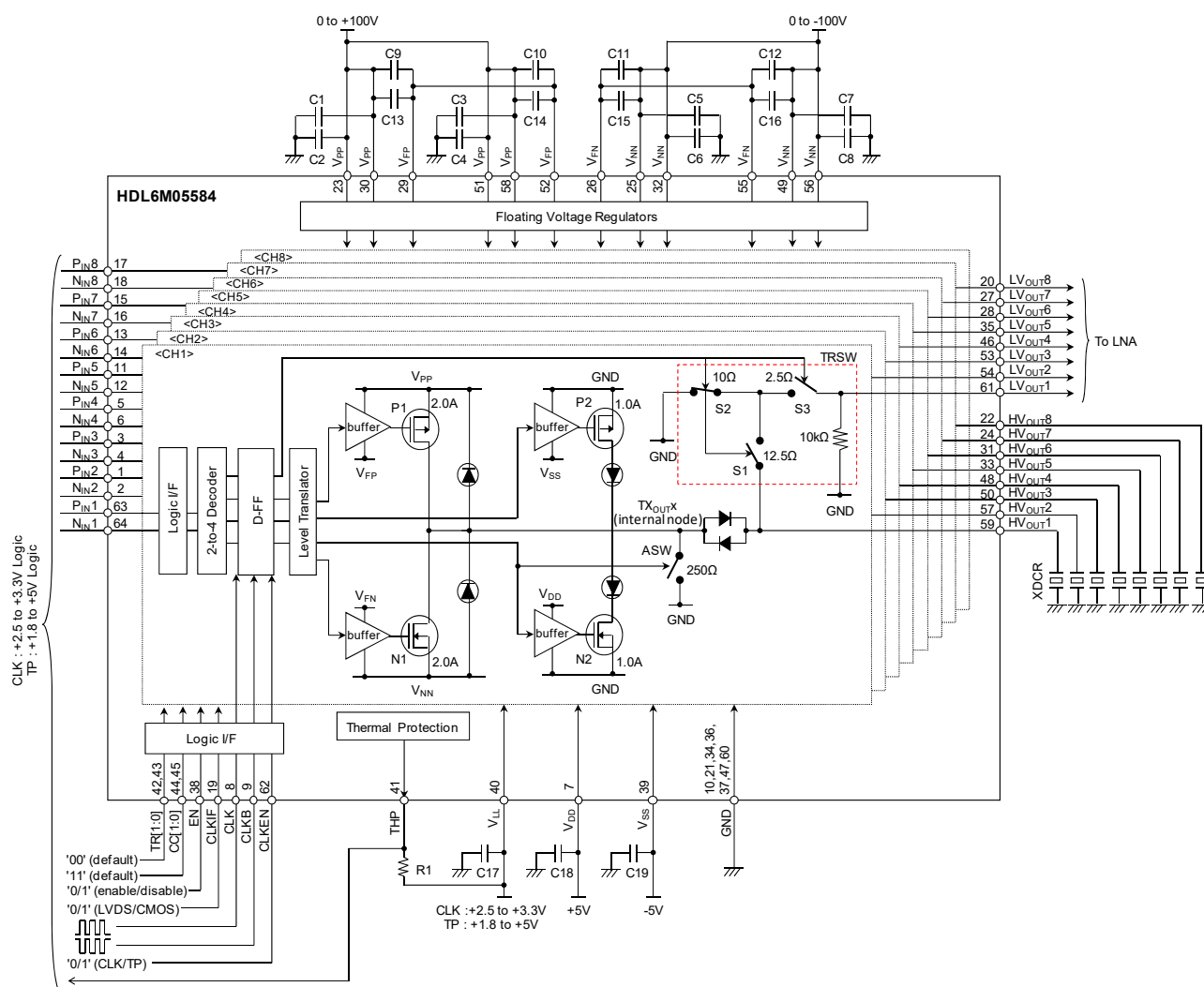


Fig.4 Typical Application Circuit

Note:

1. High-voltage power supply pins, V_{PP}/V_{NN} , can draw fast transient currents up to $\pm 2.0\text{A}$. Therefore, ceramic capacitors of $\geq 200\text{V}$ $0.1\mu\text{F}$ to $1\mu\text{F}$ (C1~8) should be connected as close to the pins as possible for bypassing purpose.
2. Ceramic capacitors of $\geq 16\text{V}$ $10\mu\text{F}$ (C9~12), $\geq 16\text{V}$ 100nF (C13~16), and $\geq 16\text{V}$ $0.1\mu\text{F}$ to $1\mu\text{F}$ (C17~19) should also be connected between high-voltage power supply and corresponding floating voltage pins V_{FP}/V_{FN} , and low-voltage power supply pins for bypassing purpose. Connect those as close to the pins as possible.
3. It is also important to minimize the trace length and to have enough trace width of those high voltage and floating voltage lines.
4. The thermal tab on the bottom of the package must be soldered to the GND.
5. Please refer to Mode Control Tables for detailed CC[1:0] and TR[1:0] setting.

4. Electrical Characteristics

4.1 Operating Supply Currents

Table 5 Operating Supply Currents

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, $CLK=CLKB=100MHz/0(CLKEN=0/1)$, $TR[1:0]='00'$,
 HV_{OUT} load= $220pF//200\Omega$, LV_{OUT} load= $47pF//200\Omega$, unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
1	V_{LL} current	TP	I_{LLQD}	-	0.03	-	mA	Quiescent current-1 EN=1(Disable) $P_{INX}=N_{INX}=0$ Current mode 3 (CC[1:0]='11') $V_{PP}/V_{NN}=+/-100V$
		LVDS CLK		-	0.08	-	mA	
		CMOS CLK		-	0.13	-	mA	
2	V_{DD} current	TP	I_{DDQD}	-	2.8	-	mA	
		LVDS CLK		-	2.8	-	mA	
		CMOS CLK		-	2.8	-	mA	
3	V_{SS} current		I_{SSQD}	-	0.63	-	mA	
4	V_{PP} current		I_{PPQD}	-	0.03	-	mA	
5	V_{NN} current		I_{NNQD}	-	0.04	-	mA	
6	V_{LL} current	TP	I_{LLQE}	-	0.08	-	mA	Quiescent current-2 EN=0(Enable) $P_{INX}=N_{INX}=0$ Current mode 3 (CC[1:0]='11') $V_{PP}/V_{NN}=+/-100V$
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
7	V_{DD} current	TP	I_{DDQE}	-	10	-	mA	
		LVDS CLK		-	30	-	mA	
		CMOS CLK		-	28	-	mA	
8	V_{SS} current		I_{SSQE}	-	9.3	-	mA	
9	V_{PP} current		I_{PPQE}	-	0.15	-	mA	
10	V_{NN} current		I_{NNQE}	-	0.15	-	mA	
11	V_{LL} current	TP	I_{LLPW}	-	0.08	-	mA	PW operating current EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level 2-cycle $f=5MHz$, $PRT=200\mu s$ $V_{PP}/V_{NN}=+/-60V$
		LVDS CLK		-	0.18	-	mA	
		CMOS CLK		-	0.13	-	mA	
12	V_{DD} current	TP	I_{DDPW}	-	10	-	mA	
		LVDS CLK		-	34	-	mA	
		CMOS CLK		-	32	-	mA	
13	V_{SS} current		I_{SSPW}	-	9.3	-	mA	
14	V_{PP} current		I_{PPPW}	-	4.2	-	mA	
15	V_{NN} current		I_{NNPW}	-	4.9	-	mA	

Table 5 Operating Supply Currents (continued)

No.	Items		Symbol	Spec			Units	Conditions
				Min	Typ	Max		
16	V _{LL} current	TP	I _{LLCW3}	-	0.43	-	mA	CW operating current-1 EN=0 Current mode 3 (CC[1:0]='11') 8-channel active Bipolar 3-level Continuous f=5MHz V _{PP} /V _{NN} =+/-5V
		LVDS CLK		-	0.53	-	mA	
		CMOS CLK		-	0.48	-	mA	
17	V _{DD} current	TP	I _{DDCW3}	-	42	-	mA	
		LVDS CLK		-	64	-	mA	
		CMOS CLK		-	61	-	mA	
18	V _{SS} current		I _{SSCW3}	-	27	-	mA	
19	V _{PP} current		I _{PPCW3}	-	217	-	mA	
20	V _{NN} current		I _{NNCW3}	-	220	-	mA	
21	V _{LL} current	TP	I _{LLCW2}	-	0.48	-	mA	CW operating current-2 EN=0 Current mode 2 (CC[1:0]='10') 8-channel active Bipolar 3-level Continuous f=5MHz V _{PP} /V _{NN} =+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
22	V _{DD} current	TP	I _{DDCW2}	-	38	-	mA	
		LVDS CLK		-	60	-	mA	
		CMOS CLK		-	57	-	mA	
23	V _{SS} current		I _{SSCW2}	-	23	-	mA	
24	V _{PP} current		I _{PPCW2}	-	208	-	mA	
25	V _{NN} current		I _{NNCW2}	-	211	-	mA	
26	V _{LL} current	TP	I _{LLCW1}	-	0.48	-	mA	CW operating current-3 EN=0 Current mode 1 (CC[1:0]='01') 8-channel active Bipolar 3-level Continuous f=5MHz V _{PP} /V _{NN} =+/-5V
		LVDS CLK		-	0.58	-	mA	
		CMOS CLK		-	0.53	-	mA	
27	V _{DD} current	TP	I _{DDCW1}	-	34	-	mA	
		LVDS CLK		-	56	-	mA	
		CMOS CLK		-	53	-	mA	
28	V _{SS} current		I _{SSCW1}	-	18	-	mA	
29	V _{PP} current		I _{PPCW1}	-	195	-	mA	
30	V _{NN} current		I _{NNCW1}	-	198	-	mA	
31	V _{LL} current	TP	I _{LLCW0}	-	0.53	-	mA	CW operating current-4 EN=0 Current mode 0 (CC[1:0]='00') 8-channel active Bipolar 3-level Continuous f=5MHz V _{PP} /V _{NN} =+/-5V
		LVDS CLK		-	0.63	-	mA	
		CMOS CLK		-	0.58	-	mA	
32	V _{DD} current	TP	I _{DDCW0}	-	28	-	mA	
		LVDS CLK		-	49	-	mA	
		CMOS CLK		-	47	-	mA	
33	V _{SS} current		I _{SSCW0}	-	13	-	mA	
34	V _{PP} current		I _{PPCW0}	-	169	-	mA	
35	V _{NN} current		I _{NNCW0}	-	173	-	mA	

4.2 Static Characteristics

Table 6 Static Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	HV _{OUTX} output voltage range	HV _{OUTX}	-100	-	+100	V	
2	HV _{OUTX} high-side peak current	I _{OH}	-	2.0	-	A	V _{PP} /V _{NN} =+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	V _{PP} /V _{NN} =+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	V _{PP} /V _{NN} =+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	V _{PP} /V _{NN} =+/-60V Current mode 0 (CC[1:0]='00')
3	HV _{OUTX} high-side GND clamp peak current	I _{OHCL}	-	1.0	-	A	V _{PP} /V _{NN} =+/-60V
4	HV _{OUTX} low-side peak current	I _{OL}	-	2.0	-	A	V _{PP} /V _{NN} =+/-60V Current mode 3 (CC[1:0]='11')
			-	1.5	-	A	V _{PP} /V _{NN} =+/-60V Current mode 2 (CC[1:0]='10')
			-	1.0	-	A	V _{PP} /V _{NN} =+/-60V Current mode 1 (CC[1:0]='01')
			-	0.5	-	A	V _{PP} /V _{NN} =+/-60V Current mode 0 (CC[1:0]='00')
5	HV _{OUTX} low-side GND clamp peak current	I _{OLCL}	-	1.0	-	A	V _{PP} /V _{NN} =+/-60V
6	HV _{OUTX} high-side on-resistance	R _{ONH}	-	10	-	Ω	I _{OH} =100mA Current mode 3 (CC[1:0]='11')
			-	13	-	Ω	I _{OH} =100mA Current mode 2 (CC[1:0]='10')
			-	18	-	Ω	I _{OH} =100mA Current mode 1 (CC[1:0]='01')
			-	31	-	Ω	I _{OH} =100mA Current mode 0 (CC[1:0]='00')
7	HV _{OUTX} high-side GND clamp on-resistance	R _{ONHCL}	-	21	-	Ω	I _{OHCL} =100mA
8	HV _{OUTX} low-side on-resistance	R _{ONL}	-	9	-	Ω	I _{OL} =100mA Current mode 3 (CC[1:0]='11')
			-	12	-	Ω	I _{OL} =100mA Current mode 2 (CC[1:0]='10')
			-	17	-	Ω	I _{OL} =100mA Current mode 1 (CC[1:0]='01')
			-	30	-	Ω	I _{OL} =100mA Current mode 0 (CC[1:0]='00')
9	HV _{OUTX} low-side GND clamp on-resistance	R _{ONLCL}	-	20	-	Ω	I _{OLCL} =100mA
10	HV _{OUTX} off-capacitance	CH _{VOFF}	-	20	-	pF	TX _{OUTX} =GND, TRSW=off

4.3 Dynamic Characteristics

Table 7 Dynamic Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP}/V_{NN}=+/-60V$, $T_A=25^{\circ}C$, $TR[1:0]='00'$, $CC[1:0]='11'$,

$CLK=CLKB=100MHz/0(CLKEN=0/1)$, HV_{OUT} load=220pF//200 Ω , LV_{OUT} load=47pF//200 Ω , unless otherwise specified.

No.	Items		Symbol	Spec			Units	Conditions			
				Min	Typ	Max					
1	Output frequency		f _{OUT}	-	20	-	MHz				
2	Output rise propagation delay	TP mode	t _{dr}	-	31	-	ns	See Fig.5			
		CLK mode		-	37	-	ns				
3	Output fall propagation delay	TP mode	t _{df}	-	31	-	ns				
		CLK mode		-	37	-	ns				
4	Output rise propagation delay clamp	TP mode	t _{drCL}	-	31	-	ns				
		CLK mode		-	37	-	ns				
5	Output fall propagation delay clamp	TP mode	t _{dfCL}	-	31	-	ns				
		CLK mode		-	37	-	ns				
6	Propagation delay matching		Δt _d	-	±1	±3	ns				
7	Output rise time		t _r	-	16	-	ns	CC[1:0]='11'	See Fig.5		
				-	24	-	ns	CC[1:0]='10'			
				-	34	-	ns	CC[1:0]='01'			
				-	44	-	ns	CC[1:0]='00'			
			t _{rCL}	-	25	-	ns				
8	Output fall time		t _f	-	16	-	ns	CC[1:0]='11'			
				-	24	-	ns	CC[1:0]='10'			
				-	34	-	ns	CC[1:0]='01'			
				-	44	-	ns	CC[1:0]='00'			
			t _{fCL}	-	25	-	ns				
9	2 nd harmonic distortion		HD2	-	-40	-	dBc	Bipolar, 2-cyc, f _{OUT} =5MHz			
10	Pulse cancellation		HDPC	-	-40	-	dBc	See Fig.6			
			HDPC2	-	-40	-	dBc				
11	RMS output jitter		t _j	-	10	-	ps	Bipolar CW, f _{OUT} =5MHz V _{PP} /V _{NN} =+/-5V			
12	Crosstalk between channels		X _{TLK}	-	-70	-	dB	f _{OUT} =5MHz, 10V _{P-P} , HV _{OUT} load=50Ω			
13	Output enable time	TP	t _{EN}	-	31	-	ns	See Fig.7			
		LVDS CLK		-	120	-	ns				
		CMOS CLK		-	140	-	ns				
14	Output disable time		t _{DS}	-	37	-	ns				
15	Clock mode enable time		t _{CLKEN}	-	37	-	ns				
16	Clock mode disable time		t _{CLKDS}	-	37	-	ns				

4.4 Integrated Peripheral Circuits Characteristics

T/R Switch

Table 8 T/R Switch Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $V_{PP1}/V_{NN1}=V_{PP2}/V_{NN2}=+/-60V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	LV _{OUTX} output voltage range	LV _{OUTX}	-0.85	-	+0.85	V	
2	TRSW on-resistance	R _{ONTR}	-	15	-	Ω	HV _{OUTX} =100mV, LV _{OUTX} =0V
3	TRSW on-capacitance	C _{ONTR}	-	12	-	pF	LV _{OUTX} =0V
4	TRSW off-resistance on HV _{OUTX}	R _{OFFTRHV}	1	-	-	MΩ	
5	TRSW off-resistance on LV _{OUTX}	R _{OFFTRLV}	8	10	12	kΩ	
6	Spike voltage on HV _{OUTX} and LV _{OUTX}	V _{TRN}	-	-	50	mV _{PP}	50pF//200Ω load on HV _{OUTX} 20pF//200Ω load on LV _{OUTX}
7	TRSW turn-on time	t _{dTRON}	-	300	-	ns	Logic input-to-ready for Rx signal See Fig.8
			-	400	-	ns	
			-	500	-	ns	
			-	600	-	ns	
8	TRSW turn-off time	t _{dTROFF}	-	50	100	ns	See Fig.8
9	Tx setup time	t _{TXSU}	100	-	-	ns	P _{INX} =N _{INX} =0 (GND) for at least 100ns before Tx burst. See Fig.8

Analog Switch

Table 9 Analog Switch Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	ASW on-resistance	R _{ONASW}	-	250	-	Ω	

HV Blocking Diode

Table 10 Output HV Blocking Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FHVD}	-	1.0	-	V	I _F =100mA
			-	1.2	-	V	I _F =200mA
2	Reverse voltage	V _{RHVD}	200	-	-	V	I _R =1μA

LV Noise-cut Diode

Table 11 Output LV Noise-cut Diode Characteristics

$T_A=25^{\circ}C$

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	Forward voltage	V _{FLVD}	-	1.1	-	V	I _F =100mA
			-	1.25	-	V	I _F =200mA

Thermal Protection

Table 12 Thermal Protection Characteristics

$V_{LL}=2.5V$, $V_{DD}/V_{SS}=+/-5V$, $T_A=25^{\circ}C$, unless otherwise specified.

No.	Items	Symbol	Spec			Units	Conditions
			Min	Typ	Max		
1	THP pull-up voltage	V_{PUTHP}	-	-	5.25	V	Open drain
2	THP output current	I_{THP}	-	1.0	-	mA	-
3	THP output low voltage	V_{OLTHP}	-	-	0.5	V	THP active, $V_{LL}=2.5V$, $I_{THP}=1mA$
4	THP temperature threshold	T_{THP}	90	110	130	$^{\circ}C$	
5	THP reset hysteresis	T_{HYSTHP}	-	10	-	$^{\circ}C$	

5. Switching Time Diagram

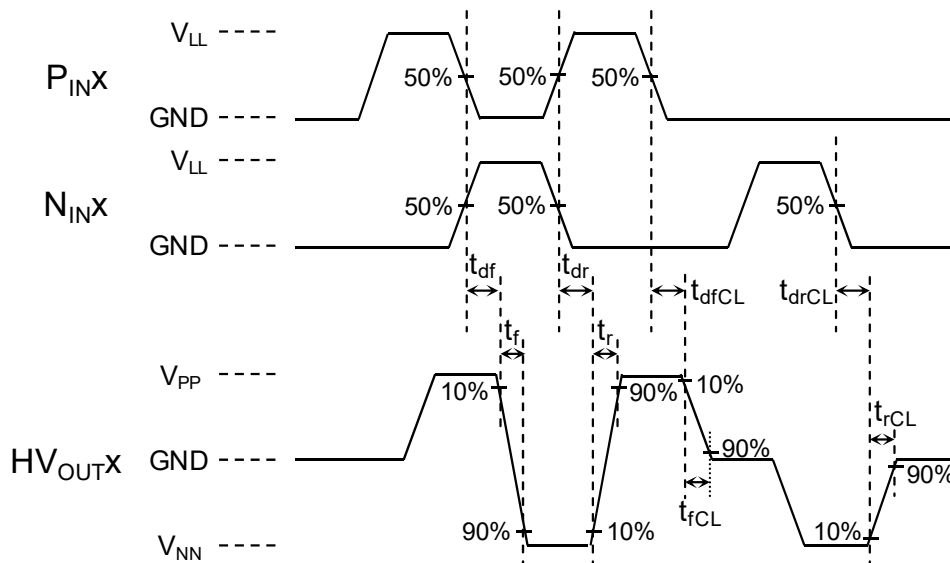
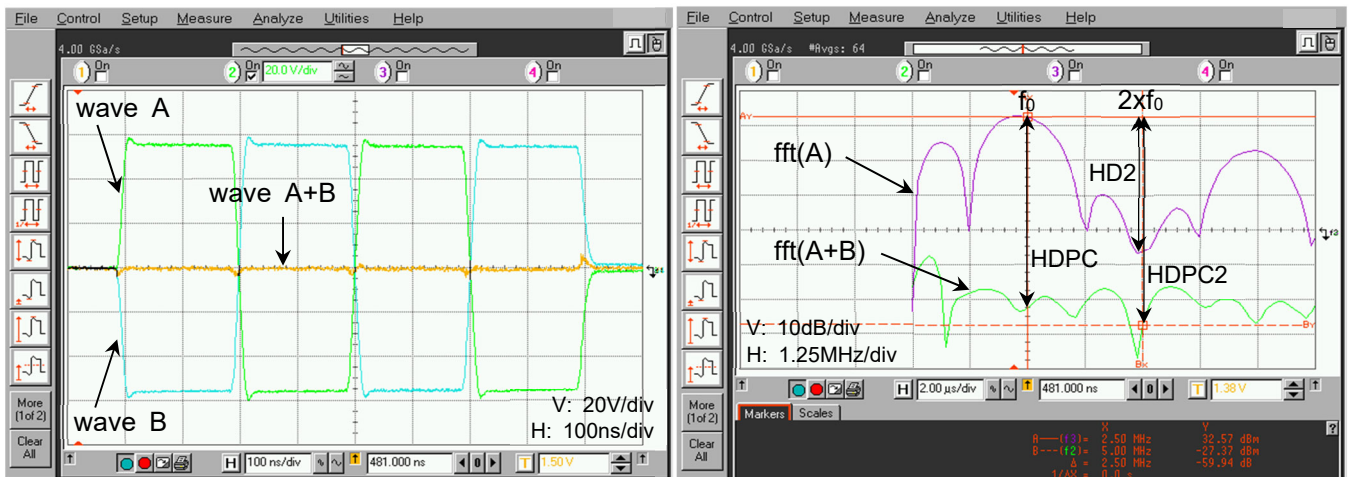


Fig.5 Propagation delay and Output rise/fall time



Example waveforms: $V_{PP}/V_{NN} = \pm 60V$, $f_0 = 2.5MHz$, 2-cycle, HV_{OUT} load = $220pF // 200\Omega$

Fig.6 2nd harmonic distortion and Pulse cancellation

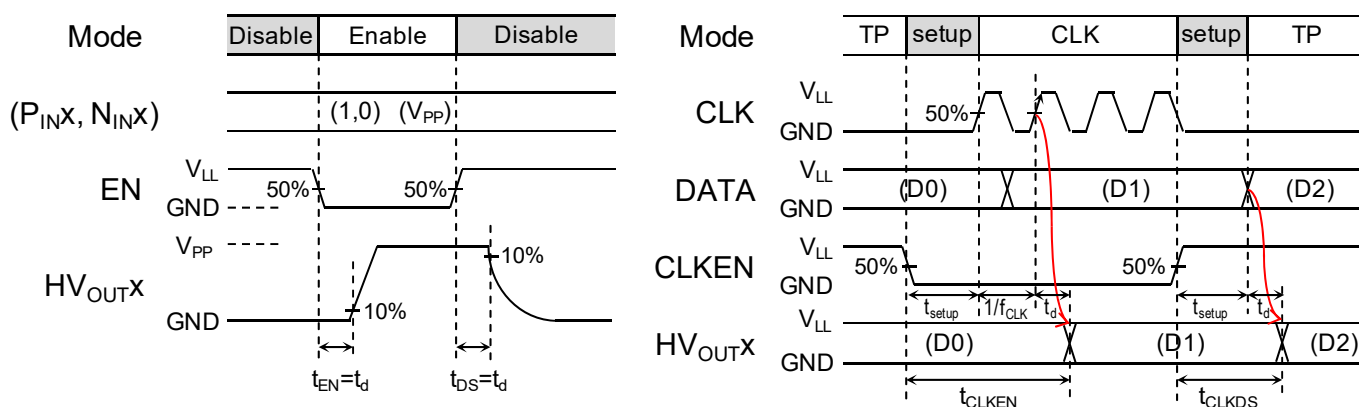


Fig.7 Output enable/disable and Clock enable/disable time

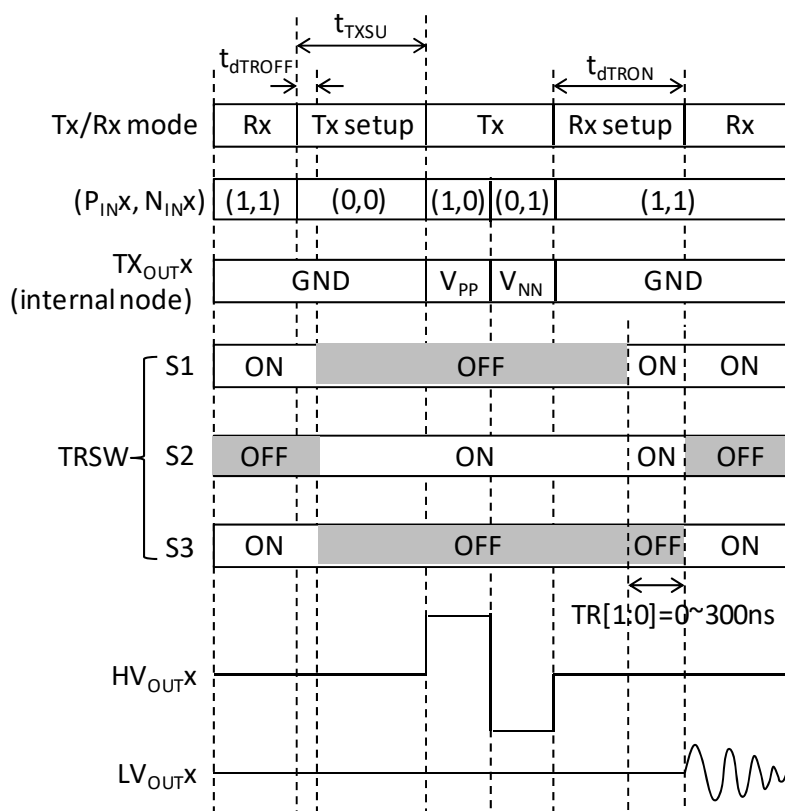


Fig.8 T/R Switch turn-on/off time

6. Truth Table and Mode Control tables

Table 13 Truth table

Logic Inputs			Internal MOSFET state								Output state	
EN	P _{INx}	N _{INx}	P1	N1	P2	N2	ASW	TRSW			TX _{OUTx}	LV _{OUTx}
			+HV	-HV	GND	GND	GND	S1	S2	S3	(internal node)	
0	0	0	OFF	OFF	ON	ON	ON	OFF	ON	OFF	GND	10k Ω
0	0	1	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	-HV	10k Ω
0	1	0	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	+HV	10k Ω
0	1	1	OFF	OFF	ON	ON	ON	ON	OFF	ON	GND	HV _{OUTx}
1	X	X	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	HiZ	10k Ω

Note: V_{PP}/ V_{NN}=+/-HV, x=1~8

Table 14 P1/N1 drive current mode

Current Mode	CC1	CC0	I _{out} [A]	
			P1	N1
0	0	0	0.5	0.5
1	0	1	1	1
2	1	0	1.5	1.5
3	1	1	2	2

Note:

Recommended mode is as follows:

- Current mode 2 or 3 for high amplitude short cycle pulse waveforms, or for driving heavy load
- Current mode 0 or 1 for low amplitude long pulse train waveforms (e.g. CW), or for driving light load

Table 15 TRSW S1-S2 turn-on overlap time control mode

TRSW Control Mode	TR1	TR0	S1-S2 ON
			overlap time [ns]
0	0	0	0 (default)
1	0	1	100
2	1	0	200
3	1	1	300

Note: Detailed switching time diagram is shown in Fig.8.

7. Pin Configuration

Table 16 Pin Configuration

Pin#	Pin Name	I/O	Function
1	P _{IN2}	I	Logic input of channel 2
2	N _{IN2}	I	Logic input of channel 2
3	P _{IN3}	I	Logic input of channel 3
4	N _{IN3}	I	Logic input of channel 3
5	P _{IN4}	I	Logic input of channel 4
6	N _{IN4}	I	Logic input of channel 4
7	V _{DD}	-	Positive low voltage power supply (+5V)
8	CLK	I	Positive clock input (up to 200MHz)
9	CLKB	I	Negative clock Input (up to 200MHz)
10	GND	-	Drive power ground (0V)
11	P _{IN5}	I	Logic input of channel 5
12	N _{IN5}	I	Logic input of channel 5
13	P _{IN6}	I	Logic input of channel 6
14	N _{IN6}	I	Logic input of channel 6
15	P _{IN7}	I	Logic input of channel 7
16	N _{IN7}	I	Logic input of channel 7
17	P _{IN8}	I	Logic input of channel 8
18	N _{IN8}	I	Logic input of channel 8
19	CLKIF	I	Control of clock interface, Hi=differential CMOS, Low=LVDS (50k Ω internal pull-up resistor)
20	LV _{OUT8}	O	Low voltage output of channel 8
21	GND	-	Drive power ground (0V)
22	HV _{OUT8}	O	High voltage output of channel 8
23	V _{PP}	-	Positive high voltage power supply (0 to +100V)
24	HV _{OUT7}	O	High voltage output of channel 7
25	V _{NN}	-	Negative high voltage power supply (0 to -100V)
26	V _{FN}	-	Built-in power supply for N-MOS (N1) gate drive
27	LV _{OUT7}	O	Low voltage output of channel 7
28	LV _{OUT6}	O	Low voltage output of channel 6
29	V _{FP}	-	Built-in power supply for P-MOS (P1) gate drive
30	V _{PP}	-	Positive high voltage power supply (0 to +100V)
31	HV _{OUT6}	O	High voltage output of channel 6
32	V _{NN}	-	Negative high voltage power supply (0 to -100V)

Table 16 Pin Configuration (cont.)

Pin#	Pin Name	I/O	Function
33	HV _{OUT5}	O	High voltage output of channel 5
34	GND	-	Drive power ground (0V)
35	LV _{OUT5}	O	Low voltage output of channel 5
36	GND	-	Drive power ground (0V)
37	GND	-	Drive power ground (0V)
38	EN	I	Control of drive output enable, Hi=off, Low=on (50k Ω internal pull-up resistor)
39	V _{SS}	-	Negative low voltage power supply (-5V)
40	V _{LL}	-	Positive voltage supply of logic input interface (1.8 to 5V)
41	THP	O	Thermal protection output flag, open N-MOS drain
42	TR0	I	Lower bit of control of T/R switch S1 and S2 turn-on overlap time (50k Ω internal pull-down resistor)
43	TR1	I	Upper bit of control of T/R switch S1 and S2 turn-on overlap time (50k Ω internal pull-down resistor)
44	CC0	I	Lower bit of control of P1/N1 drive current (50k Ω internal pull-up resistor)
45	CC1	I	Upper bit of control of P1/N1 drive current (50k Ω internal pull-up resistor)
46	LV _{OUT4}	O	Low voltage output of channel 4
47	GND	-	Drive power ground (0V)
48	HV _{OUT4}	O	High voltage output of channel 4
49	V _{NN}	-	Negative high voltage power supply (0 to -100V)
50	HV _{OUT3}	O	High voltage output of channel 3
51	V _{PP}	-	Positive high voltage power supply (0 to +100V)
52	V _{FP}	-	Built-in power supply for P-MOS (P1) gate drive
53	LV _{OUT3}	O	Low voltage output of channel 3
54	LV _{OUT2}	O	Low voltage output of channel 2
55	V _{FN}	-	Built-in power supply for N-MOS (N1) gate drive
56	V _{NN}	-	Negative high voltage power supply (0 to -100V)
57	HV _{OUT2}	O	High voltage output of channel 2
58	V _{PP}	-	Positive high voltage power supply (0 to +100V)
59	HV _{OUT1}	O	High voltage output of channel 1
60	GND	-	Drive power ground (0V)
61	LV _{OUT1}	O	Low voltage output of channel 1
62	CLKEN	I	Control of clock enable, Hi=clock disable, Low=clock enable (50k Ω internal pull-up resistor)
63	P _{IN1}	I	Logic input of channel 1
64	N _{IN1}	I	Logic input of channel 1

■ Package

Table 17 Package Drawing Codes

Package Name	Dimension	Tray	Marking	Land	Packing
QFN-64(0909)B	QN064-B-P-SD	QFN9x9-B-T-SD	QN064-B-M-S2	QN064-B-L-SD	QN064-B-K-SD

■ Storage, Mounting

1. Storage conditions

- 1.1 The storage location should be kept at 5 to 35°C and 40 to 70% relative humidity. Keeping in a dry box is recommended. Moisture-proof property is assured for 12 months from delivery date for sealed moisture-proof packing, while it is guaranteed for 7 days from unpacked date under the condition above.
- 1.2 When the storage conditions do not conform to those above or other conditions occur indicating moisture exposure, the ICs should be dried to avoid package cracks. A baking process at 125°C lasting for 24 hours results in sufficient dehumidification. The baking is not allowed more than twice, and the ICs should be mounted within 7 days after initial baking or within 10 days of total exposure after the second dehumidification.

2. Reflow soldering

The temperature rise may be different in the resin and a terminal part due to the reflow soldering. It is necessary to check the package surface temperature (resin) before setting the temperature profile.

Fig. 9 shows the resistance to soldering heat condition for package (Reflow method).

Confirm the heat resistance of the package shown below. (Based on JEDEC J-STD-020).

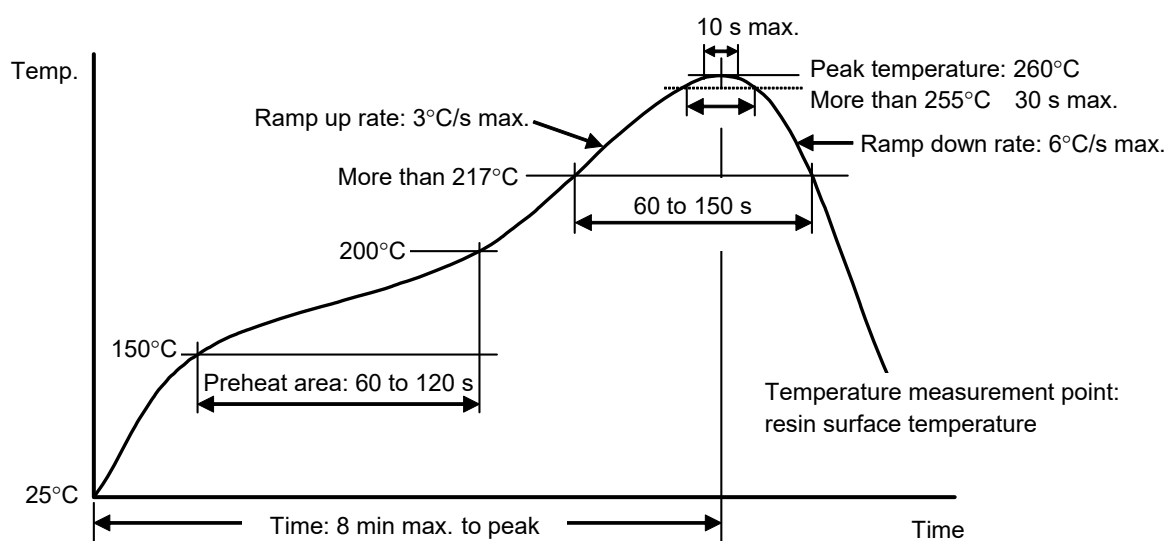


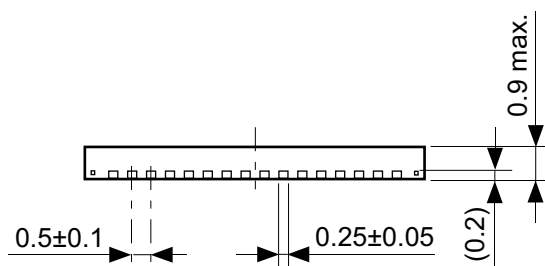
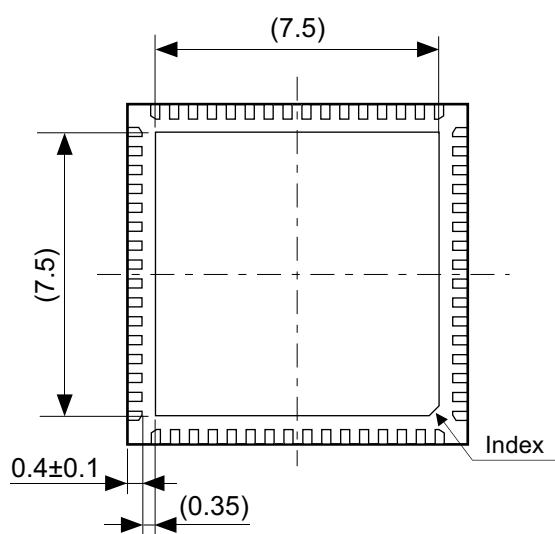
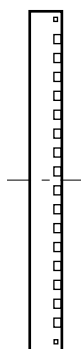
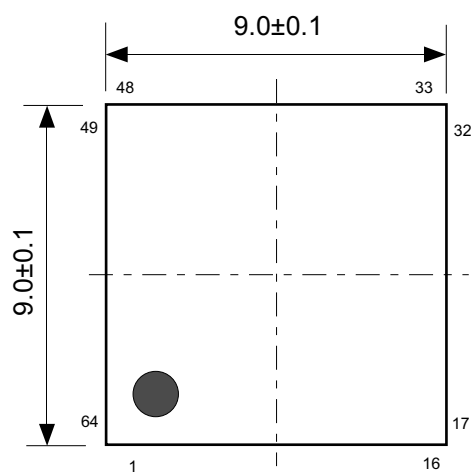
Fig. 9 Resistance to Soldering Heat Condition for Package (Reflow Method)

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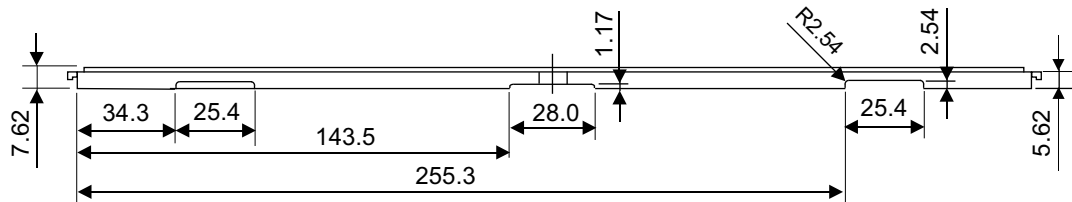
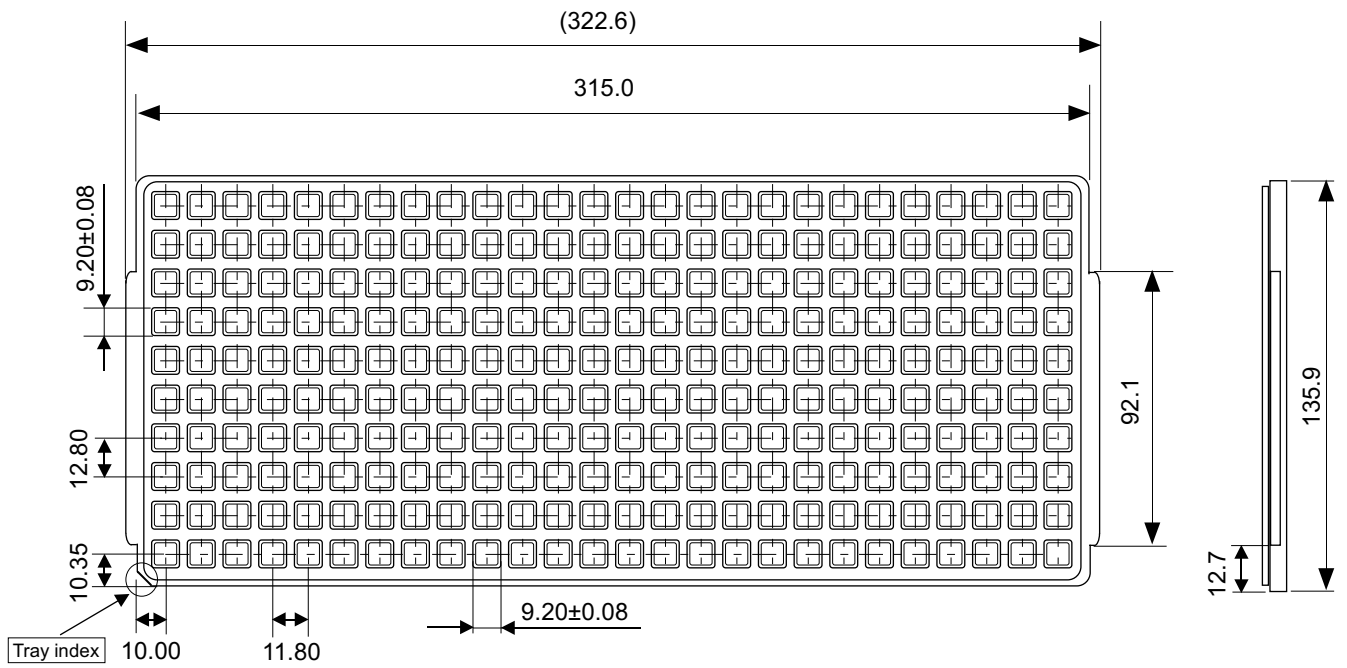
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 - 1.3 Those who deal with products should be grounded through a large series impedance around 100kΩ to 1MΩ.
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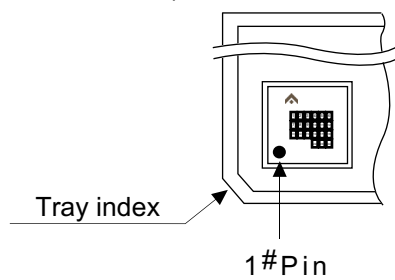


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UNIT	mm
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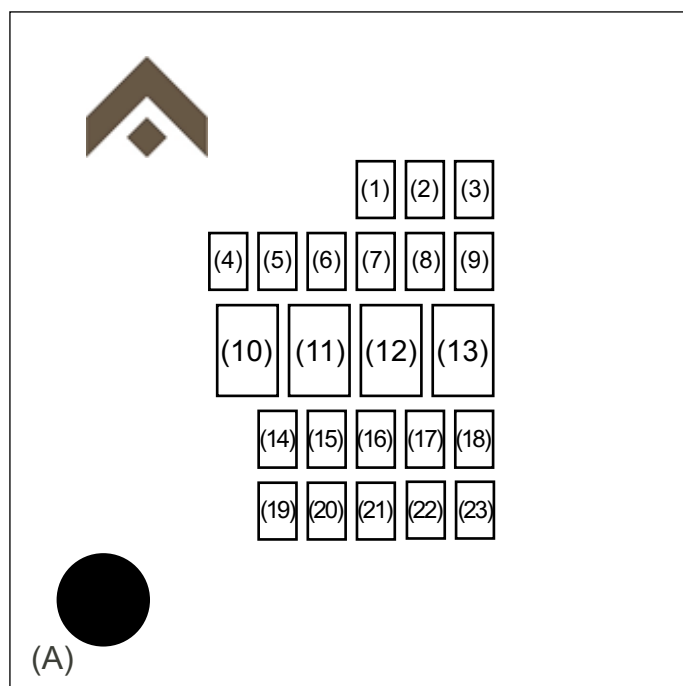


(Direction of IC in tray)



No. QFN9x9-B-T-SD-1.0

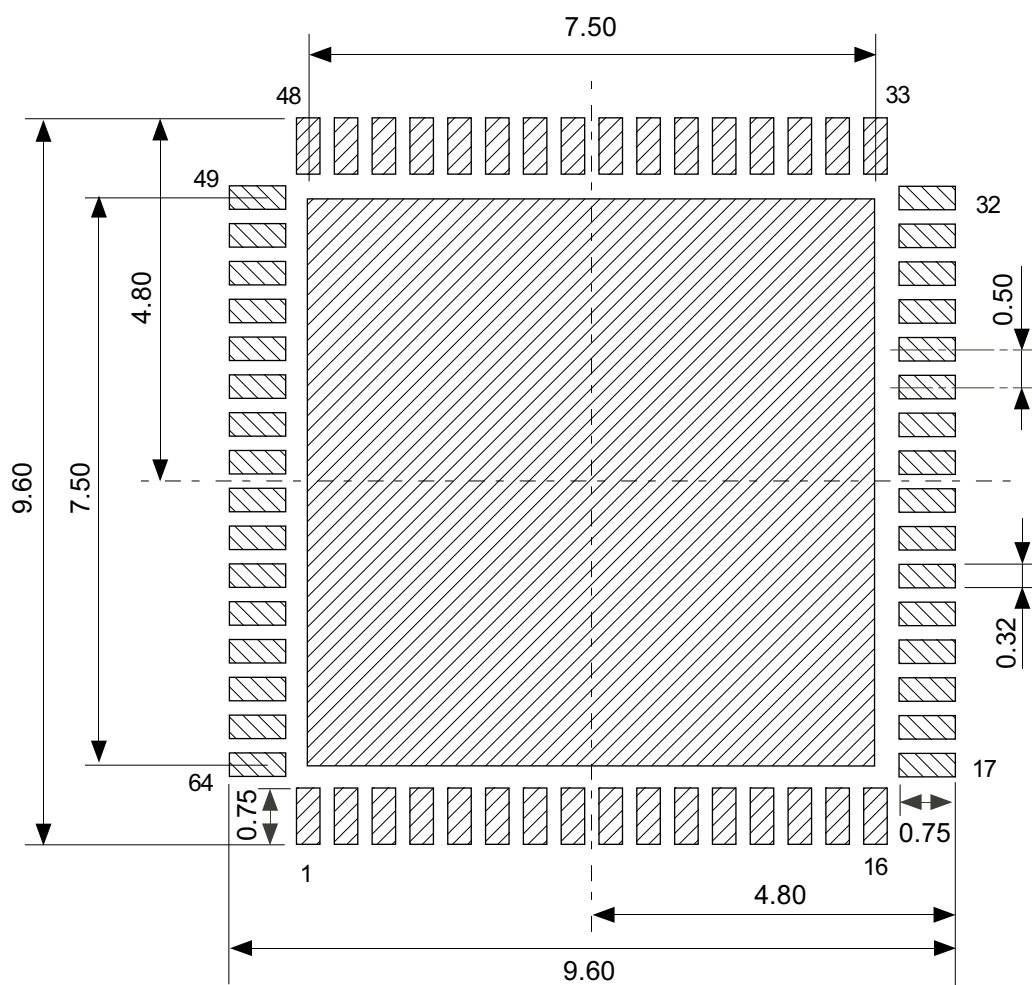
TITLE	QFN9x9-B-Tray		
No.	QFN9x9-B-T-SD-1.0		
ANGLE		QTY.	260
UNIT	mm		
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- (1) : Year of assembly
 (2) : Month of assembly
 (3) : Week of assembly
 (4) to (13) : Product code
 (14) to (23) : Quality control code
 (A) : 1-pin mark

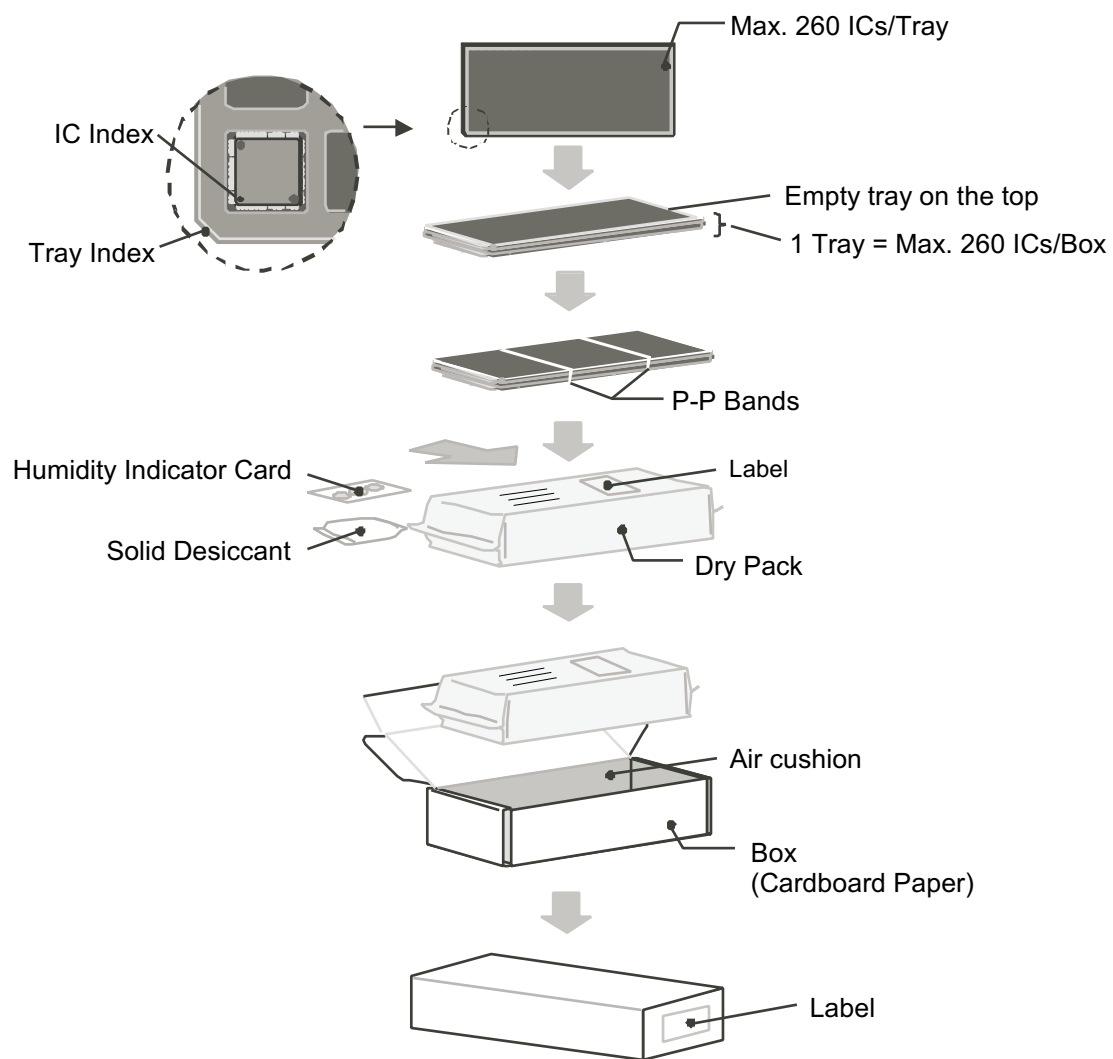
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TITLE	QFN64-B-Markings (S-UM5543 / S-UM5584)		
No.	QN064-B-M-S2-1.0		
ANGLE			
UNIT		TYPE	LASER
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No. QN064-B-L-SD-2.0

TITLE	QFN64-B -Land Recommendation
No.	QN064-B-L-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	



No. QN064-B-K-SD-2.0

TITLE	QFN64-B -Packing Procedure
No.	QN064-B-K-SD-2.0
ANGLE	
UNIT	
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