Features

- Six High-side and Six Low-side Drivers
- Outputs Freely Configurable as Switch, Half Bridge or H-bridge
- Capable to Switch all Kinds of Loads such as DC Motors, Bulbs, Resistors, Capacitors and Inductors
- 0.6A Continuous Current per Switch
- Low-side: R_{DSon} < 1.5Ω versus Total Temperature Range
- High-side: R_{DSon} < 2.0Ω versus Total Temperature Range
- Very Low Quiescent Current Is < 20 µA in Standby Mode
- Outputs Short-circuit Protected
- Overtemperature Prewarning and Protection
- Undervoltage Protection
- Various Diagnosis Functions such as Shorted Output, Open Load, Overtemperature and Power Supply Fail
- Serial Data Interface
- Operation Voltage up to 40V
- Daisy Chaining Possible
- SO28 Power Package

40-V Dual Hex Output Driver with Serial Input Control

T6816

1. Description

The T6816 is a fully protected driver interface designed in 0.8 µm BCDMOS technology. It is especially suitable for truck or bus applications and the industrial 24-V supply. It controls up to 12 different loads via a 16-bit dataword.

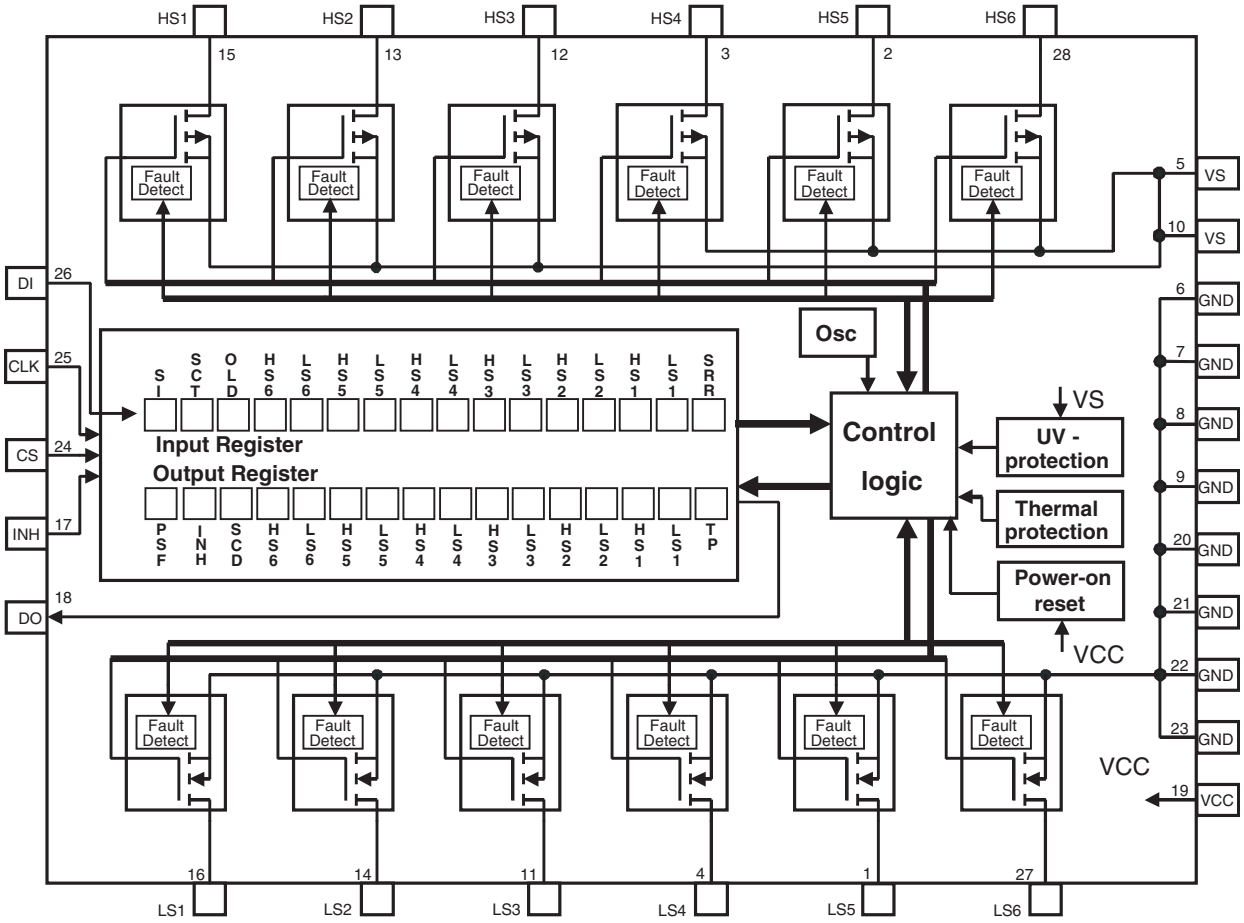
Each of the six high-side and six low-side drivers is capable to drive currents up to 600 mA. The drivers are freely configurable and can be controlled separately from a standard serial data interface. Therefore, all kinds of loads such as bulbs, resistors, capacitors and inductors can be combined. The IC is also designed to easily build H-bridges to drive DC motors in motion-control applications.

Protection is guaranteed in terms of short-circuit conditions, overtemperature and undervoltage. Various diagnosis functions and a very low quiescent current in standby mode open a wide range of applications.

Automotive qualification referring to conducted interferences, EMC protection and 2 kV ESD protection gives added value and enhanced quality for the exacting requirements of automotive applications.

4595G–BCD–04/09

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning SO28

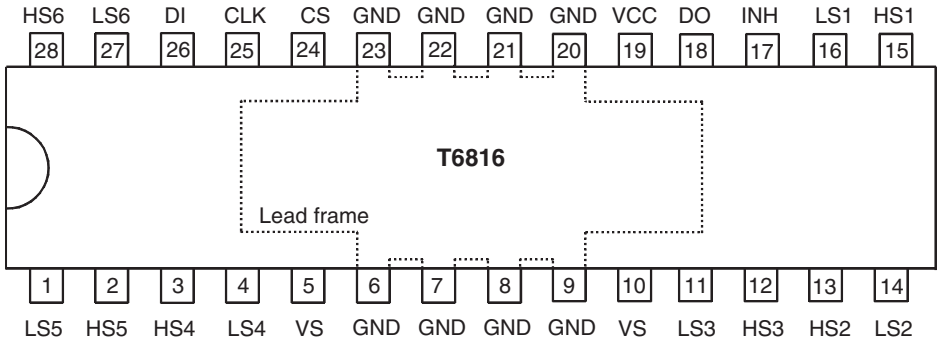


Table 2-1. Pin Description

Pin	Symbol	Function
1	LS5	Low-side driver output 5; Power-MOS open drain with internal reverse diode; short-circuit protection; diagnosis for short and open load
2	HS5	High-side driver output 5; Power-MOS open drain with internal reverse diode; short-circuit protection; diagnosis for short and open load
3	HS4	High-side driver output 4; see pin 2
4	LS4	Low-side driver output 4; see pin 1
5	VS	Power supply output stages HS4, HS5, HS6, internal supply; external connection to pin 10 necessary
6, 7, 8, 9	GND	Ground; reference potential; internal connection to pin 20-23; cooling tab
10	VS	Power supply output stages HS1, HS2 and HS3
11	LS3	Low-side driver output 3; see pin 1
12	HS3	High-side driver output 3; see pin 2
13	HS2	High-side driver output 2; see pin 2
14	LS2	Low-side driver output 2; see pin 1
15	HS1	High-side driver output 1; see pin 2
16	LS1	Low-side driver output 1; see pin 1
17	INH	Inhibit input; 5V logic input with internal pull down; low = standby, high = normal operating
18	DO	Serial data output; 5V CMOS logic level tri-state output for output (status) register data; sends 16-bit status information to the microcontroller (LSB is transferred first). Output will remain tri-stated unless device is selected by CS = low, therefore, several ICs can operate on one data output line only.
19	VCC	Logic supply voltage (5V)
20-23	GND	Ground; see pin 6-9
24	CS	Chip select input; 5V CMOS logic level input with internal pull up; low = serial communication is enabled, high = disabled
25	CLK	Serial clock input; 5V CMOS logic level input with internal pull down; controls serial data input interface and internal shift register (f_{max} = 2 MHz)
26	DI	Serial data input; 5V CMOS logic level input with internal pull down; receives serial data from the control device; DI expects a 16-bit control word with LSB being transferred first
27	LS6	Low-side driver output 6; see pin 1
28	HS6	High-side driver output 6; see pin 2

3. Functional Description

3.1 Serial Interface

Data transfer starts with the falling edge of the CS signal. Data must appear at DI synchronized to CLK and are accepted on the falling edge of the CLK signal. LSB (bit 0, SRR) has to be transferred first. Execution of new input data is enabled on the rising edge of the CS signal. When CS is high, pin DO is in tri-state condition. This output is enabled on the falling edge of CS. Output data will change their state with the rising edge of CLK and stay stable until the next rising edge of CLK appears. LSB (bit 0, TP) is transferred first.

Figure 3-1. Data Transfer Input Data Protocol

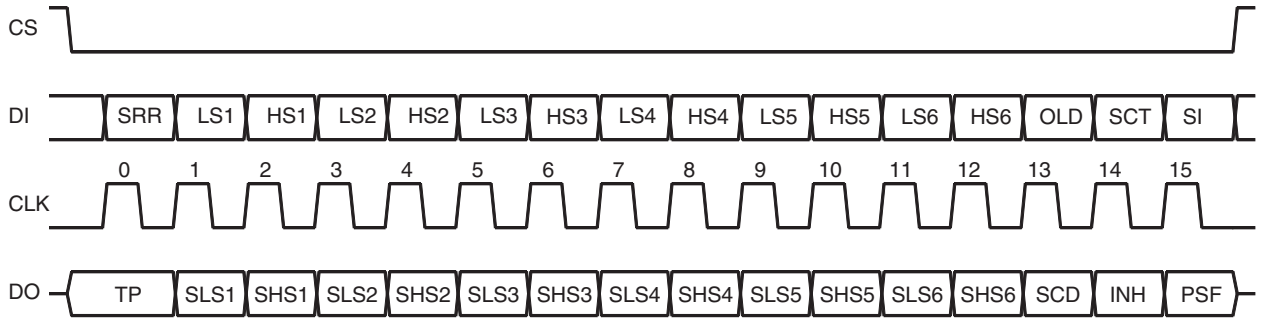


Table 3-1. Input Data Protocol

Bit	Input Register	Function
0	SRR	Status register reset (high = reset; the bits PSF, SCD and overtemperature shutdown in the output data register are set to low)
1	LS1	Controls output LS1 (high = switch output LS1 on)
2	HS1	Controls output HS1 (high = switch output HS1 on)
3	LS2	See LS1
4	HS2	See HS1
5	LS3	See LS1
6	HS3	See HS1
7	LS4	See LS1
8	HS4	See HS1
9	LS5	See LS1
10	HS5	See HS1
11	LS6	See LS1
12	HS6	See HS1
13	OLD	Open load detection (low = on)
14	SCT	Programmable time delay for short circuit (shutdown delay high/low = 12 ms/1.5 ms)
15	SI	Software inhibit; low = standby, high = normal operation (data transfer is not affected by standby function because the digital part is still powered)

Table 3-2. Output Data Protocol

Bit	Output (Status) Register	Function
0	TP	Temperature prewarning: high = warning (overtemperature shutdown see remark below)
1	Status LS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
2	Status HS1	Normal operation: high = output is on, low = output is off Open-load detection: high = open load, low = no open load (correct load condition is detected if the corresponding output is switched off)
3	Status LS2	Description see LS1
4	Status HS2	Description see HS1
5	Status LS3	Description see LS1
6	Status HS3	Description see HS1
7	Status LS4	Description see LS1
8	Status HS4	Description see HS1
9	Status LS5	Description see LS1
10	Status HS5	Description see HS1
11	Status LS6	Description see LS1
12	Status HS6	Description see HS1
13	SCD	Short circuit detected: set high, when at least one output is switched off by a short circuit condition
14	INH	Inhibit: this bit is controlled by software (bit SI in input register) and hardware inhibit (pin 17). High = standby, low = normal operation
15	PSF	Power supply fail: undervoltage at pin VS detected

Note: Bit 0 to 15 = high: overtemperature shutdown

Table 3-3. Status of the Input Register after Power on Reset

Bit 15 (SI)	Bit 14 (SCT)	Bit 13 (OLD)	Bit 12 (HS6)	Bit 11 (LS6)	Bit 10 (HS5)	Bit 9 (LS5)	Bit 8 (HS4)	Bit 7 (LS4)	Bit 6 (HS3)	Bit 5 (LS3)	Bit 4 (HS2)	Bit 3 (LS2)	Bit 2 (HS1)	Bit 1 (LS1)	Bit 0 (SRR)
H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L

3.2 Power Supply Fail

In case of undervoltage at pin VS, an internal timer is started. When the undervoltage delay time (t_{dUV}) programmed by the SCT bit is reached, the power supply fail bit (PSF) in the output register is set and all outputs are disabled. When normal voltage is present again, the outputs are enabled immediately. The PSF bit remains high until it is reset by the SRR bit in the input register.

3.3 Open-load Detection

If the open-load detection bit (OLD) is set to low, a pull-up current for each high-side switch and a pull-down current for each low-side switch is turned on (open-load detection current I_{HS1-6}, I_{LS1-6}). If $V_{VS} - V_{HS1-6}$ or V_{LS1-6} is lower than the open-load detection threshold (open-load condition), the corresponding bit of the output in the output register is set to high. Switching on an output stage with OLD bit set to low disables the open-load function for this output.

3.4 Overtemperature Protection

If the junction temperature exceeds the thermal prewarning threshold, $T_{jPW\ set}$, the temperature prewarning bit (TP) in the output register is set. When the temperature falls below the thermal prewarning threshold, $T_{jPW\ reset}$, the bit TP is reset. The TP bit can be read without transferring a complete 16-bit data word: with CS = high to low, the state of TP appears at pin DO. After the microcontroller has read this information, CS is set high and the data transfer is interrupted without affecting the state of the input and output registers.

If the junction temperature exceeds the thermal shutdown threshold, $T_{j\ switch\ off}$, the outputs are disabled and all bits in the output register are set high. The outputs can be enabled again when the temperature falls below the thermal shutdown threshold, $T_{j\ switch\ on}$, and when a high has been written to the SRR bit in the input register. Thermal prewarning and shutdown threshold have hysteresis.

3.5 Short-circuit Protection

The output currents are limited by a current regulator. Current limitation takes place when the overcurrent limitation and shutdown threshold (I_{HS1-6}, I_{LS1-6}) are reached. Simultaneously, an internal timer is started. The shorted output is disabled when during a permanent short the delay time (t_{dSd}) programmed by the short-circuit timer bit (SCT) is reached. Additionally, the short-circuit detection bit (SCD) is set. If the temperature prewarning bit TP in the output register is set during a short, the shorted output is disabled immediately and SCD bit is set. By writing a high to the SRR bit in the input register, the SCD bit is reset and the disabled outputs are enabled.

3.6 Inhibit

There are two ways to inhibit the T6816:

1. Set bit SI in the input register to zero
2. Switch pin 17 (INH) to 0V

In both cases, all output stages are turned off but the serial interface stays active. The output stages can be activated again by bit SI = 1 or by pin 17 (INH) switched back to 5V.

4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All values refer to GND pins

Parameter	Pin	Symbol	Value	Unit
Supply voltage	5, 10	V_{VS}	–0.3 to +40	V
Supply voltage t < 0.5 s; $I_S \geq -2$ A	5, 10	V_{VS}	–1	V
Supply voltage difference $\lvert V_{S\_pin5} - V_{S\_pin10} \rvert$		ΔV_{VS}	150	mV
Supply current	5, 10	I_{VS}	1.4	A
Supply current t < 200 ms	5, 10	I_{VS}	2.6	A
Logic supply voltage	19	V_{VCC}	–0.3 to +7	V
Input voltage	17	V_{INH}	–0.3 to +17	V
Logic input voltage	24 to 26	V_{DI}, V_{CLK}, V_{CS}	–0.3 to V_{VCC} +0.3	V
Logic output voltage	18	V_{DO}	–0.3 to V_{VCC} +0.3	V
Input current	17, 24 to 26	I_{INH}, I_{DI}, I_{CLK}, I_{CS}	–10 to +10	mA
Output current	18	I_{DO}	–10 to +10	mA
Output current	1 to 4, 11 to 16, 27 and 28	I_{LS1} to I_{LS6} I_{HS1} to I_{HS6}	Internal limited, see output specification	
Output voltage	2, 3, 12, 13, 15, 28	HS1 to HS6	–0.3 to +40	V
	1, 4, 11, 14, 16, 27	LS1 to LS6		
Reverse conducting current (t_{Pulse} = 150 µs)	2, 3, 12, 13, 15, 28 towards 5, 10	I_{HS1} to I_{HS6}	17	A
Junction temperature range		T_j	–40 to +150	°C
Storage temperature range		T_{STG}	–55 to +150	°C

5. Thermal Resistance

All values refer to GND pins

Parameter	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Junction pin	Measured to GND	6 to 9, 20 to 23	R_{thJP}			25	K/W
Junction ambient			R_{thJA}			65	K/W

6. Operating Range

All values refer to GND pins

Parameter	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit
Supply voltage		5, 10	V_{VS}	V_{UV}(1)		40	V
Logic supply voltage		19	V_{VCC}	4.5	5	5.5	V
Logic input voltage		17, 24 to 26	V_{INH}, V_{DI}, V_{CLK}, V_{CS}	–0.3		V_{VCC}	V
Serial interface clock frequency		25	f_{CLK}			2	MHz
Junction temperature range			T_j	–40		150	°C

Note: 1. Threshold for undervoltage detection.

7. Noise and Surge Immunity

Parameter	Test Conditions	Value
Conducted interferences	ISO 7637-1	Level 4(1)
Interference Suppression	VDE 0879 Part 2	Level 5
ESD (Human Body Model)	MIL-STD-883D Method 3015.7	2 kV
ESD (Machine Model)	EOS/ESD - S 5.2	150V

Note: 1. Test pulse 5: V_{Smax} = 40V

8. Electrical Characteristics

7.5V < V_{VS} < 40V; 4.5V < V_{VCC} < 5.5V; INH = High; –40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current Consumption**								
1.1	Quiescent current (VS)	V_{VS} < 28V, INH or bit SI = low	5, 10	I_{VS}			40	µA	A
1.2	Quiescent current (VCC)	4.5V < V_{VCC} < 5.5V, INH or bit SI = low	19	I_{VCC}			20	µA	A
1.3	Supply current (VS)	V_{VS} < 28V normal operating, all output stages off	5, 10	I_{VS}		0.8	1.2	mA	A
1.4	Supply current (VS)	V_{VS} < 28V normal operating, all output stages on, no load	5, 10	I_{VS}			10	mA	A
1.5	Supply current (VCC)	4.5V < V_{VCC} < 5.5V, normal operating pin	19	I_{VCC}			150	µA	A
2	**Internal Oscillator Frequency**								
2.1	Frequency (timebase for delay timers)			f_{OSC}	19		45	kHz	A
3	**Undervoltage Detection, Power-on Reset**								
3.1	Power-on reset threshold		19	V_{VCC}	3.4	3.9	4.4	V	A
3.2	Power-on reset delay time	After switching on V_{VCC}	19	t_{dPor}	30	95	160	µs	A
3.3	Undervoltage detection threshold		5, 10	V_{UV}	5.5		7.0	V	A
3.4	Undervoltage detection hysteresis		5, 10	ΔV_{UV}		0.4		V	A
3.5	Undervoltage detection delay		5, 10	t_{dUV}	7		21	ms	A
4	**Thermal Prewarning and Shutdown**								
4.1	Thermal prewarning		17	T_{jPWset}	125	145	165	°C	A
4.2	Thermal prewarning		17	$T_{jPWreset}$	105	125	145	°C	A
4.3	Thermal prewarning hysteresis			ΔT_{jPW}		20		K	A
4.4	Thermal shutdown		17	$T_{j\ switch\ off}$	150	170	190	°C	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.5V < V_{VCC} < 5.5V; INH = High; –40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.5	Thermal shutdown		17	$T_{j\ switch\ on}$	130	150	170	°C	A
4.6	Thermal shutdown hysteresis			$\Delta T_{j\ switch\ off}$		20		K	A
4.7	Ratio thermal shutdown/thermal prewarning			$T_{j\ switch\ off}/T_{jPW\ set}$	1.05	1.17			A
4.8	Ratio thermal shutdown/thermal prewarning			$T_{j\ switch\ on}/T_{jPW\ reset}$	1.05	1.2			A
5	**Output Specification (LS1-LS6, HS1-HS6)**								
5.1	On resistance	I_{Out} = 600 mA	1, 4, 11, 14, 16, 27	$R_{DS\ OnL}$			1.5	Ω	A
5.2	On resistance	I_{Out} = –600 mA	2, 3, 12, 13, 15, 28	$R_{DS\ OnH}$			2.0	Ω	A
5.3	Output clamping voltage	I_{LS1-6} = 50 mA	1, 4, 11, 14, 16, 27	V_{LS1-6}	40		60	V	A
5.4	Output leakage current	V_{LS1-6} = 40V all output stages off	1, 4, 11, 14, 16, 27	I_{LS1-6}			10	µA	A
5.5	Output leakage current	V_{HS1-6} = 0V all output stages off	2, 3, 12, 13, 15, 28	I_{HS1-6}	–10			µA	A
5.7	Inductive shutdown energy		1-4, 11-16, 27, 28	W_{outx}			15	mJ	D
5.8	Output voltage edge steepness		1-4, 11-16, 27, 28	dV_{LS1-6}/dt dV_{HS1-6}/dt	50	200	400	mV/µs	A
5.9	Overcurrent limitation and shutdown threshold		1-4, 11-16, 27	I_{LS1-6}	650	950	1250	mA	A
5.10	Overcurrent limitation and shutdown threshold		2, 3, 12,13, 15, 28	I_{HS1-6}	–1250	–950	–650	mA	A
5.11	Overcurrent shutdown delay time	Input register bit 14 (SCT) = low		t_{dSd}	1.0	1.5	2.0	ms	A
5.12	Open load detection current	Input register bit 13 (OLD) = low, output off	1, 4, 11,14, 16, 27	I_{LS1-6}	60		200	µA	A
5.13	Open load detection current	Input register bit 13 (OLD) = low, output off	2, 3, 12, 13 15, 28	I_{HS1-6}	–150		–30	µA	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level

8. Electrical Characteristics (Continued)

7.5V < V_{VS} < 40V; 4.5V < V_{VCC} < 5.5V; INH = High; –40°C < T_j < 150°C; unless otherwise specified, all values refer to GND pins.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.14	Open load detection current ratio			I_{LS1-6}/I_{HS1-6}	1.2				A
5.15	Open load detection threshold	Input register bit 13 (OLD) = low, output off	1, 4, 11,14, 16, 27	V_{LS1-6}	0.6		2	V	A
5.16	Open load detection threshold	Input register bit 13 (OLD) = low, output off	2, 3, 12, 13 15, 28	$V_{VS} – V_{HS1-6}$	0.6		2	V	A
5.17	Output switch on delay(1)	R_{Load} = 1 kΩ		t_{don}			0.5	ms	A
5.18	Output switch off delay(1)	R_{Load} = 1 kΩ		t_{doff}			1	ms	A
6	**Inhibit Input**								
6.1	Input voltage low level threshold		17	V_{IL}	$0.3 \times V_{VCC}$			V	A
6.2	Input voltage high level threshold		17	V_{IH}			$0.7 \times V_{VCC}$	V	A
6.3	Hysteresis of input voltage		17	ΔV_I	100		700	mV	A
6.4	Pull-down current	$V_{INH} = V_{VCC}$	17	I_{PD}	10		80	µA	A
7	**Serial Interface - Logic Inputs DI, CLK, CS**								
7.1	Input voltage low-level threshold		24-26	V_{IL}	$0.3 \times V_{VCC}$			V	A
7.2	Input voltage high-level threshold		24-26	V_{IH}			$0.7 \times V_{VCC}$	V	A
7.3	Hysteresis of input voltage		24-26	ΔV_I	50		500	mV	A
7.4	Pull-down current pin DI, CLK	V_{DI}, $V_{CLK} = V_{VCC}$	25, 26	I_{PDSI}	2		50	µA	A
7.5	Pull-up current pin CS	V_{CS}= 0V	24	I_{PUSI}	–50		–2	µA	A
8	**Serial Interface - Logic Output DO**								
8.1	Output voltage low level	I_{OL} = 3 mA	18	V_{DOL}			0.5	V	A
8.2	Output voltage high level	I_{OL} = –2 mA	18	V_{DOH}	V_{VCC} –0.7V			V	A
8.3	Leakage current (tri-state)	$V_{CS} = V_{VCC}$, 0V < V_{DO} < V_{VCC}	18	I_{DO}	–10		10	µA	A

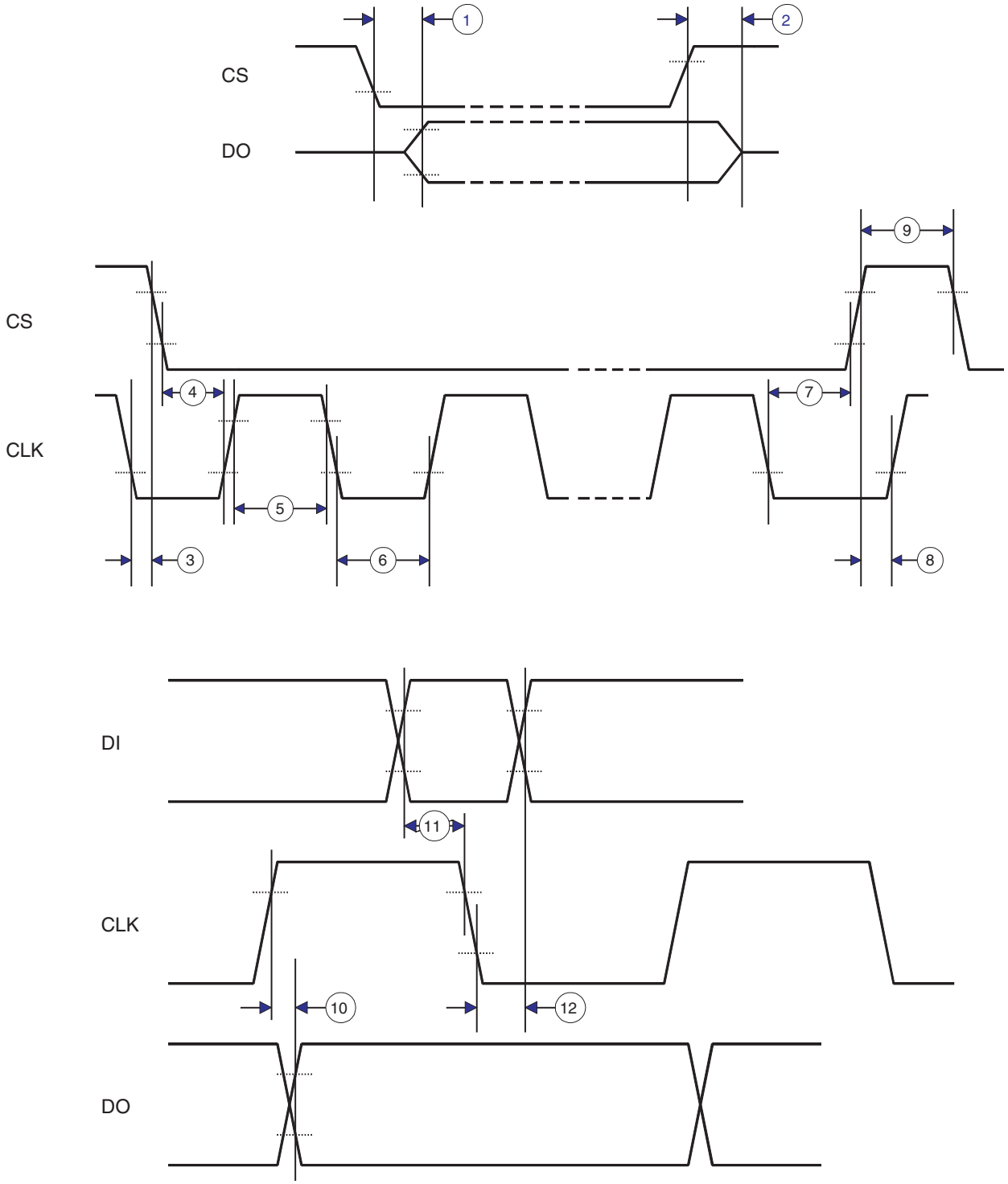
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes: 1. Delay time between rising edge of CS after data transmission and switch on output stages to 90% of final level

9. Serial Interface - Timing

Parameters	Test Conditions	Timing Chart No.	Symbol	Min.	Typ.	Max.	Unit
DO enable after CS falling edge	C_{DO} = 100 pF	1	t_{ENDO}			200	ns
DO disable after CS rising edge	C_{DO} = 100 pF	2	t_{DISDO}			200	ns
DO fall time	C_{DO} = 100 pF	–	t_{DOf}			100	ns
DO rise time	C_{DO} = 100 pF	–	t_{DOr}			100	ns
DO valid time	C_{DO} = 100 pF	10	t_{DOVal}			200	ns
CS setup time		4	$t_{CSSethl}$	225			ns
CS setup time		8	$t_{CSSetlh}$	225			ns
CS high time	Input register bit 14 (SCT) = high	9	t_{CSh}	16			ms
CS high time	Input register bit 14 (SCT) = low	9	t_{CSh}	2			ms
CLK high time		5	t_{CLKh}	225			ns
CLK low time		6	t_{CLKl}	225			ns
CLK period time		–	t_{CLKp}	500			ns
CLK setup time		7	$t_{CLKSethl}$	225			ns
CLK setup time		3	$t_{CLKSetlh}$	225			ns
DI setup time		11	t_{DIset}	40			ns
DI hold time		12	t_{DIHold}	40			ns

Figure 9-1. Serial Interface Timing with Chart Numbers

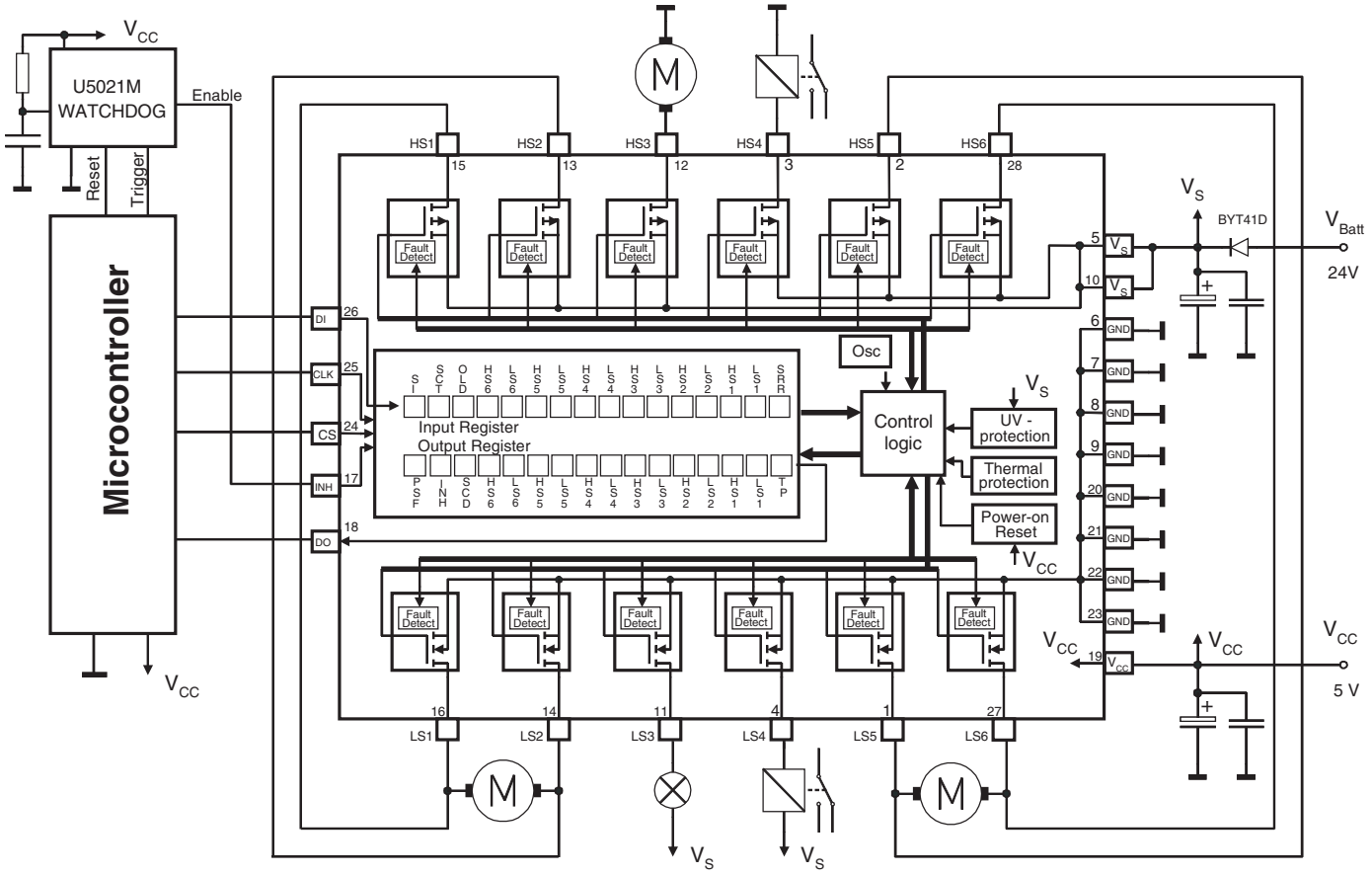


Inputs DI, CLK, CS: High level = $0.7 \times V_{CC}$, low level = $0.2 \times V_{CC}$

Output DO: High level = $0.8 \times V_{CC}$, low level = $0.2 \times V_{CC}$

10. Application

Figure 10-1. Application Circuit



10.1 Application Notes

It is strongly recommended to connect the blocking capacitors at V_{CC} and V_S as close as possible to the power supply and GND pins.

Recommended value for capacitors at V_S:
electrolythic capacitor C > 22 µF in parallel with a ceramic capacitor C = 100 nF. Value for electrolytic capacitor depends on external loads, conducted interferences and reverse conducting current I_{HSX} (see: Absolute Maximum Ratings).

Recommended value for capacitors at V_{CC}:
electrolythic capacitor C > 10 µF in parallel with a ceramic capacitor C = 100 nF.

To reduce thermal resistance it is recommended to place cooling areas on the PCB as close as possible to GND pins.

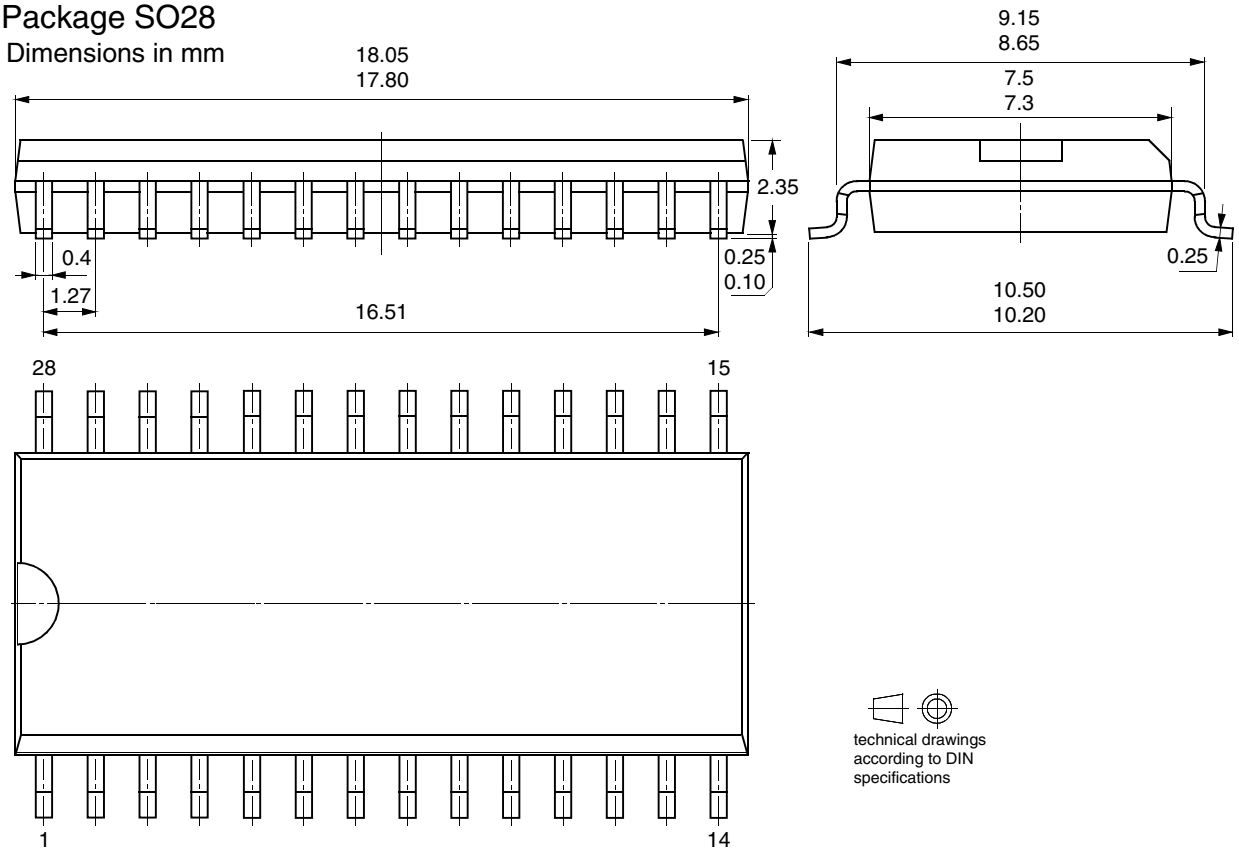
11. Ordering Information

Extended Type Number	Package	Remarks
T6816-TIQY	SO28	Power package, taped and reeled, Pb-free

12. Package Information

Package SO28

Dimensions in mm



13. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4595G-BCD-04/09	• Put datasheet in the newest template • Absolute Maximum Ratings table changed
4595F-BCD-02/08	• Put datasheet in the newest template • Pb-free logo on page 1 deleted • Section 8 “Electrical Characteristics” number 5 on page 9 changed
4595E-BCD-09/05	• Pb-free logo on page 1 added • Section 1 “Description” on page 1 changed • Ordering Information on page 14 changed
4595D-BCD-05/05	• Put datasheet in a new template • Table “Electrical Characteristics” rows 5.15 and 5.16 changed
4595C-BCD-04/04	• Put datasheet in a new template • Table “Absolute Maximum Ratings” on page 7 changed • Table “Electrical Characteristics” on page 10 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Atmel:
T6816-TIQY