embOS/IP Switch Board

User Guide & Reference Manual

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Manual versions

This manual describes the current hardware version. If you find an error in the manual or a problem in the hardware, please inform us and we will try to assist you as soon as possible. Contact us for further information on topics or functions that are not yet documented.

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Revision	Date	By	Description
1	16040x	OO	- Minor changes. - Restructuring.
0	160202	KB	Initial Release.

About this document

Assumptions

This document assumes that you already have a solid knowledge of the following:

- The software tools used for building your application (assembler, linker, C compiler).
- The C programming language.
- The target processor.
- DOS command line.

If you feel that your knowledge of C is not sufficient, we recommend *The C Programming Language* by Kernighan and Richie (ISBN 0–13–1103628), which describes the standard in C programming and, in newer editions, also covers the ANSI C standard.

How to use this manual

This manual explains all the functions and macros that the product offers. It assumes you have a working knowledge of the C language. Knowledge of assembly programming is not required.

Typographic conventions for syntax

This manual uses the following typographic conventions:

Style	Used for
Body	Body text.
`Keyword`	Text that you enter at the command prompt or that appears on the display (that is system functions, file- or pathnames).
`Parameter`	Parameters in API functions.
`Sample`	Sample code in program examples.
`Sample comment`	Comments in program examples.
Reference	Reference to chapters, sections, tables and figures or other documents.
GUIElement	Buttons, dialog boxes, menu names, menu commands.
Emphasis	Very important sections.

Table of contents

Chapter 1

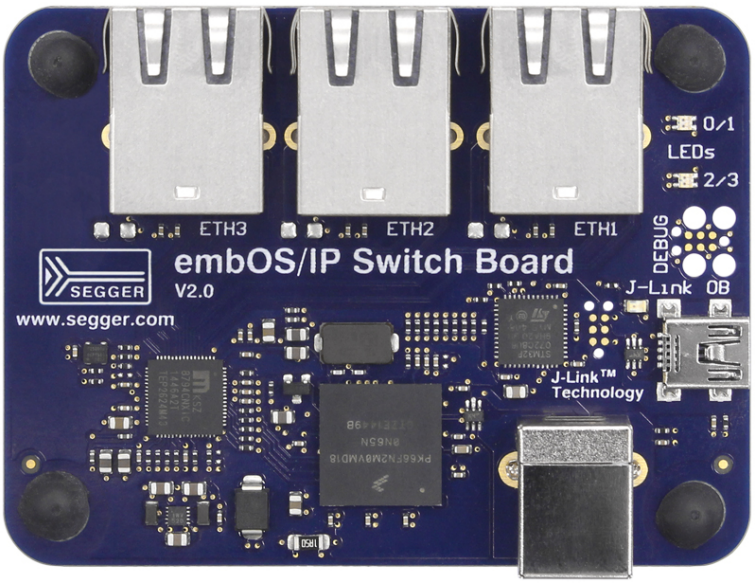
Introduction to embOS/IP Switch Board

This section presents an overview of embOS/IP Switch Board, its structure, and its capabilities.

The embOS/IP Switch Board is intended to be mainly a demonstrator board for the Tail Tagging add-on of SEGGER's embedded IP stack embOS/IP. Micrel/Microchip has developed switches which can expand one physical port into 1+n ports, supported by the so-called Tail Tagging mode. This enhancement allows to establish multiple physical external ports when only one physical Ethernet port is available on the CPU - by choosing another PHY. The board features an NXP Kinetis K66 CPU, Micrel/Microchip switch PHY KSZ8794CNX with three usable Ethernet ports and a J-Link OB debug probe.

The eval package is available for download and can be found here: https://www.segger.com/embos-ip-switch-board.html

This document is designed to give a quick overview on the features and specifications of the embOS/IP Switch Board. If you are looking for a detailed description of the embOS/IP Tail Tagging add-on, please refer to the product site at https://www.segger.com/embos-ip-tail-tagging.html



1.1 Overview on hardware features and specifications

1.1.1 Board main features:

- NXP Kinetis K66 MCU (MK66FN2M0VMD18)
- Micrel/Microchip KSZ8794CNX managed Ethernet switch with 3 external 10/100 ports and one Gigabit RGMII/MII/RMII uplink port
- 3 RJ45 Ethernet connectors
- On-board debug probe J-Link-OB with Drag & Drop (STM32F072, mini A/B-type connector)
- USB device: High speed, B-type connector
- LEDs: 2x BiColor red/green
- No jumpers or solder jumpers
- Rubber feet
- Dimensions 80 mm x 60 mm

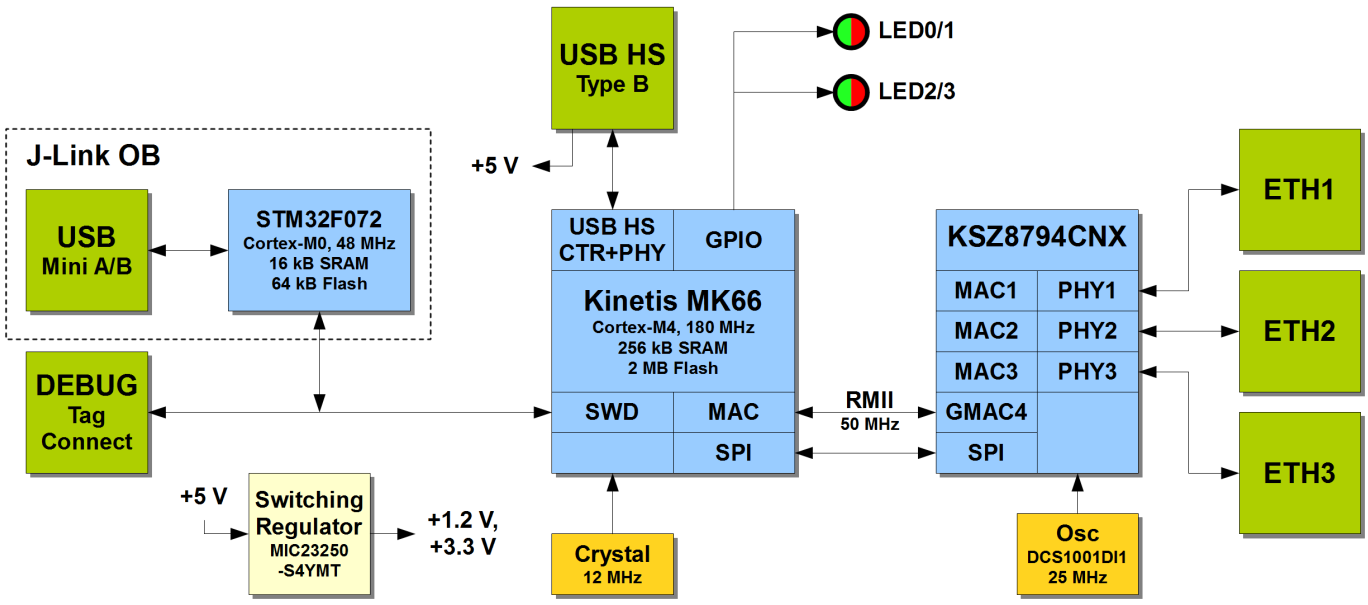
1.1.2 Controller main features:

- 180 MHz ARM Cortex-M4 based core with DSP instructions and Single Precision Floating Point unit
- 2 MB program flash memory, 256 KB RAM, 4 KB FlexRAM
- Memory protection unit with multi-master protection
- Ethernet controller with RMII interface to external PHY and hardware IEEE 1588 capability
- USB high-/full-/low-speed On-the-Go with on-chip high speed transceiver

1.1.3 Switch main features:

- Layer 2 managed 4-port switch
- 3 10/100 Mbps copper ports + 1 10/100/1000 Mbps uplink port
- Internal biasing, on-chip termination
- Enhanced power management features incl. Energy Efficient Ethernet (EEE), PME, WoL
- Programmable rate limiting and priority ratio
- Tagged and port-based VLAN
- Port based security and ACL-rule based packet filtering technology
- QoS priority with four queues
- High-performance memory bandwidth and a shared memory-based switch fabric with non-blocking support

1.2 Functional block diagram

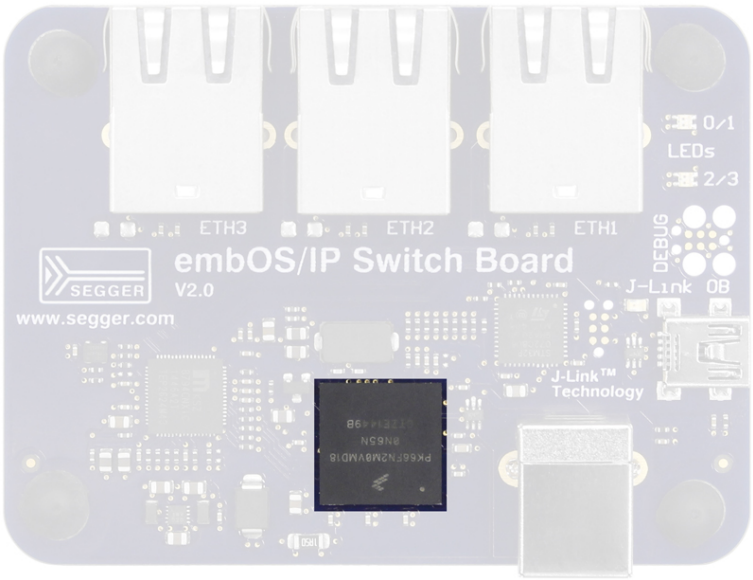


Chapter 2

Functional Description

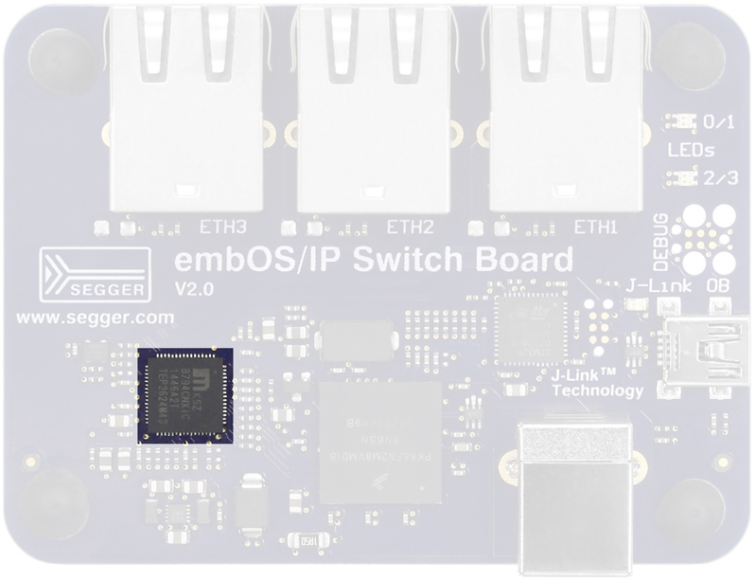
This section describes the hardware features from a functional point of view.

2.1 NXP Kinetis K66 MCU (MK66FN2M0VMD18)



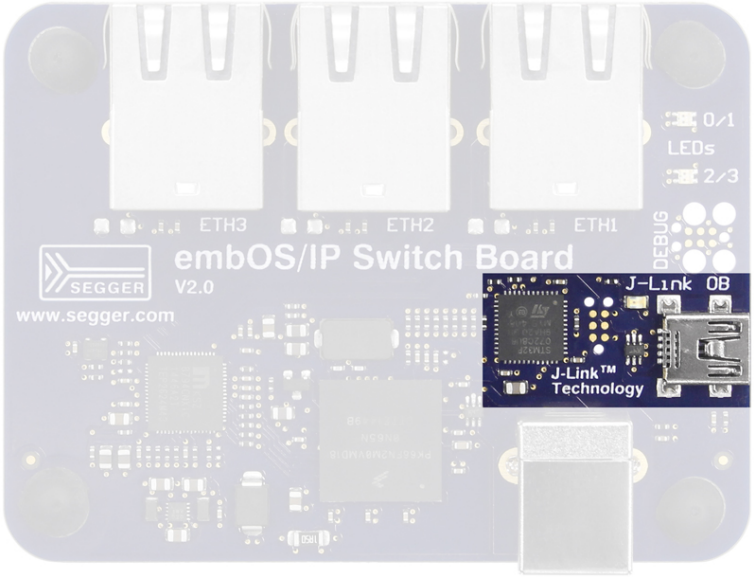
As microcontroller an NXP Kinetis K66 is used. It is clocked at 180 MHz and comes with 256 KB SRAM as well as 2 MB Flash memory. Main peripheral functions used in this application are the USB2.0 controller with an integrated HS USB PHY and one Ethernet controller.

2.2 Micrel/Microchip Managed Ethernet Switch (KSZ8794CNX)



The KSZ8794CNX is a highly integrated, Layer 2 managed, four-port switch. This switch has three MACs, one GMAC (for uplink) and three PHYs that are fully compliant with the IEEE 802.3u standard. It is intended for applications requiring three 10/100Mbps copper ports and one 10/100/1000Mbps Gigabit uplink port. The KSZ8794CNX incorporates a small package outline, lowest power consumption with internal biasing, and on-chip termination. Its extensive features set includes enhanced power management, programmable rate limiting and priority ratio, tagged and port-based VLAN, port-based security and ACL rule-based packet filtering technology, QoS priority with four queues, management interfaces, enhanced MIB counters, high-performance memory bandwidth, and a shared memory-based switch fabric with non-blocking support. The KSZ8794CNX provides support for multiple CPU data interfaces to effectively address both current and emerging fast Ethernet and Gigabit Ethernet applications where the GMAC interface can be configured to any of RGMII, MII and RMII modes.

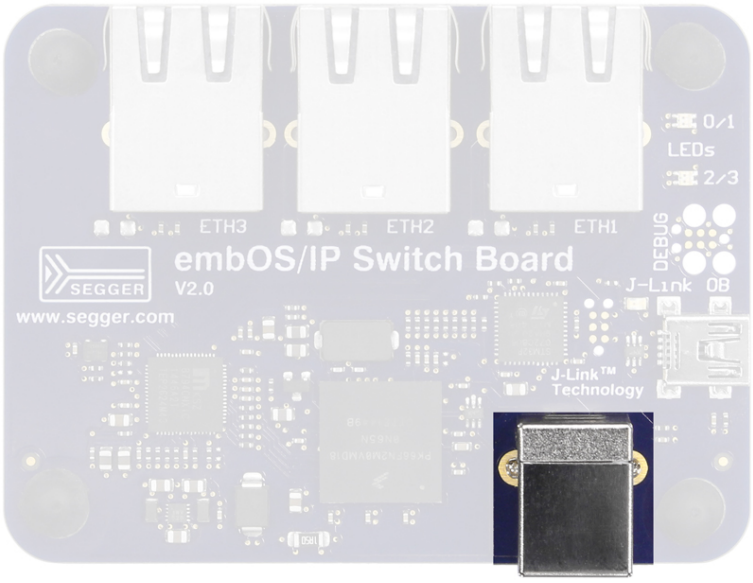
2.3 Debug Access



Quick and easy debug access to the Kinetis core MCU can be achieved by the J-Link OB, SEGGER's on-board debug probe. It connects to the debug host through a USB2.0 FS interface. Alternatively regular debug probes from the J-Link series (J-Link BASE/PLUS/ ULTRA+/PRO) can be used by means of a TagConnect debug footprint for use with SEGGER's J-Link Needle Adapter. Details can be found here: https://www.segger.com/jlink-needle-adapter.html

2.4 USB/Power Supply

The embOS/IP Switch board is powered by the USB device connector (B-type connector). Current consumption drawn depends on the configuration and connected Ethernet links. Idle consumption is approx. 140 mA. This USB interface can be used for a connection to a host providing High Speed USB2.0 device functionality (if provided by the application).



Chapter 3

Quick Start

For quick start instructions for your new embOS/IP Switch Board please refer to the following location: https://www.segger.com/start-embos-ip-switch-board.html

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