

System Power Supply LSI Series for Use in Automotive Electronics

Multifunction System Power Supply IC with mute function

BA4907FP



●Description

The BA4907FP system power supply features multiple microcontroller outputs and is capable of operating on a very low standby current. It incorporates a built-in reset with a microcontroller delay and a BATTERY/ACCESSORY voltage detection, and is ideal for car audio and satellite navigation systems.

●Features

- 1) Very low standby current: 125 μ A
- 2) Built-in 5 V microcontroller power supply
- 3) Built-in 5 V power supplies
- 4) Built-in current amplifier pins using external transistors
- 5) The IC monitors the +B voltage and outputs the results of comparing it to the internally set voltage to the BUF pin.
- 6) The IC monitors the ACC voltage and outputs the results of comparing it to the internally set voltage to the ACCO pin.
- 7) The IC monitors the VDD voltage and outputs the results of comparing it to the internally set voltage to the RESET pin.
- 8) The delay time from output voltage detection to the RESET signal can be set externally for the RESET circuit.
- 9) The ability to operate VDD using the charge stored in a backup capacitor makes the IC unlikely to malfunction in the event of a sudden BATTERY power failure.
- 10) Built-in overcurrent protection circuits protect the IC from damage in the event of an output short.
- 11) Built-in overvoltage protection circuits make the IC resistant to VCC and ACC surge input.
- 12) Built-in thermal shutdown circuits protect the IC from thermal destruction.
- 13) Power package gives the IC large power dissipation capabilities and is ideal for space-saving designs.

●Applications

Car audio and satellite navigation systems

● **Absolute maximum ratings** (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	VCC	36	V
Power Dissipation 1	Pd1	0.85	W
Power Dissipation 2 (*1)	Pd2	1.45	W
Power Dissipation 3 (*2)	Pd3	6.60	W
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
Peak Supply Voltage	VCC PEAK	50 (Note 1)	V

*1: When mounted on a glass epoxy board (70 mm × 70 mm × 1.6 mm [thickness]) (25°C).

*2: When using an infinite heat sink (75°C).

Note 1: tr ≥ 1 ms; Bias voltage is applied for less than 200 ms.

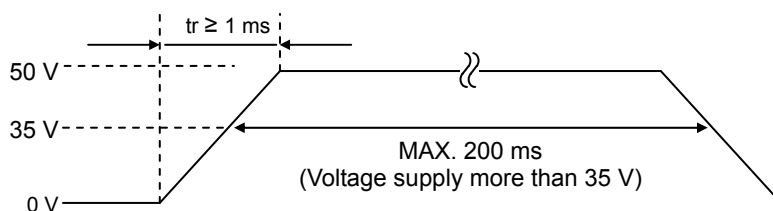


Fig.1 Peak Supply Voltage Waveform

● **Recommended operating conditions** (Ta = 25°C)

Parameter	Min.	Typ.	Max.	Unit
Recommended Supply Voltage Range	7.85	14.4	18	V

*Electrical characteristics are not guaranteed (especially when operating on).

● **Electrical characteristics** (Unless otherwise specified, Ta = 25°C; VCC = 14.4 V)

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
Standby Current	—	125	150	μA	VCC = 14.4 V
[Output Block]					
Output Voltage (VDD)	4.75	5.0	5.25	V	Io = 150 mA
Line Regulation	—	5	50	mV	7.85 V ≤ VCC ≤ 18 V
Load Regulation	—	90	—	mV	5 mA ≤ Io ≤ 150 mA
Dropout Voltage	—	1.9	2.6	V	VCC ≥ 5 V
Peak Output Current	100	—	—	mA	
Ripple Rejection	—	60	—	dB	

◎ This IC is not designed to be radiation-resistant.

● **Electrical characteristics** (Unless otherwise specified, Ta = 25°C; VCC = 14.4 V)

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
Output Voltage (REG1)	4.75	5.0	5.25	V	Io = 50 mA
Line Regulation	—	10	—	mV	7.85 V ≤ VCC ≤ 18 V, Io = 50 mA
Load Regulation	—	90	—	mV	Io = 0 mA to 50 mA
Dropout Voltage	—	1.9	2.6	V	Io = 50 mA
Peak Output Current	100	—	—	mA	VREG1 ≥ 4.75 V
Ripple Rejection	—	60	—	dB	f = 100 Hz, VRR = -10 dBV
Output Voltage (REG2)	4.75	5.0	5.25	V	Io = 10 mA
Line Regulation	—	10	—	mV	7.85 V ≤ VCC ≤ 18 V, Io = 10 mA
Load Regulation	—	90	—	mV	Io = 0 mA to 10 mA
Dropout Voltage	—	1.9	2.6	V	Io = 10 mA
Peak Output Current	100	—	—	mA	VREG2 ≥ 4.75 V
Ripple Rejection	—	60	—	dB	f = 100 Hz, VRR = -10 dBV
[VBU Detector Block]					
Detection Voltage H	6.2	7.5	8.1	V	VBU voltage
Detection Voltage L	—	2.25	—	V	VBU voltage
Hysteresis Width	—	5.25	—	V	
[RESET Block]					
Detection Voltage	2.7	2.8	2.9	V	VDD voltage
Sink Current	1	4	—	mA	RESET ≤ 0.5 V
RESET Pull Up Resistance	2.5	3.1	3.7	KΩ	VDD = 5 V
C Terminal Voltage	3.00	3.33	3.66	V	VDD = 5 V
Charge Resistance	160	200	240	KΩ	*VDD = 5 V
RESET Rise Time	—	—	50	μsec	
RESET Fall Time	—	—	50	μsec	
[BATT Voltage Detection]					
Threshold Voltage	1.18	1.23	1.28	V	L→H
Hysteresis Width	36	72	144	mV	
BUF Voltage H	4.0	—	5.25	V	Io = 5 μA
BUF Voltage L	—	—	0.5	V	I1 = 0 mA
Output Current H	5	10	—	mA	VOH ≥ 4 V
Output Current L	0.1	0.2	—	mA	VOL ≤ 0.5 V
BUF Rise Time	—	—	50	μsec	
BUF Fall Time	—	—	50	μsec	

*Delay time (t = 200 KΩ × 1.15C (s))

◎ This IC is not designed to be radiation-resistant.

● **Electrical characteristics** (Unless otherwise specified, Ta = 25°C; VCC = 14.4 V)

Parameter	Limits			Unit	Condition
	Min.	Typ.	Max.		
[ACC Voltage Detection]					
Threshold Voltage	1.18	1.23	1.28	V	L→H
Hysteresis Width	36	72	144	mV	
Output Voltage H	4.0	—	5.25	V	I _o = 5 μA
Output Voltage L	—	—	0.5	V	I _l = 0 mA
Output Current H	5	10	—	mA	VOH ≥ 4 V
Output Current L	0.1	0.2	—	mA	VOL ≤ 0.5 V
ACC Rise Time	—	—	50	μsec	
ACC Fall Time	—	—	50	μsec	
Backup-switch					
VBU Peak Output Current	0.2	0.3	—	A	VBU > 5 V
Reverse Current	—	—	200	μA	VCC = 0 V, VBU = 12 V
REG1SW					
Standby Level	—	—	1.4	V	
Active Level	2.2	—	—	V	
SW Input Current	13	25	37	μA	REG1SW = 5 V
REG2SW					
Standby Level	—	—	1.4	V	
Active Level	2.2	—	—	V	
SW Input Current	13	25	37	μA	REG2SW = 5 V
REG3SW					
Standby Level	—	—	1.4	V	
Active Level	2.2	—	—	V	
SW Input Current	13	25	37	μA	REG3SW = 5 V
REG3					
Output Voltage	4.75	5	5.25	V	
Base Current	7	—	—	mA	Vo ≥ 4.75 V

● This IC is not designed to be radiation-resistant.

●Reference data

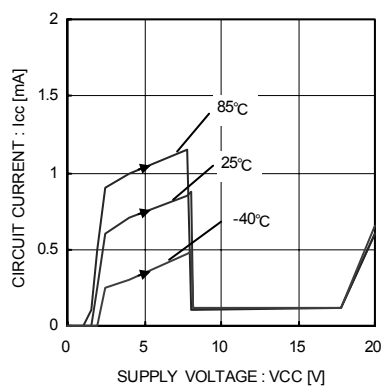


Fig. 2 Standby Current

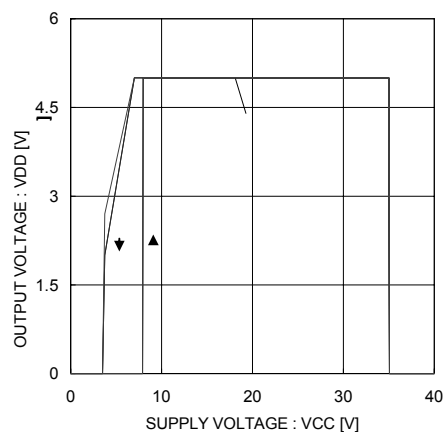


Fig. 3 VDD Line Regulation
($I_o = 150 \text{ mA}$)

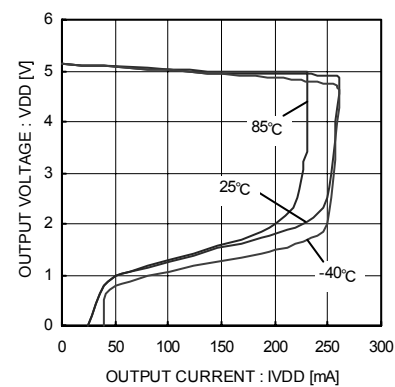


Fig. 4 VDD Load Regulation

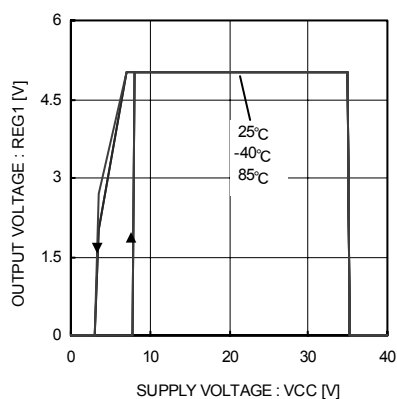


Fig. 5 REG1 Line Regulation
($I_o = 50 \text{ mA}$)

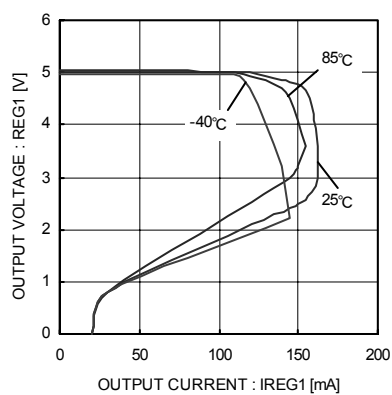


Fig. 6 REG1 Load Regulation

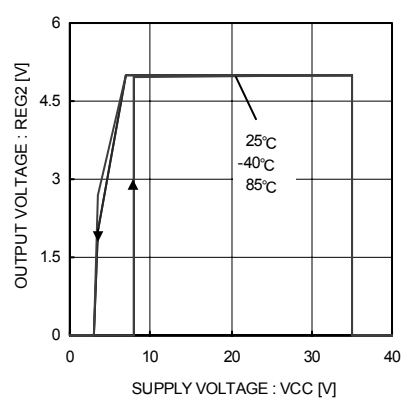


Fig. 7 REG2 Line Regulation
($I_o = 10 \text{ mA}$)

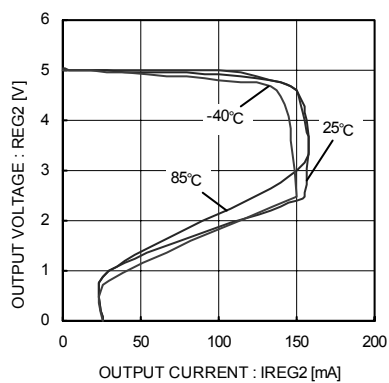


Fig. 8 REG2 Load Regulation

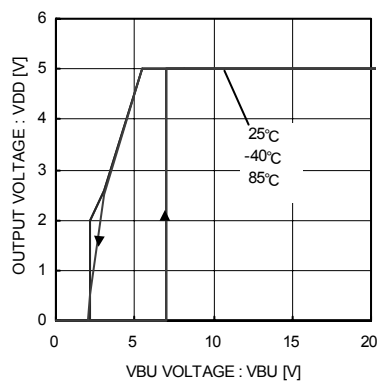


Fig. 9 VBU Threshold Voltage

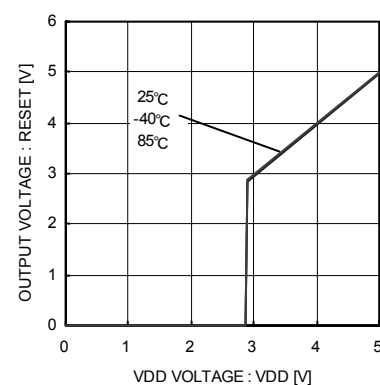


Fig. 10 RESET Detection Voltage

●Reference data

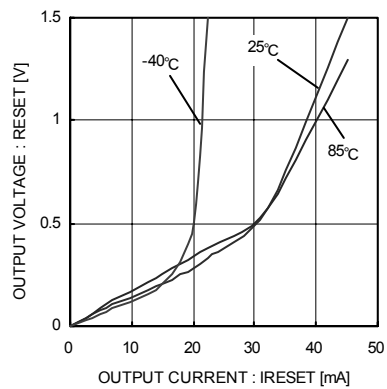


Fig. 11 RESET Sink Current

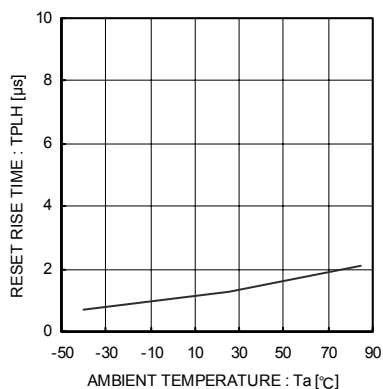


Fig. 12 RESET Rise Time

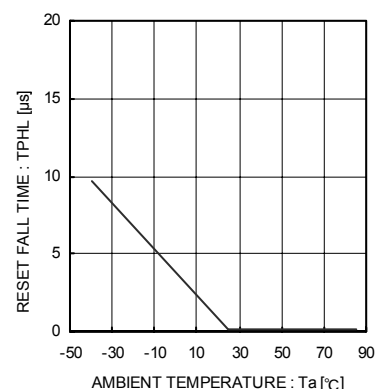


Fig. 13 RESET Fall Time

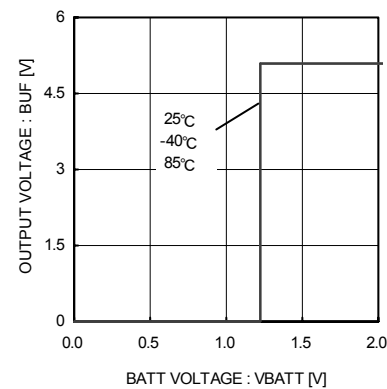


Fig. 14 BATT Threshold Voltage

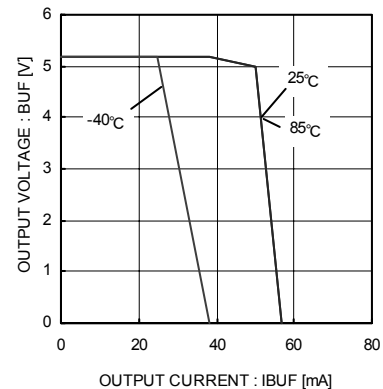


Fig. 15 BUF High Voltage

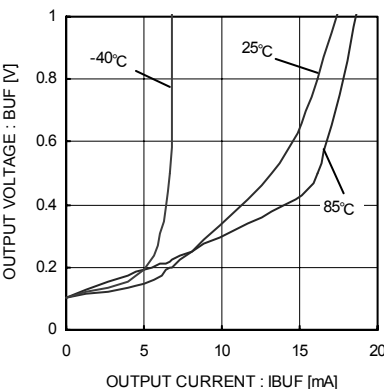


Fig. 16 BUF Low Voltage

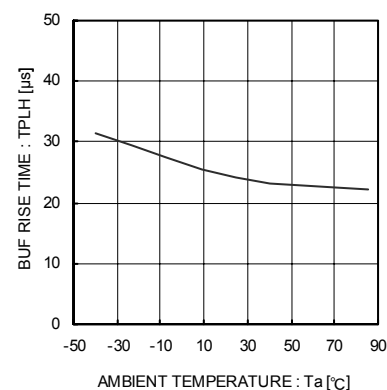


Fig. 17 BUF Rise Time

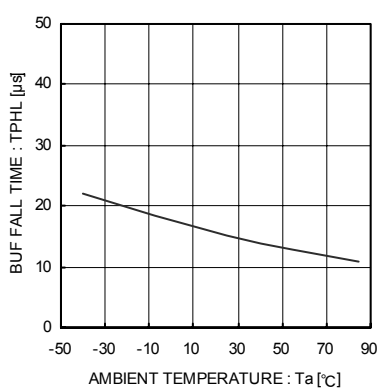


Fig. 18 BUF Fall Time

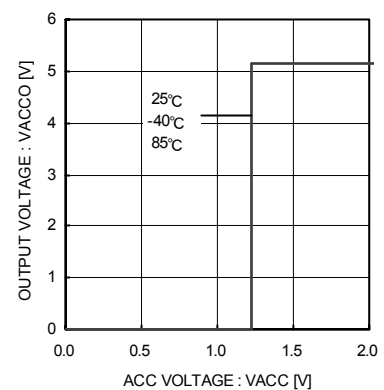


Fig. 19 ACC Threshold Voltage

●Reference data

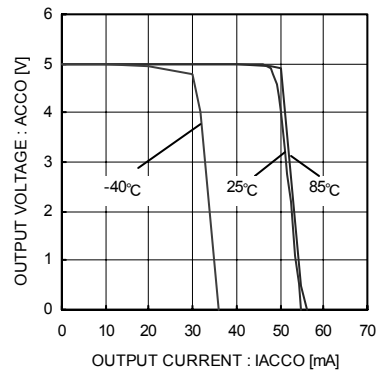


Fig. 20 ACCO High Voltage

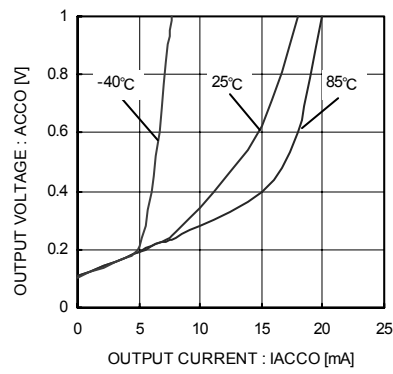


Fig. 21 ACCO Low Voltage

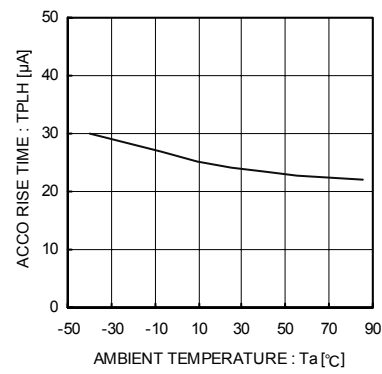


Fig. 22 ACC Rise Time

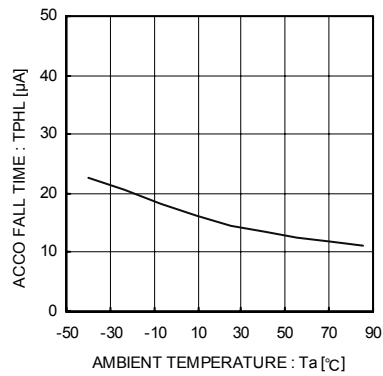


Fig. 23 ACC Fall Time

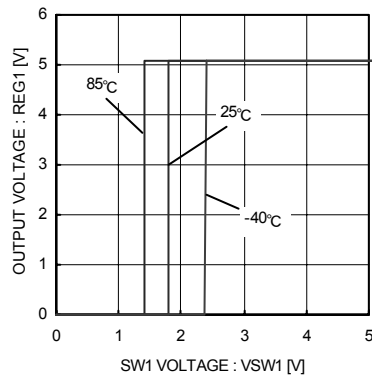


Fig. 24 SW1 Threshold Voltage

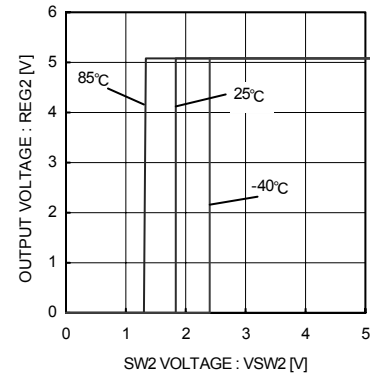


Fig. 25 SW2 Threshold Voltage

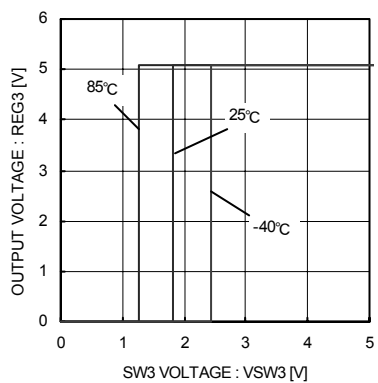


Fig. 26 SW3 Threshold Voltage

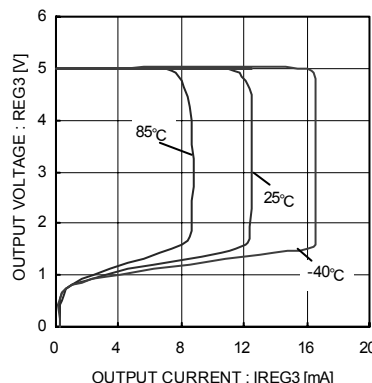


Fig. 27 REG3 Base Current

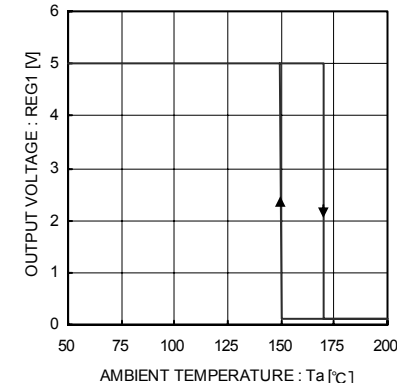


Fig. 28 Thermal Shutdown Operation

●Block diagram

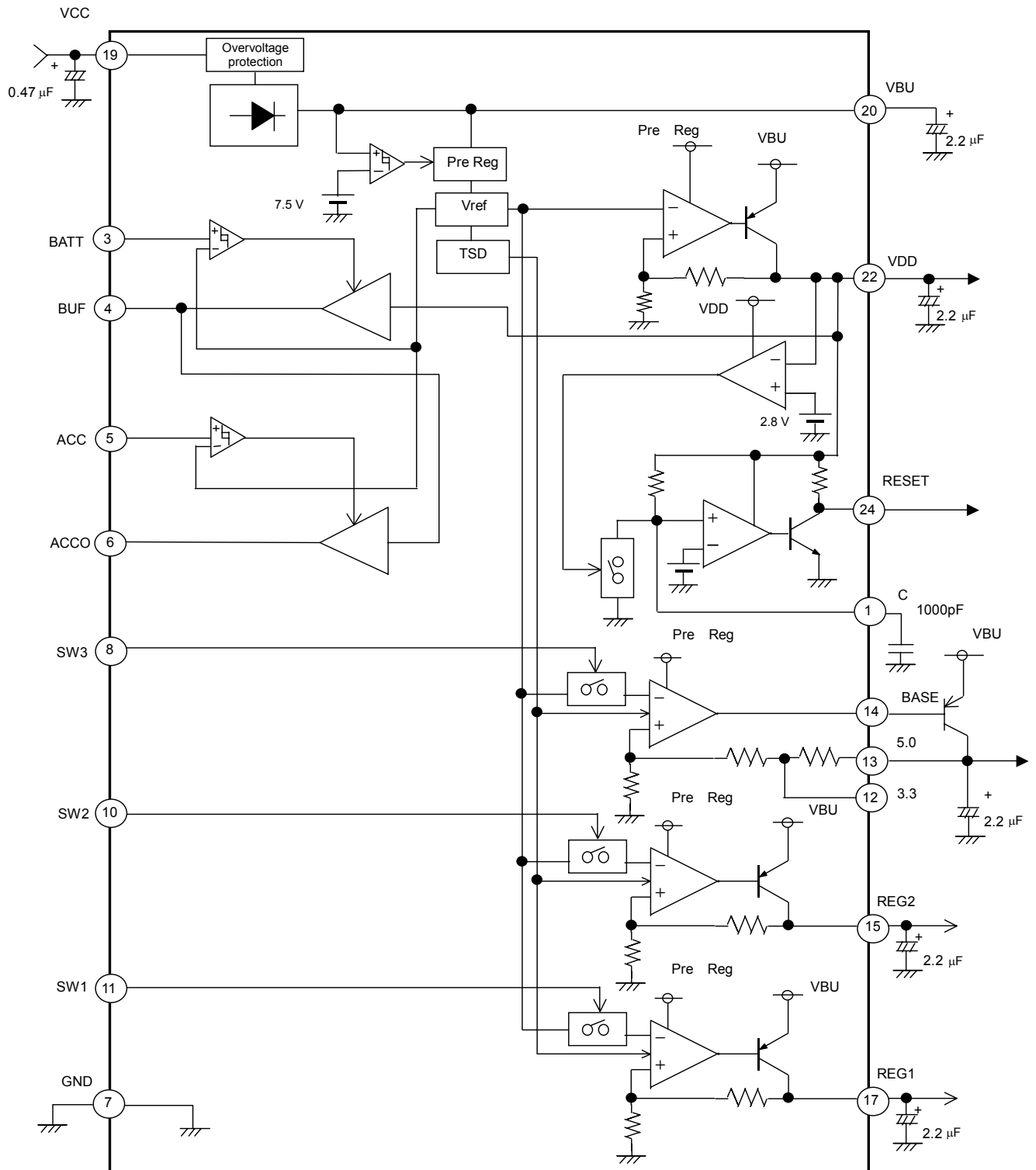


Fig. 29 Block Diagram

●Pin descriptions

No.	Pin name	Function
1	C	Pin for setting a delay in RESET rising time.
2	N.C.	Not connected to the IC internally.
3	BATT	Input pin for low BATTERY detection.
4	BUF	Output pin for the low BATTERY detection signal. (The low-level BUF signal is output when the BATT is low.)
5	ACC	Input pin for monitoring ACCESSORY power supply voltage.
6	ACCO	Input pin for ACC voltage drop detection. (The low-level ACCO signal is output when the ACC is low.)
FIN	FIN	Connected to the substrate of the IC.
7	GND	GND pin of the IC.
8	SW3	Control pin of external component output. (The external transistor turns on with the SW3 set to high level.)
9	N.C.	Not connected to the IC internally.
10	SW2	Control pin for REG2 output. (REG2 turns on with SW2 set to high level.)
11	SW1	Control pin for REG1 output. (REG1 turns on with SW1 set to high level.)
12	3.3	3.3 V is output by shorting this pin to the 5.0 pin.
13	5.0	5.0 V is output by connecting this pin to the collector of the external transistor.
14	BASE	Base drive pin of the external transistor.
15	REG2	5.0 V is output with a maximum output current of 100 mA.
16	N.C.	Not connected to the IC internally.
17	REG1	5.0 V is output with a maximum output current of 100 mA.
18	N.C.	Not connected to the IC internally.
19	VCC	BATTERY power supply connection pin.
20	VBU	Backup capacitor connection pin.
21	N.C.	Not connected to the IC internally.
22	VDD	5.0 V is output with a maximum output current of 100 mA.
23	N.C.	Not connected to the IC internally.
24	RESET	Reset signal output pin. (Low-level RESET signal is output when the VDD is low.)
25	N.C.	Not connected to the IC internally.

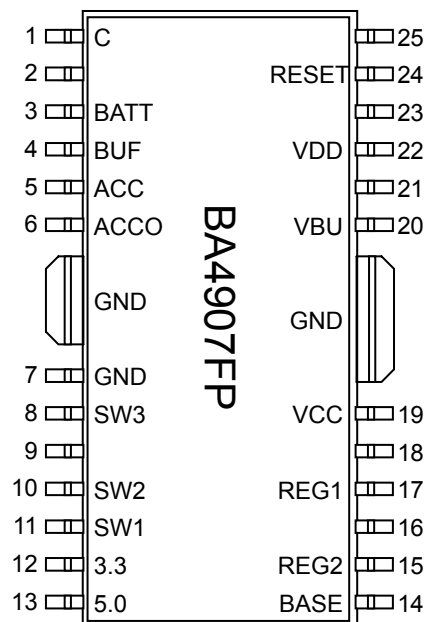


Fig. 30 Pin Assignment Diagram

●I/O Timing chart

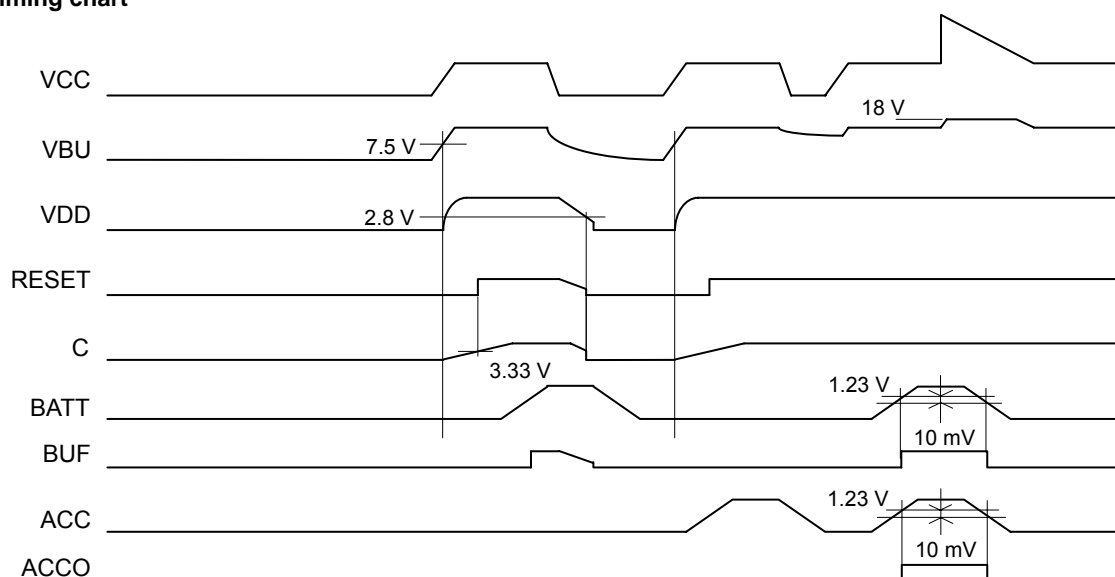


Fig. 31 Timing Chart

●I/O Equivalent circuit diagrams

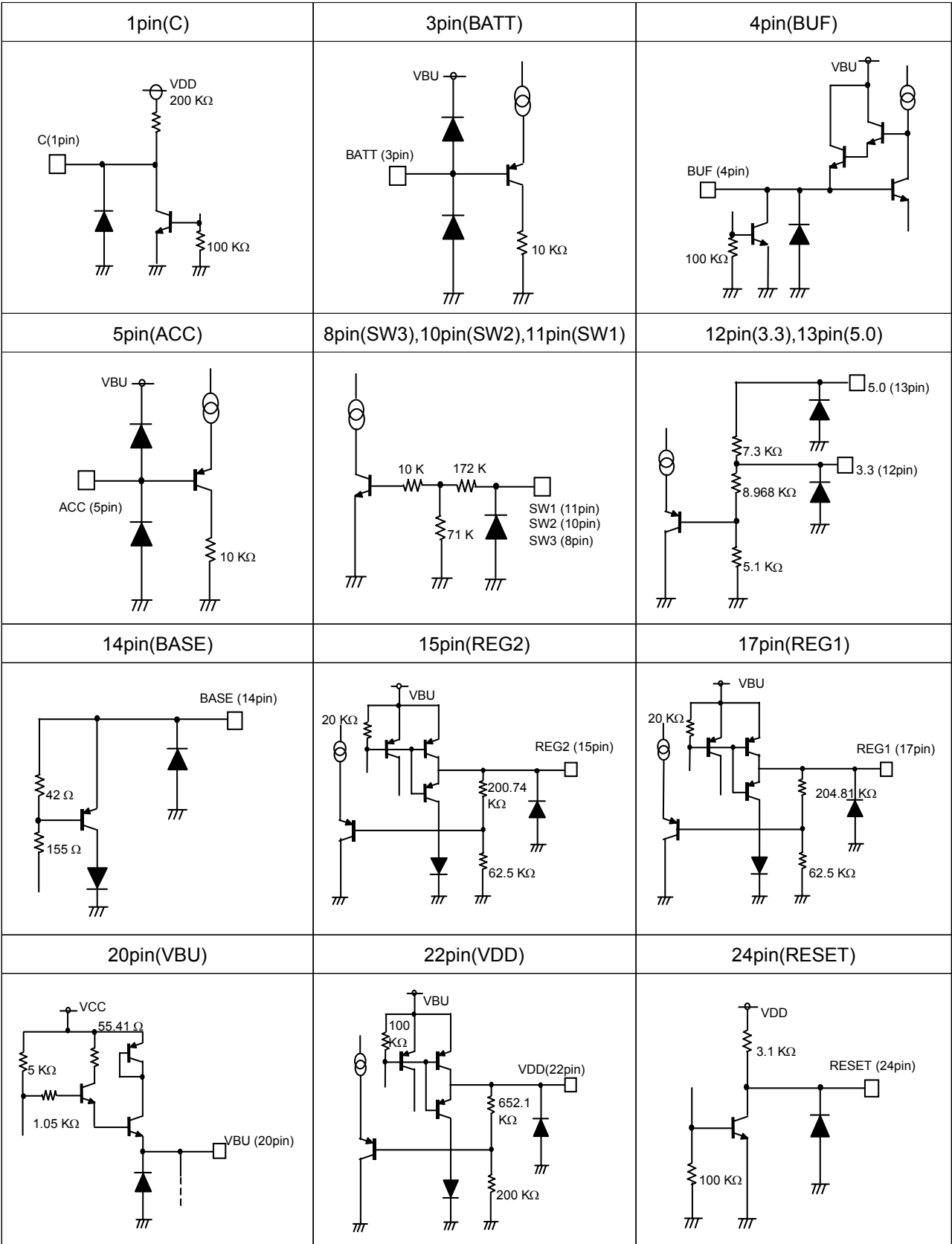


Fig.32

●Thermal design

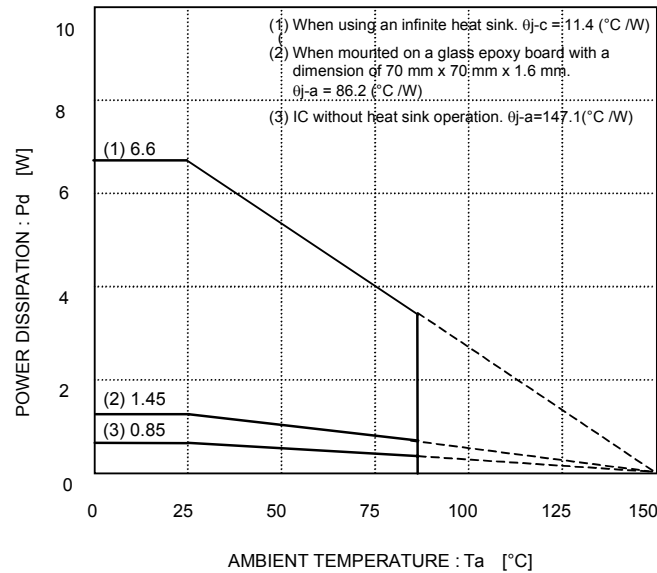


Fig. 33 Power Dissipation Characteristics

Refer to the power dissipation characteristics illustrated in Fig. 33 when using the IC in an environment where $T_a \geq 25^\circ\text{C}$. The characteristics of the IC are greatly influenced by the operating temperature. If the temperature is in excess of the maximum junction temperature $T_{j\text{max}}$, the elements of the IC may be deteriorated or damaged. It is necessary to give sufficient consideration to the heat of the IC in view of two points; First, the protection of the IC from instantaneous damage and second, the maintenance of the reliability of the IC in long-time operation.

In order to protect the IC from thermal destruction, it is necessary to operate the IC below the maximum junction temperature $T_{j\text{max}}$. The chip's (junction area) temperature T_j may rise considerably even when the IC is being used at room temperature (25°C). Always operate the IC within the power dissipation P_d .

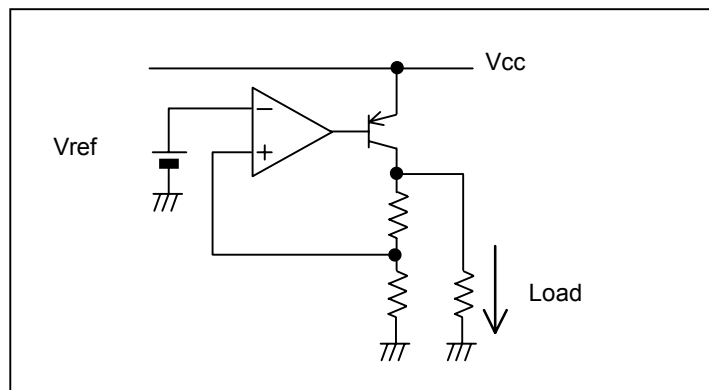


Fig.34

The maximum power consumption P_{MAX} (W) can be calculated as described below, where A denotes the maximum VCC input voltage:

I_1 = Max. VDD output current

I_2 = Max. REG1 output current

I_3 = Max. REG2 output current

I_4 = Max. REG3 output current

H_{fe} = Current amplification factor for external transistor

• Power consumed by VDD

$$P_1 = (A - 5.0 \text{ V}) \times I_1 + (I_1/60 + I_1/10) \times A$$

• Power consumed by REG1

$$P_2 = (A - 5.0 \text{ V}) \times I_2 + (I_2/30 + I_2/10) \times A$$

• Power consumed by REG2

$$P_3 = (A - 5.0 \text{ V}) \times I_3 + (I_3/30 + I_3/10) \times A$$

• Power consumed by REG3

$$P_4 = I_4/H_{fe} \times A$$

• Power consumed by each circuit's current

$$P_5 = V_{CC} \times \text{Circuit current (circuit current is approximately 1.5 mA)}$$

$$P_{\text{MAX}} = P_1 + P_2 + P_3 + P_4 + P_5$$

● Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

3. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (P_d) in actual operating conditions.

4. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7. Regarding input pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated.

P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When $GND > \text{Pin A}$ and $GND > \text{Pin B}$, the P-N junction operates as a parasitic diode.

When $GND > \text{Pin B}$, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

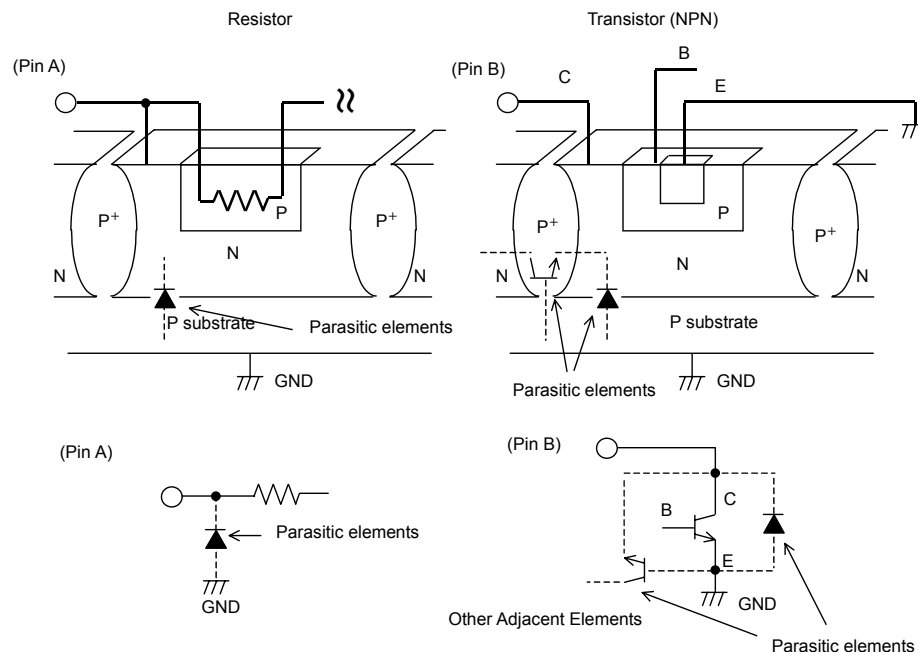


Fig.35 Example of a Simple Monolithic IC Architecture

8. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

9. Recommended operating ranges

Proper circuit functionality is guaranteed within the operating temperature range for supply voltages that fall within the recommended ranges. Although standard electrical characteristics values are not guaranteed, characteristics values will not vary suddenly within these ranges.

10. Capacitors for stopping oscillation for output pins

Capacitors for stopping oscillation must be placed between each output pin and the GND pin.

Use a ceramic capacitor (1 μF) connected with a resistor (1 Ω) in series, and connect them in parallel to an electrolytic capacitor (2.2 μF).

• Recommended

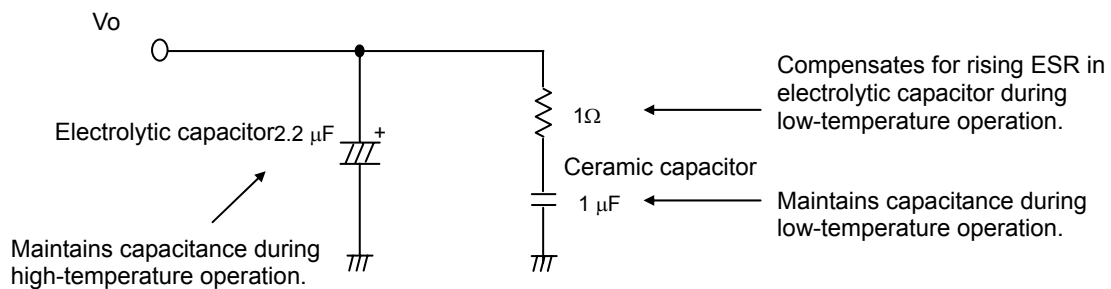


Fig.36

11. Applications or inspection processes with modes where the potentials of the VCC or VBU pin and other pins may be reversed from their normal states may cause damage to the IC's internal circuitry or elements. For example, such damage might occur when VCC is shorted with the GND pin while an external capacitor is charged. It is recommended to insert a diode to prevent back current flow in series with VCC, or bypass diodes between VCC and each pin. If the VCC/VBU pin carries a lower voltage than the GND pin, insert a protective diode between the VCC/VBU and GND pins.

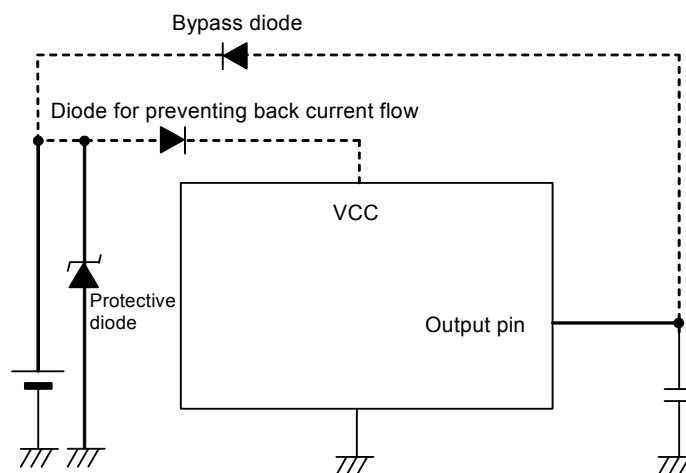


Fig. 37 Example of Bypass Diode Insertion to Prevent Back Current Flow

12. Overcurrent protection circuits

The IC incorporates built-in overcurrent protection circuits for the VDD, REG1, REG2, and REG3 output pins. Each circuit is specifically designed for the current capacity of the corresponding pin and acts to prevent damage to the IC when an overcurrent flows.

The protection circuits use dropping fold-back type current limiting and are designed to limit current flow by not latching up in the event of a large and instantaneous current flow originating from a large capacitor or other component. Their design allows for sufficient safety margins. When designing the application, keep in mind that when the output voltage falls to 1 V_F or lower, output is treated as short mode, and the output current is subject to greater limitation.

13. Overvoltage protection circuit

Overvoltage protection is designed to turn off all output voltages when the voltage differential between the VIN and GND pins exceeds approximately 33 V (at room temperature). Use caution when determining the power supply voltage range to use.

14. Thermal shutdown circuit (TSD)

This IC incorporates a built-in thermal shutdown circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's temperature T_j will trigger the thermal shutdown circuit to turn off all output power elements. The circuit will automatically reset once the chip's temperature T_j drops. Operation of the thermal shutdown circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the circuit.

15. Bypass capacitor between the VCC and GND pins

It is recommended to insert a bypass capacitor from 0.47 μ F to 10 mF between the VCC and GND pins, positioning it as close as possible to the pins.

16. Applications with modes where the potentials of the input pins (VCC) and GND pins and other output pins may be reversed from their normal states may cause damage to the IC's internal circuitry. In particular, it is recommended to create a bypass route with diodes or other components when loads including large inductance components are connected where BEMF may be generated during startup or when output is turned off.

Example:

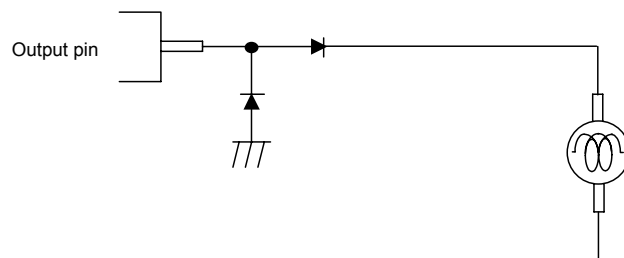


Fig. 38 Example of Protective Diode Insertion

17. REG3 emitter external power supply

The external power supply for the REG3 emitter should use a voltage at least 2 V higher than the REG3 output voltage, but not exceeding the rated voltage.

●Power dissipation reduction

B A 4 9 0 7

ROHM model name

F P

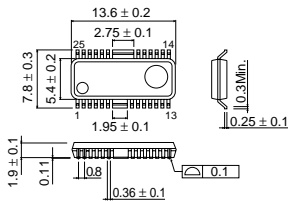
Package type

— E 2

Taping type

HSOP25

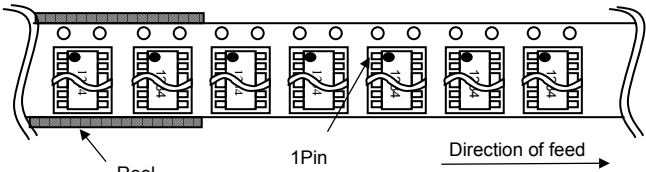
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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