STRUCTURE	Silicon Monolithic Integrated Circuit
PRODUCT SERIES	BTL driver for CD/CD-ROM
TYPE	BA 5 9 8 3 FP
PACKAGE OUTLINES	Figure 1 (Plastic Mold)
POWER DISSIPATION	Figure 2
BLOCK DIAGRAM	Figure 3
APPLICATION	Figure 4
TEST CIRCUIT	Figure 5

FUNCTIONS

- 4ch BTL Driver.
- Small surface mounting power package (HSOP 28) .
- Wide dynamic range. (4V(typ.) at PreVcc=12V,PowVcc=5V,RL=8Ω)
- Thermal shut down circuit built in.
- Separating Vcc into Pre and Power (Power divides into CH1/2 and CH3/4) , can make better power efficiency, by low supply voltage drive.
- Mute operated individually CH4 and CH1/2/3.
- All channels mute is stand by mode.
- Suitable for low operation voltage DSP by wide D-range pre opamp.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limits	Unit
Supply voltage	PreVcc,PowVcc	13.5	V
Power dissipation	Pd	1.7 #1	W
Max output current	I_{OMAX}	1 #2	A
Operating temperature	Topr	-35~ 85	℃
Storage temperature	Tstg	-55~ 150	℃

#1 On less than 3% (percentage occupied by copper foil) , 70× 70mm² ,t=1.6mm, glass epoxy mounting. Reduce power by 13.6mW for each degree above 25℃ .
#2 The output current must not exceed the maximum Pd and ASO.

GUARANTEED OPERATING RANGES

Parameter	Symbol	Limits	Unit
Vcc for pre block	PreVcc	4.5~ 13.2	V
Vcc for power block	PowVcc	4.5~ PreVcc	V

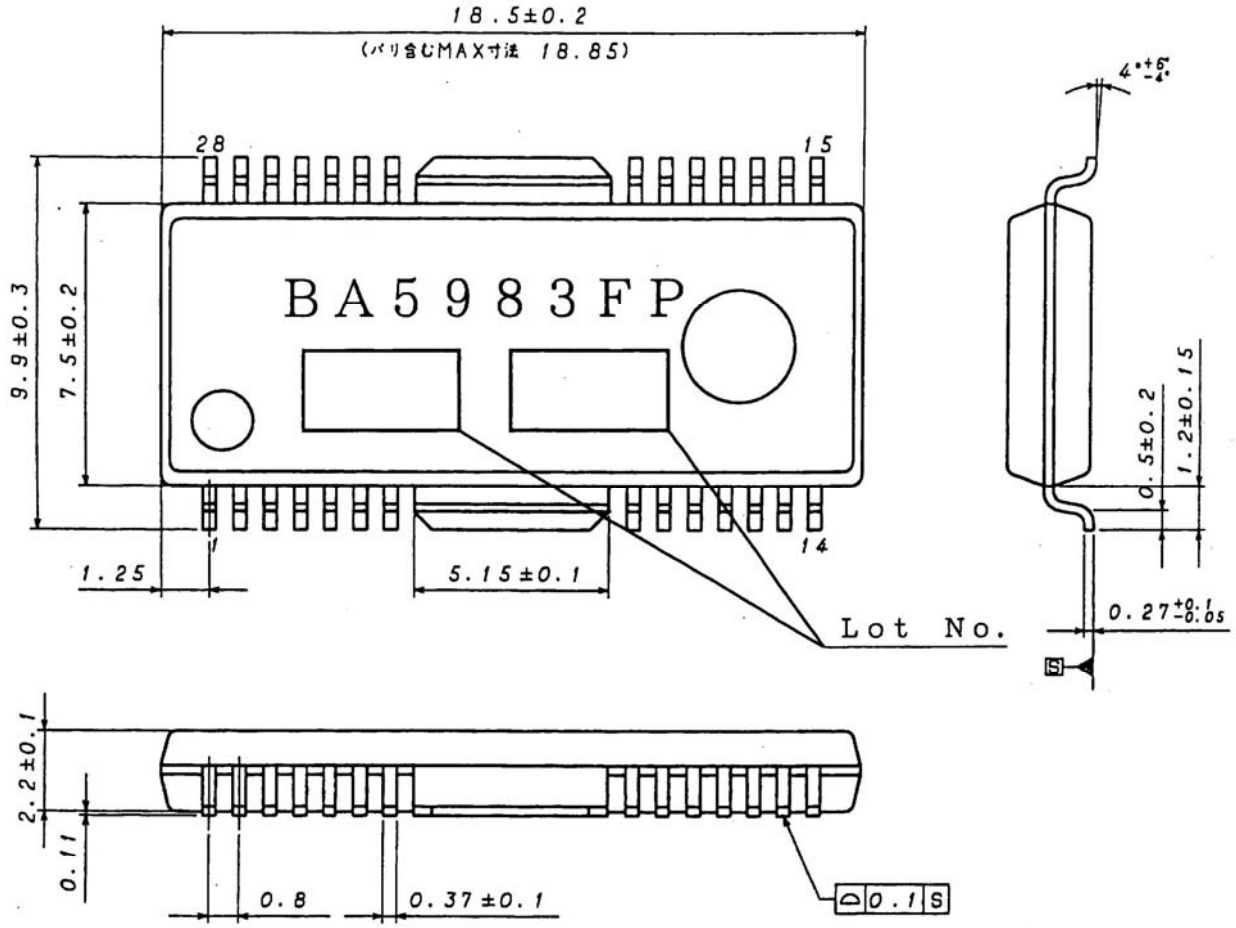
ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, Ta=25℃, PreVcc=8V,PowVcc1=5V,PowVcc2=8V,V_{BIAS} =1.65V,RL=8Ω)

Parameter	Symbol	Min.	Typ.	Max.	UNIT	Conditions	Test circuit
Quiescent current	IQ	—	20	32	mA	R_L=∞	Fig.5
CH1-3 Standby Current	I_{QST1}	—	6.2	13	mA	R_L=∞	Fig.5
CH4 Standby Current	I_{QST2}	—	16	26	mA	R_L=∞	Fig.5
All Channel Standby Current	I_{QST3}	—	—	1	mA	R_L=∞	Fig.5
<Driver block>							
Output offset voltage	V_{OOF}	-70	—	70	mV		Fig.5
Maximum output voltage 1	V_{OM1}	3.6	4.0	—	V	CH1,2 VIN=V_{BIAS} ± 1.65V	Fig.5
Maximum output voltage 2	V_{OM2}	5.4	6.0	—	V	CH3,4 VIN=V_{BIAS} ± 1.65V	Fig.5
Closed loop voltage gain 1	G_{VC1}	10	12	14	dB	CH1,2 VIN=V_{BIAS} ± 0.5V	Fig.5
Closed loop voltage gain 2	G_{VC2}	16	18	20	dB	CH3,4 VIN=V_{BIAS} ± 0.5V	Fig.5
Slew Rate	SR_{DRV}	—	2	—	V	Input pulse 100kHz,2Vp-p	Fig.5
Standby on voltage	VST_{ON}	—	—	0.5	V		Fig.5
Standby off voltage	VST_{OFF}	2.0	—	—	V		Fig.5
Bias drop mute on voltage	VBM_{DN}	—	—	0.7	V		Fig.5
Bias drop mute off voltage	VBM_{DFF}	1.3	—	—	V		Fig.5
<Pre operational amplifier>							
Common mode input range	V_{ICM}	0	—	6.8	V		Fig.5
Input offset voltage	V_{OFOP}	-6	0	6	mV		Fig.5
Input bias current	I_{BOP}	—	—	300	nA		Fig.5
High level output voltage	V_{OHOP}	7	7.8	—	V	V_{BIAS} =4V	Fig.5
Low level output voltage	V_{OLOP}	—	—	0.3	V	V_{BIAS} =4V	Fig.5
Output sink current	I_{SI}	1	—	—	mA	output to PreVcc by 50Ω, V_{BIAS} =4V	Fig.5
Output source current	I_{SO}	300	500	—	μA	output to GND by 50Ω, V_{BIAS} =4V	Fig.5
Slew rate	SROP	—	2	—	V/μs	Input pulse 100kHz,2Vp-p	Fig.5

○ This product is not designed for protection against radioactive rays.

PACKAGE OUTLINES (mm)

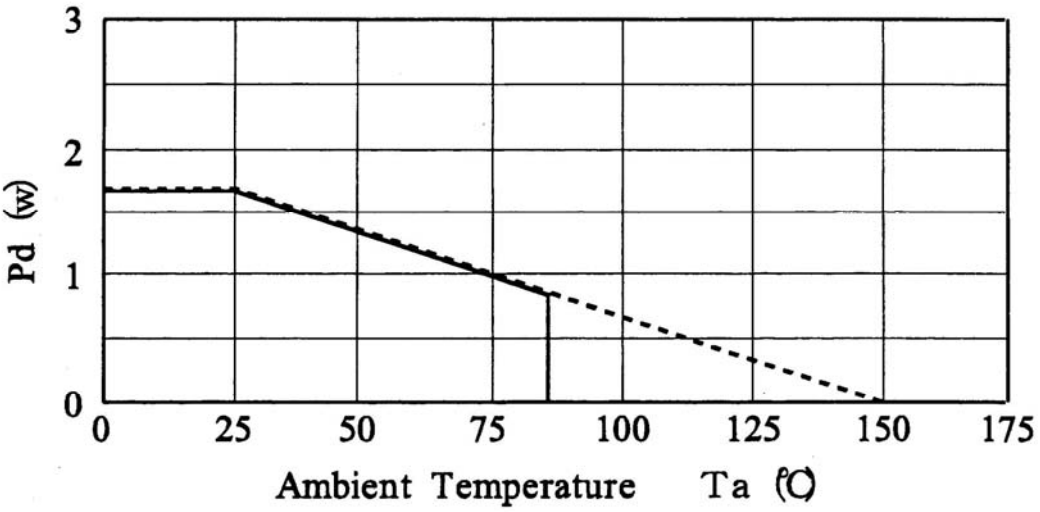


(UNIT: mm)

図番: EX140-5001-1

Figure 1

POWER DISSIPATION / Electrical characteristic curves

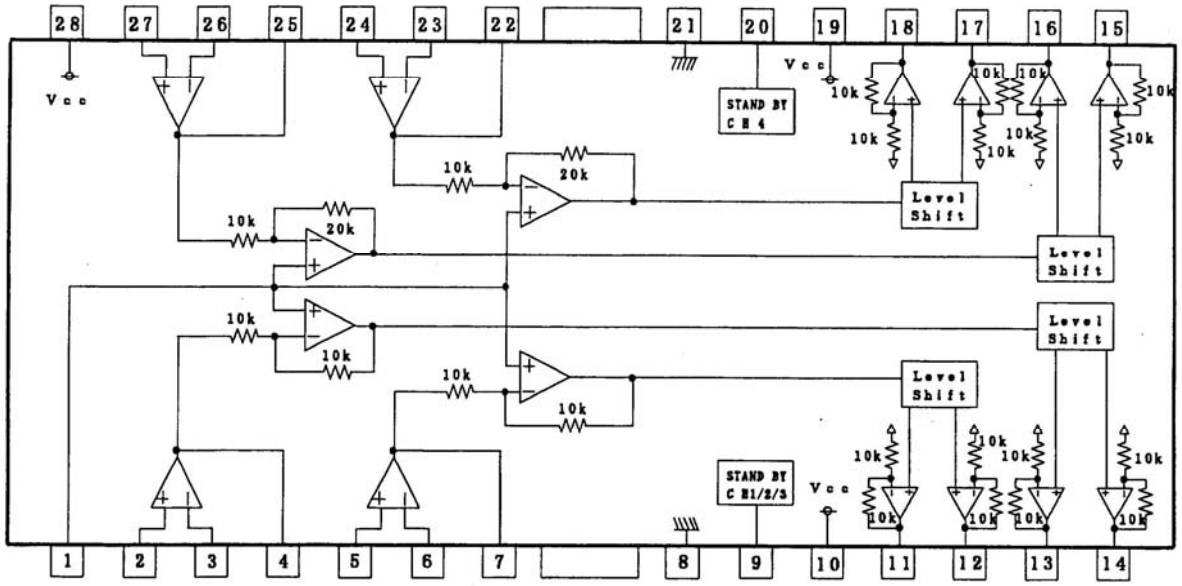


Pd : power dissipation

* On less than 3% (percentage occupied by copper foil) , 70× 70mm² ,t=1.6mm glass epoxy mounting.

Figure 2

BLOCK DIAGRAM



resistor unit : Ω

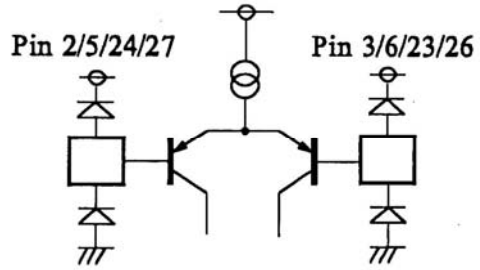
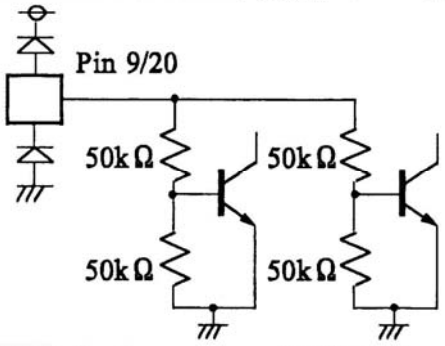
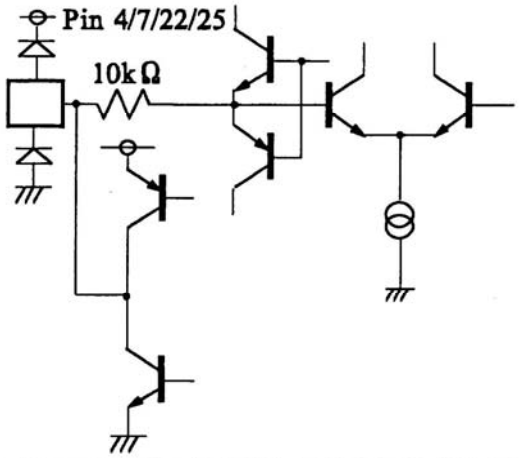
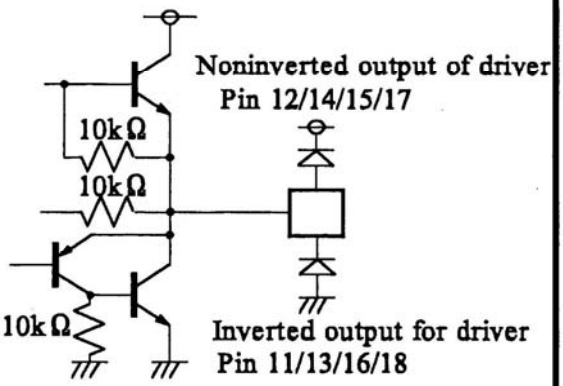
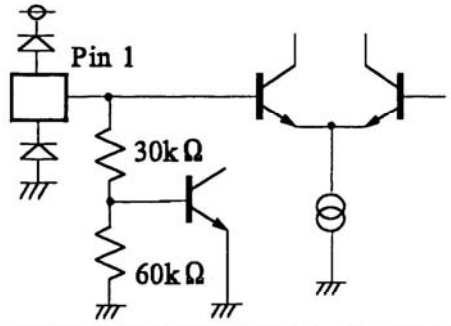
Figure 3

Pin description

NO	Symbol	Function	NO	Symbol	Function
1	BIAS IN	Input for Bias-amplifier	15	VO4(+)	Non inverted output of CH4
2	OPIN1(+)	Non inverting input for CH1 OP-AMP	16	VO4(-)	Inverted output of CH4
3	OPIN1(-)	Inverting input for CH1 OP-AMP	17	VO3(+)	Non inverted output of CH3
4	OPOUT1	Output for CH1 OP-AMP	18	VO3(-)	Inverted output of CH3
5	OPIN2(+)	Non inverting input for CH2 OP-AMP	19	PowVcc2	Vcc for CH3/4 power block
6	OPIN2(-)	Inverting input for CH2 OP-AMP	20	STBY2	Input for CH4 stand by control
7	OPOUT2	output for CH2 OP-AMP	21	GND	Substrate ground
8	GND	Substrate ground	22	OPOUT3	Output for CH3 OP-AMP
9	STBY1	Input for CH1/2/3 stand by control	23	OPIN3(-)	Inverting input for CH3 OP-AMP
10	PowVcc1	Vcc for CH1/2 power block	24	OPIN3(+)	Non inverting input for CH3 OP-AMP
11	VO2(-)	Inverted output of CH2	25	OPOUT4	Output for CH4 OP-AMP
12	VO2(+)	Non inverted output of CH2	26	OPIN4(-)	Inverting input for CH4 OP-AMP
13	VO1(-)	Inverted output of CH1	27	OPIN4(+)	Non inverting input for CH4 OP-AMP
14	VO1(+)	Non inverted output of CH1	28	PreVcc	Vcc for pre block

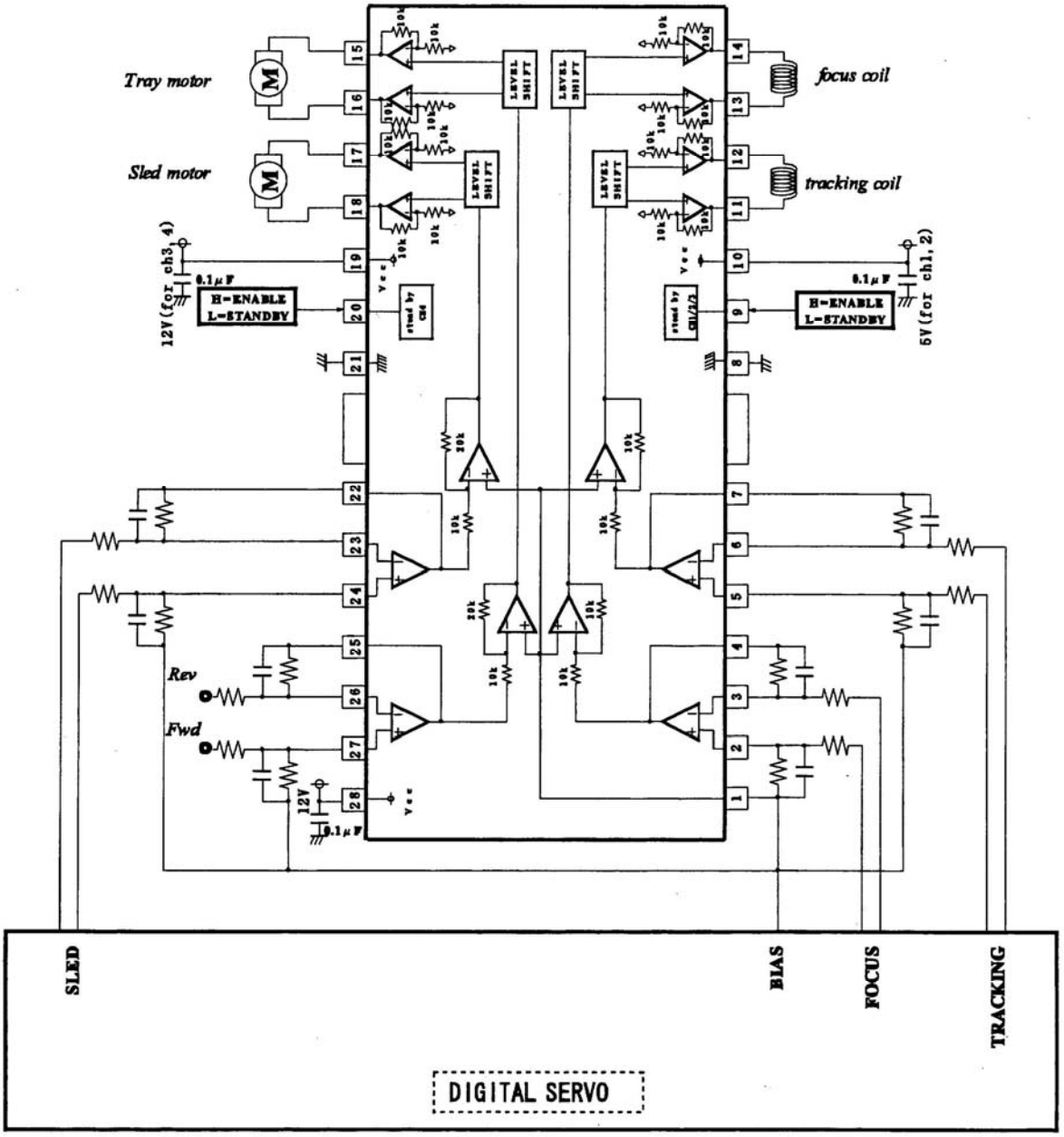
notes) Symbol of + and - (output of drivers) means polarity to input pin.
(For example if voltage of pin4 high,pin14 is high.)

EQUIVALENT CIRCUIT OF TERMINALS

Input for Operational amplifier	Input for stand by control
	
Output of OP - amp & input for driver	**Output of driver**
	
Input for bias amplifier	
	

resistor unit : Ω

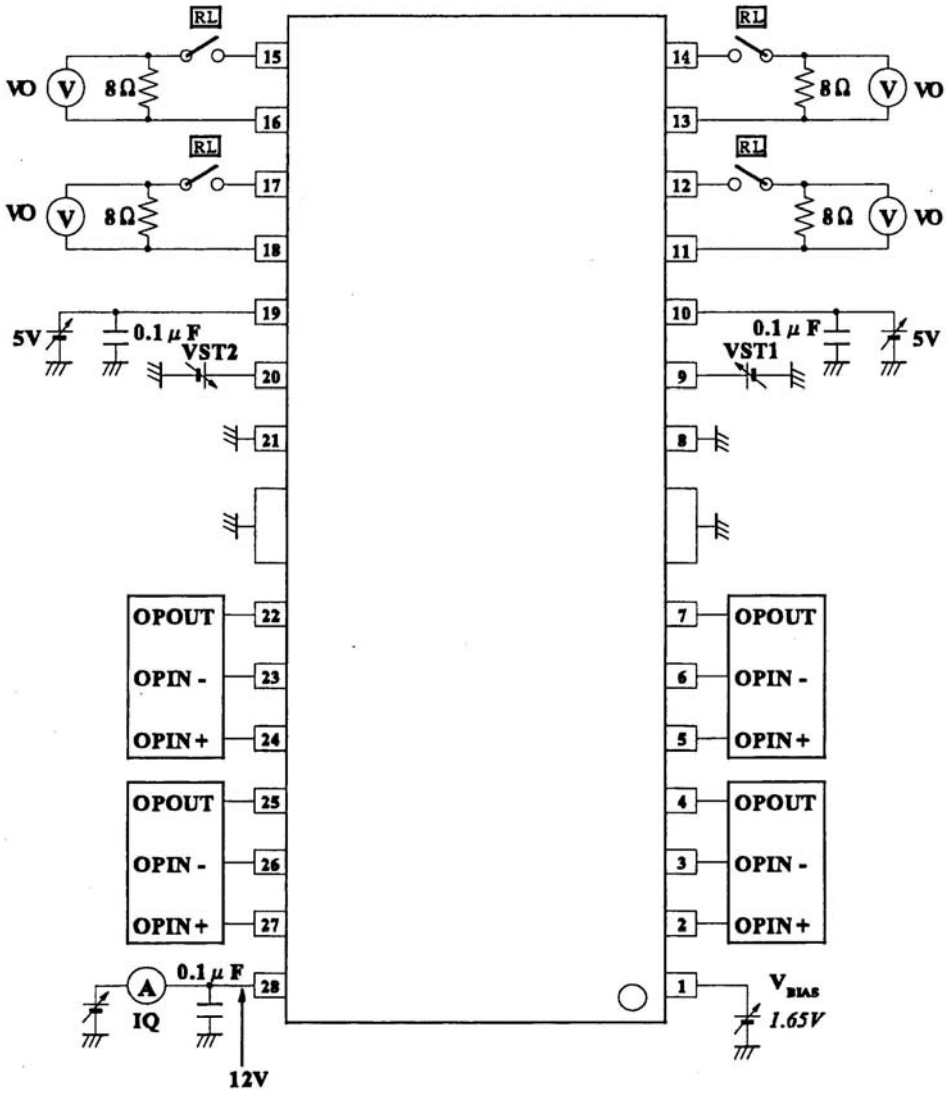
Application circuit

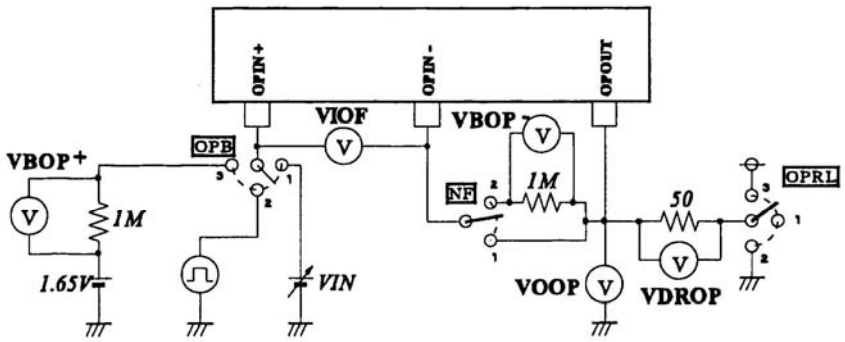


resistor unit : Ω

Figure 4

TEST CIRCUIT





resistor unit : Ω

Figure 5

Table of measuring circuit switches

1) Quiescent current or standby (VIN=V_{BIAS}=1.65V, OPB→ 1, RL→ OFF, NF→ 1, OPRL→ 1)

Symbol	Input		Conditions	Measuring point
	VST1	VST2		
IQ	5V	5V		IQ
IQST1	0V	5V		IQ
IQST2	5V	0V		IQ
IQST3	0V	0V		IQ

2) Driver block (OPB→ 1,NF→ 1,OPRL→ 1, RL→ ON)

Symbol	SW	Input				Condition	Measuring point
	OPB	VIN	VST1	VST2	V_{BIAS}		
VOO1	1	1.65V	2.0V	2.0V	1.65V		VO (CH1,2)
VOO2	1	1.65V	2.0V	2.0V	1.65V		VO (CH3,4)
VOM1	1	± 1.65V	2.0V	2.0V	1.65V	VIN=0V or 3.3V	VO (CH1,2)
VOM2	1	± 1.65V	2.0V	2.0V	1.65V	VIN=0V or 3.3V	VO (CH3,4)
GVC1	1	± 0.5V	2.0V	2.0V	1.65V	VIN=1.15V or 2.15V	VO (CH1,2)
GVC2	1	± 0.5V	2.0V	2.0V	1.65V	VIN=1.15V or 2.15V	VO (CH3,4)
VSTON	1	3.0V	0.5V	0.5V	1.65V	Check output of driver is muted.	VO
VSTOFF	1	3.0V	2.0V	2.0V	1.65V	Check output of driver is active.	VO
VBMON	1	3.0V	0.5V	0.5V	0.5V	Check output of driver is muted.	VO
VBMOFF	1	3.0V	2.0V	2.0V	1.3V	Check output of driver is active.	VO
SR_{DRV}	2	± 1V	2.0V	2.0V	1.65V	Input pulse 100kHz, *$2V_{P-P}$	VO

3) Pre operational amplifier (VST1=VST2=2V,RL→ OFF)

Symbol	Switch			Input		Conditions	Measuring point
	OPB	NF	OPRL	VIN	V_{BIAS}		
VOFOP	1	1	1	1.65V	1.65V		VIOF
VBOP	3	2	1	1.65V	1.65V		VBOP/1MΩ
VOHOP	1	1	1	12V	6V	V_{BIAS}=VCC/2	VOOP
VOLOP	1	1	1	0V	6V	V_{BIAS}=VCC/2	VOOP
ISI	1	1	3	6V	6V	V_{BIAS}=VCC/2	VDROP/50Ω
ISO	1	1	2	6V	6V	V_{BIAS}=VCC/2	VDROP/50Ω
SROP	2	1	1	± 1.0V*	1.65V	Input pulse 100kHz, *$2V_{P-P}$	VOOP

. **Notes on use**

1. Thermal shut down circuit is built in. In case IC chip temperature rises to 175℃(typ) , thermal shut down circuit operates and muted the output current. Next time IC chip temperature falls below 150℃(typ) , the driver blocks start.

2. Bias pin (pin1) should be pulled up more than 1.3V. In case bias pin voltage is under 0.7V(typ.) , output current is muted.

3. In case supply voltage falls below 3.8V(typ.) , output current is muted. Next time supply voltage rises to 4.0V (typ.), the driver blocks start.

4. Mute operation is caused by thermal shut down, decrease of bias pin voltage or decrease of supply voltage. when mute is done, output voltage becomes internal reference voltage(about PowVcc/2 .

5. In case of one of the standby terminals turn into or open , correspondence channel circuit(include opamp) is muted.

6. Both of the standby terminals low or open, all circuits shutdown(sleep mode) and all output pins become high impedance.
In addition to threshold is 1.4V(typ.) .

7. Supply voltage of PreVcc should be equal to or higher than PowVcc.

8. Take care the external resister value of OPamp .
OPamp source current supplies to internal resister (10K Ω) as well as external resister.

9. Insert the by pass capacitor between Vcc pin and GND pin of IC as near as possible (approximately 0.1μ F) .

10. Keep the GND pin voltage the lowest of all pins .

11. Heat dissipation fins are attached to the GND on the inside of the package. Make sure to connect these to the external GND.

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