STRUCTURE Silicon Monolithic Integrated Circuit

NAME OF PRODUCT DC-AC Inverter Control IC

TYPE **ＢＤ９７６６ＦＶ**

FUNCTION
- 2ch control with Half-bridge
- Lamp current and voltage sense feed back control
- Sequencing easily achieved with Soft Start Control
- Short circuit protection with Timer Latch
- Under Voltage Lock Out
- Short circuit protection with over voltage
- Mode-selectable the operating or stand-by mode by stand-by pin
- Control PWM and BURST mode by DUTY pin
- BURST mode with 2ch Reverse phase

○Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage	V_{CC}	12	V
Operating Temperature Range	Topr	-35～+85	℃
Storage Temperature Range	Tstg	-55～+125	℃
Power Dissipation	Pd	850*	mW
Maximum Junction Temperature	Tjmax	+125	℃

*Pd derated at 8.5mW/℃ for temperature above Ta = 25℃ (When mounted on a PCB 70.0mm×70.0mm×1.6mm)

○Recommended operating condition

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	5.0～11.0	V
CT oscillation frequency	f_{CT}	35～200	kHz
BCT oscillation frequency	f_{BCT}	0.10～0.50	kHz

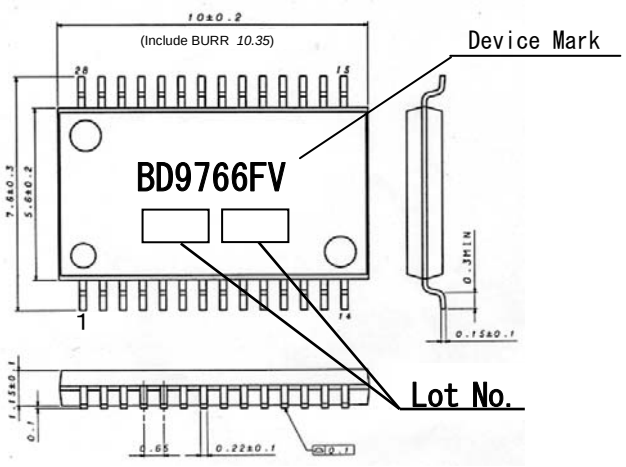
Status of this document
The Japanese version of this document is the official specification.
Please use the translation version of this document as a reference to expedite understanding of the official version.
If these is any uncertainty in translation version of this document, official version takes priority.

○Electric Characteristics (Ta=25℃, VCC=7V)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
((WHOLE DEVICE))						
Operating current	Icc1	—	9.0	17.0	mA	CT=0.5V
Stand-by current	Icc2	—	4	8	uA	
((OVER VOLTAGE DETECT))						
FB over voltage detect voltage	Vovf	2.70	3.00	3.30	V	
((OUTPUT BLOCK))						
Pch output voltage H	VoutPH	VCC-0.3	VCC-0.1	—	V	
Nch output voltage H	VoutNH	VCC-0.3	VCC-0.1	—	V	
Pch output voltage L	VoutPL	—	0.1	0.3	V	
Nch output voltage L	VoutNL	—	0.1	0.3	V	
Pch output sink resistance	RsinkP	—	8	16	Ω	
Pch output source resistance	RsourceP	—	10	20	Ω	
Nch output sink resistance	RsinkN	—	8	16	Ω	
Nch output source resistance	RsourceN	—	10	20	Ω	
((STAND-BY CONTROL))						
Stand-by voltage H	VstH	2.0	—	—	V	System ＯＮ
Stand-by voltage L	VstL	—	—	0.8	V	System ＯＦＦ
Hysteresis width	⊿Vst	0.05	0.15	0.25	V	
((TIMER LATCH))						
Timer Latch voltage	Vcp	1.5	1.9	2.3	V	
Timer Latch current	Icp	1.0	2.0	3.0	uA	
((OSC BLOCK))						
Active edge current	Iact	1.2/RT	1.5/RT	1.8/RT	A	
Negative edge current	Ineg	1.2/RDIS	1.5/RDIS	1.8/RDIS	A	
OSC Max voltage	VoscH	1.8	2.0	2.2	V	fact=10kHz
OSC Min voltage	VoscL	0.3	0.5	0.7	V	fneg=100kHz
Soft start current	Iss	1.0	2.0	3.0	uA	
IS COMP detect Voltage	VISC	—	0.6	—	V	
SS COMP detect voltage	Vss	—	2.2	—	V	
SRT ON resistance	RSRT	—	200	400	Ω	
((UVLO BLOCK))						
Operating voltage	VuvloH	4.25	4.50	4.75	V	
Shut down voltage	VuvloL	4.0	4.25	4.50	V	
((FEED BACK BLOCK))						
IS threshold voltage	Vis	1.220	1.250	1.280	V	
VS threshold voltage	Vvs	1.220	1.250	1.280	V	
IS source current 1	Iis1	—	—	1.5	uA	DUTY=2.0V
IS source current 2	Iis2	13.0	20.0	27.0	uA	DUTY=0V、IS=0.5V
VS source current	Ivs	—	—	0.9	uA	
((BURST MODE))						
BOSC Max voltage	VburH	1.8	2.0	2.2	V	f_{BCT}=0.3kHz
BOSC Min Voltage	VburL	0.3	0.5	0.7	V	f_{BCT}=0.3kHz
BOSC constant current	I_{burosc}	1.2/BRT	1.5/BRT	1.8/BRT	A	
((REG BLOCK))						
REG output voltage	VREG	3.038	3.100	3.162	V	
REG source current	IREG	5.0	—	—	mA	
((COMP BLOCK))						
Over voltage detect	VCOMPH	2.20	2.5	2.80	V	
Under voltage detect	VCOMPL	0.590	0.640	0.690	V	
((PROTECT CLOCK))						
Normal output voltage	VPH	2.9	3.1	3.3	V	
Protect output voltage	VPL	—	—	0.5	V	

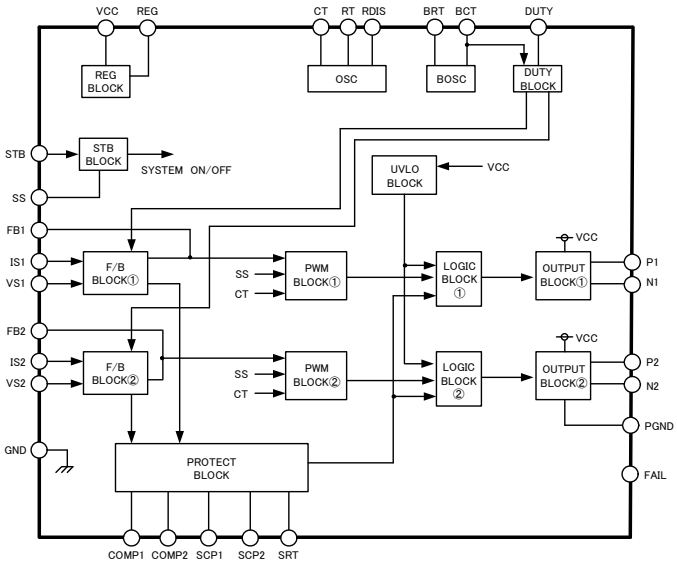
(This product is not designed for normal operation with in a radio active environment.)

○Package Dimensions



SSOP-B28 (Unit:mm)

○Block Diagram



○Pin Description

Pin No.	Pin Name	Function
1	DUTY	Control PWM mode and BURST mode
2	BRT	External resistor from BRT to GND for adjusting the BURST triangle oscillator
3	BCT	External capacitor from BCT to GND for adjusting the BURST triangle oscillator
4	RDIS	External resistor from RDIS to GND for adjusting the triangle oscillator
5	RT	External resistor from SRT to RT for adjusting the triangle oscillator
6	SRT	External resistor from SRT to RT for adjusting the triangle oscillator
7	CT	External capacitor from CT to GND for adjusting the triangle oscillator
8	GND	GROUND
9	FB1	Error amplifier output①
10	IS1	Error amplifier input①
11	VS1	Error amplifier input②
12	FB2	Error amplifier output②
13	IS2	Error amplifier input③
14	VS2	Error amplifier input④
15	FAIL	Protect clock output
16	STB	Stand-by switch
17	COMP1	Under, over voltage detect for 1ch
18	COMP2	Under, over voltage detect for 1ch
19	REG	Internal regulator output
20	SS	External capacitor from SS to GND for Soft Start Control
21	SCP1	External capacitor from SCP1 to GND for Timer Latch for 1ch
22	SCP2	External capacitor from SCP2 to GND for Timer Latch for 2ch
23	P2	FET driver for 2ch
24	N2	FET driver for 2ch
25	PGND	Ground for FET drivers
26	N1	FET driver for 1ch
27	P1	FET driver for 1ch
28	Vcc	Supply voltage input

○NOTE FOR USE

1. When designing the external circuit, including adequate margins for variation between external devices and the IC.Use adequate margins for steady state and transient characteristics.
2. Recommended Operating Range

   The circuit functionality is guaranteed within of ambient temperature operation range as long as it is within recommended operating range. The standard electrical characteristic values cannot be guaranteed at other voltages in the operating ranges, however, the variation will be small.
3. Mounting Failures

   Mounting failures, such as misdirection or miscounts, may harm the device.
4. Electromagnetic Fields

   A strong electromagnetic field may cause the IC to malfunction.
5. The GND pin should be the location within ±0.3V compared with the PGND pin
6. BD9766FV has the short circuit protection with Thermal Shut Down System. When STB or Vcc pin re-supplied, They enables to cancel the latch. If It rise the temperature of the chip more than 170℃(TYP), It make the external FET OFF
7. Absolute maximum ratings are those values that, if exceeded, may cause the life of a device to become significantly shortened. Moreover, the exact failure mode caused by short or open is not defined. Physical countermeasures, such as a fuse, need to be considered when using a device beyond its maximum ratings.
8. About the external FET, the parasitic Capacitor may cause the gate voltage to change, when the drain voltage is switching. Make sure to leave adequate margin for this IC variation.
9. On operating Slow Start Control (SS is less than 2.2V), It does not operate Timer Latch.
10. By STB voltage, BD9886FV is changed to 2 states. Therefore, do not input STB pin voltage between one state and the other state (0.8～2.0V).
11. The pin connected a connector need to connect to the resistor for electrical surge destruction.
12. This IC is a monolithic IC which (as shown is Fig-1)has P^+ substrate and between the various pins. A P-N junction is formed from this P layer of each pin. For example, the relation between each potential is as follows,

    ○(When GND > PinB and GND > PinA, the P-N junction operates as a parasitic diode.)

    ○(When PinB > GND > PinA, the P-N junction operates as a parasitic transistor.)

Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage. Accordingly you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate)voltage to an input pin.

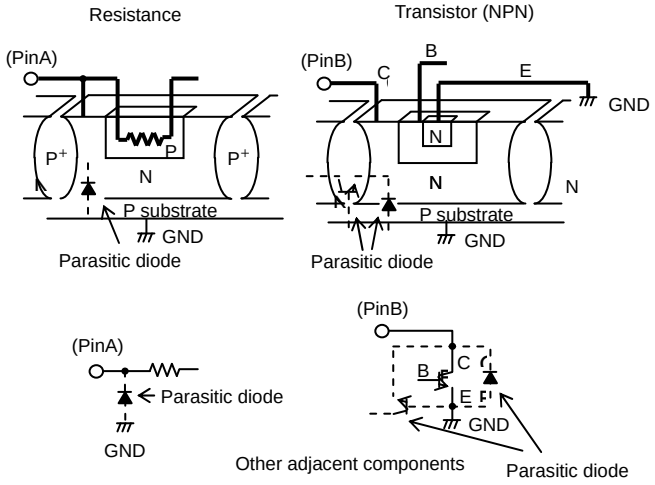


図-1 Simplified structure of a Bipolar IC

Notes

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