High-performance Regulator IC Series for PCs

Switching Regulators
for DDR-SDRAM Cores

BD9532EKN

●Description

BD9532EKN is a switching regulator controller with high output current which can achieve low output voltage (0.7V to 2.0V) from a wide input voltage range (4.5V to 25V). High efficiency for the switching regulator can be realized by utilizing an external N-MOSFET power transistor. A new technology called H^{3}Reg^{TM} is a Rohm proprietary control method to realize ultra high transient response against load change. SLLM^{TM} (Simple Light Load Mode) technology is also integrated to improve efficiency in light load mode, providing high efficiency over a wide load range. For protection and ease of use, the soft start function, variable frequency function, short circuit protection function with timer latch, and REF synchronous function are all built in. This switching regulator is specially designed for the DDR-SDRAM core.

●Features

1) H^{3}Reg^{TM} Switching Regulator Controller
2) Light Load Mode and Continuous Mode Changeable
3) Thermal Shut Down (TSD), Under Voltage LockOut (UVLO), Over Current Protection (OCP),
   Short Circuit Protection(SCP) built-in
4) Soft start function to minimize rush current during startup
5) Switching Frequency Variable (f=200KHz～600KHz)
6) HQFN20V Package

●Applications

Laptop PC, Desktop PC, LCD-TV, Digital Components

Sep. 2008

●Maximum Absolute Ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit
Input Voltage 1	VCC	7 *1*2	V
Input Voltage 2	VDD	7 *1*2	V
Input Voltage 3	VIN	30 *1*2	V
BOOT Voltage	BOOT	35 *1*2	V
BOOT-SW Voltage	BOOT-SW	7 *1*2	V
HG-SW Voltage	HG-SW	7 *1*2	V
LG Voltage	LG	VDD	V
REF Voltage	REF	VCC	V
Output Voltage	VOUT/Is+/Is-	VCC	V
ILIM/SCP/SS/FS/SLLM Voltage	ILIM/SCP/SS/FS/SLLM	VCC	V
VREG Voltage	VREG	VCC	V
EN Input Voltage	EN	7 *1	V
Power Dissipation 1	Pd1	0.5 *3	W
Power Dissipation 2	Pd2	0.75 *4	W
Power Dissipation 3	Pd3	1.75 *5	W
Power Dissipation 4	Pd4	2.00 *6	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.
*3 Reduced by 4mW for each increase in Ta of 1℃ over 25℃ (when not mounted on a heat radiation board)
*4 Reduced by 6mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB.)
*5 Reduced by 14mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB.)
*6 Reduced by 16mW for increase in Ta of 1℃ over 25℃. (when mounted on a board 70.0mm×70mm×1.6mm Glass-epoxy PCB.)

●Operating Conditions (Ta=25℃)

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	VCC	4.5	5.5	V
Input Voltage 2	VDD	4.5	5.5	V
Input Voltage 3	VIN	4.5	25	V
BOOT Voltage	BOOT	4.5	30	V
SW Voltage	SW	-0.7	25	V
BOOT-SW Voltage	BOOT-SW	4.5	5.5	V
SLLM Input Voltage	SLLM	0	5.5	V
EN Input Voltage	EN	0	5.5	V
Output setting voltage	REF	0.7	2.0	V
Is Input Voltage	Is+/Is-	0.7	2.7	V
MIN ON Time	Tonmin	-	200	nsec

★ This product should not be used in a radioactive environment.

●ELECTRICAL CHARACTERISTICS

(unless otherwise noted, Ta=25°C VCC=5V,VDD=5V,EN/SLLM=5V,VIN=12V,REF=1.8V,RFS=68kΩ)

| Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
[Whole Device]						
VCC Bias Current	Icc	-	700	900	µA	
VIN Bias Current	Iin	-	100	200	µA	
VCC Standby Current	Iccstb	-	0	10	µA	EN=0V
VIN Standby Current	Iinstb	-	100	200	µA	EN=0V
EN Low Voltage	Enlow	GND	-	0.8	V	
EN HighVoltage	Enhigh	2.3	-	5.5	V	
EN Bias Current	Ien	-	7	10	µA	
VREG Voltage	Vreg	2.475	2.500	2.525	V	Ireg=100µA Ta=-10°C to 100°C*
[Under Voltage Locked Out]						
VCC threshold voltage	Vcc_UVLO	4.1	4.3	4.5	V	VCC:Sweep up
VCC hysteresis voltage	dVcc_UVLO	100	160	220	mV	Vcc:Sweep down
VIN threshold voltage	Vin_UVLO	4.1	4.3	4.5	V	VIN:Sweep up
VIN hysteresis voltage	dVin_UVLO	100	160	220	mV	VIN:Sweep down
VREG threshold voltage	Vreg_UVLO	2.0	2.2	2.4	V	VREG:Sweep up
VREG hysteresis voltage	dVreg_UVLO	100	160	220	mV	VREG:Sweep down
[H³Reg™ Controller]						
Frequency	Fosc	-	300	-	kHz	
ON Time	Ton	400	500	600	nsec	
MAX ON Time	Tonmax	-	3	-	µsec	
MIN OFF Time	Toffmin	-	450	550	nsec	
[FET Driver]						
HG Higher side ON resistor	HGhon	-	3.0	6.0	Ω	
HG Lower side ON resistor	HGlon	-	2.0	4.0	Ω	
LG Higher side ON resistor	LGhon	-	2.0	4.0	Ω	
LG Lower side ON resistor	LGlon	-	0.5	1.0	Ω	
[Dead Time]						
HG rising	Hgdead	-	50	-	nsec	
LG rising	LGdead	-	50	-	nsec	
[SCP]						
SCP Detect Voltage	Vscp	REF ×0.65	REF ×0.7	REF ×0.75	V	
SCP threshold voltage	Vscpth	1.2	1.25	1.3	V	
Charge current	Iscp	1.5	2	2.5	µA	
Standby voltage	Vscp_stb	-	-	50	mV	
[Soft start]						
Charge current	Iss	1.5	2	2.5	µA	
Standby voltage	Vss_stb	-	-	50	mV	
[Over Current Protection Block]						
Current limit threshold1	Ilim1	43	50	57	mV	ILIM=0.5V Ta=-10°C to 100°C*
Current limit threshold2	Ilim2	160	200	240	mV	ILIM=2.0V
Reverse-current limit threshold1	ReIlim1	-	-50	-	mV	
Reverse-current limit threshold2	ReIlim2	-	-200	-	mV	
ILIM bias current	IILIM	-	15	-	nA	
[VOUT setting]						
VOUT offset voltage	Voutoff	REF-7m	REF	REF+7m	V	Ta=-10°C to 100°C*
VOUT bias current	Ivout	-100	0	100	nA	
REF bias current	Iref	-100	0	100	nA	
Is+ Input current	IIs+	-1	0	1	µA	Is+=1.8V
Is- Input current	IIs-	-1	0	1	µA	Is-=1.8V
[SLLM]						
Continuous mode threshold	Vthcon	Vcc-0.5	-	Vcc	V	
SLLM threshold	VthSLLM	GND	-	0.5	V	

* Design Guarantee

●Reference Data
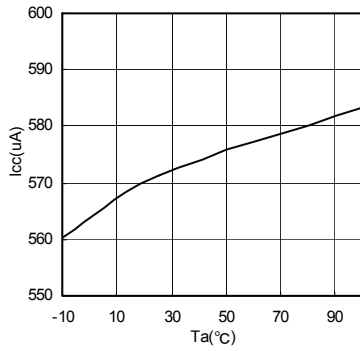
Fig.1 Ta vs Icc
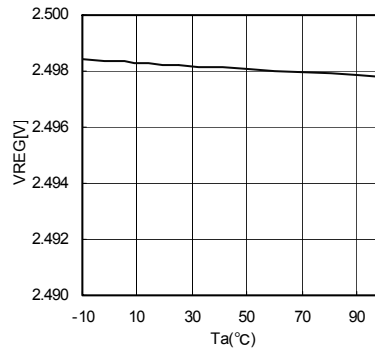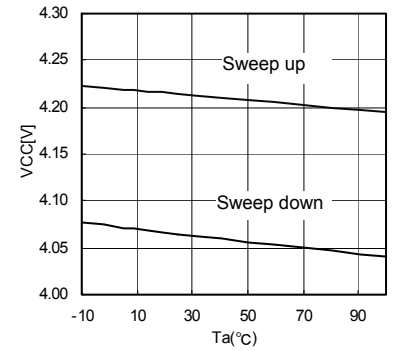

Fig.2 Ta vs VREG

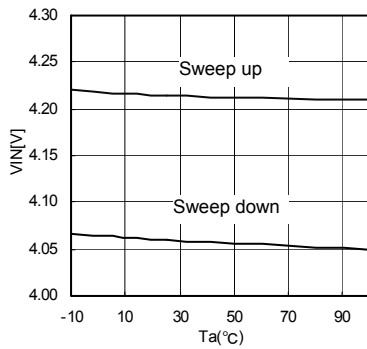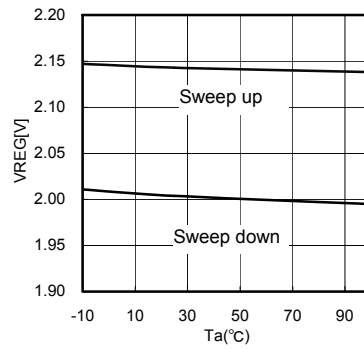Fig.3 Ta vs UVLO (Vcc)

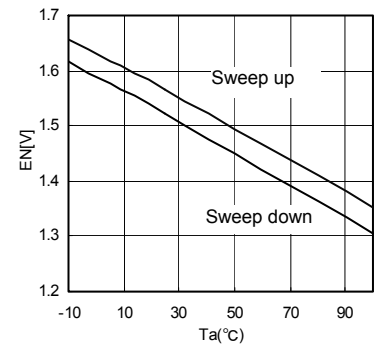Fig.4 Ta vs UVLO (VIN)

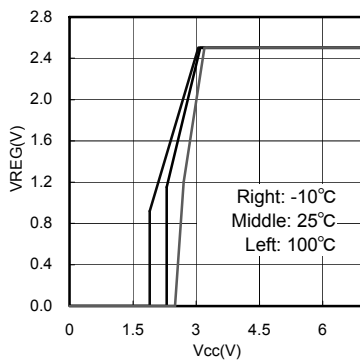Fig.5 Ta vs UVLO (VREG)

Fig.6 Ta vs EN Threshold
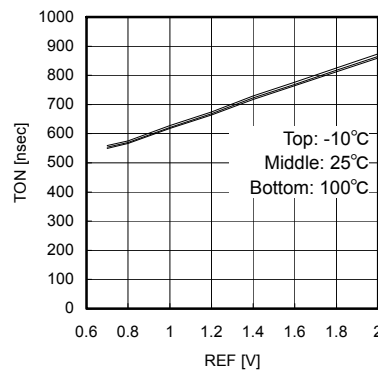

Fig.7 Vcc vs VREG (Start up)
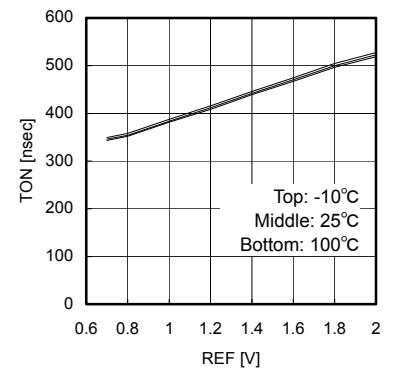

Fig.8 REF vs ON TIME
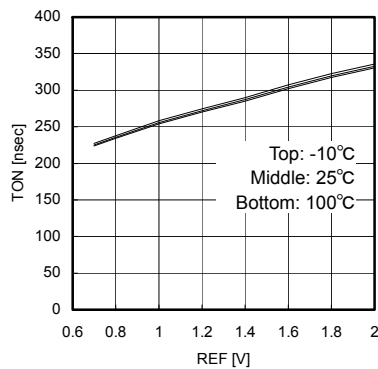(VIN=7V)

Fig.9 REF vs ON TIME
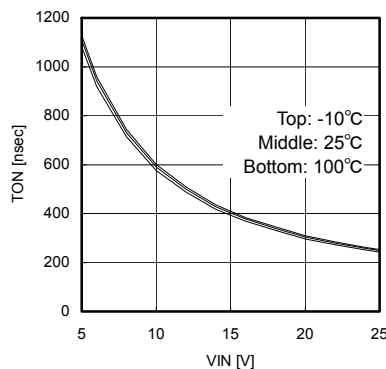(VIN=12V)

Fig.10 REF-ON TIME
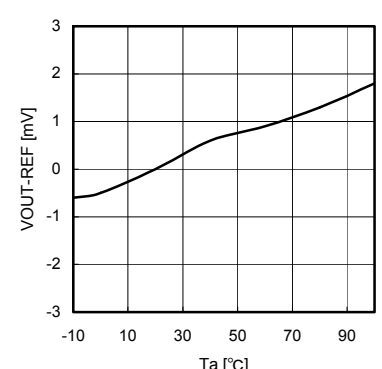(VIN=25V)

Fig.11 VIN-ON TIME
(REF=1.8V)
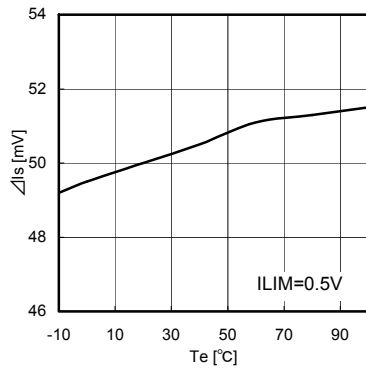

Fig.12 Ta vs VOUT offset

●Reference Data

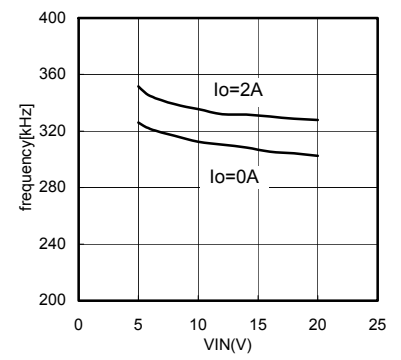Fig.13 Ta vs current limit threshould
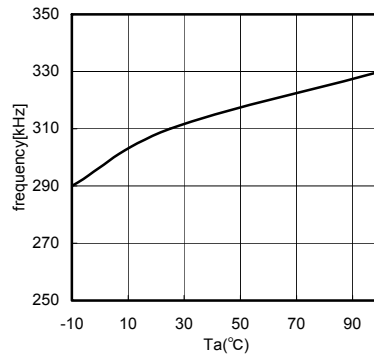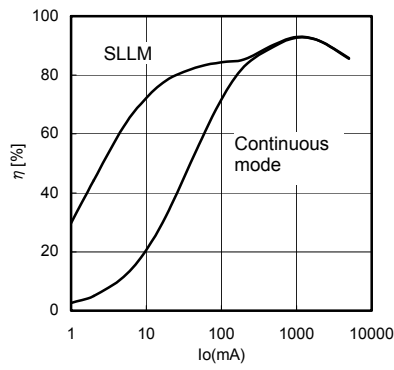

Fig.14 Ta vs Frequency

Fig.15 V$_{IN}$ vs Frequency

Fig.16 Io vs Efficiency (V$_{IN}$=7V)
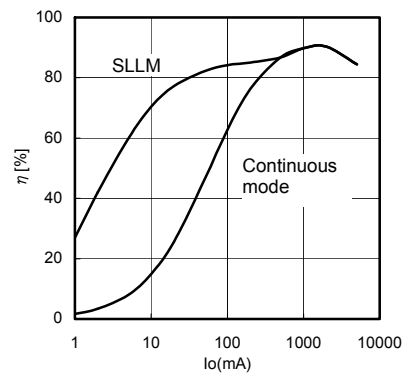
Fig.17 Io vs Efficiency (V$_{IN}$=12V)
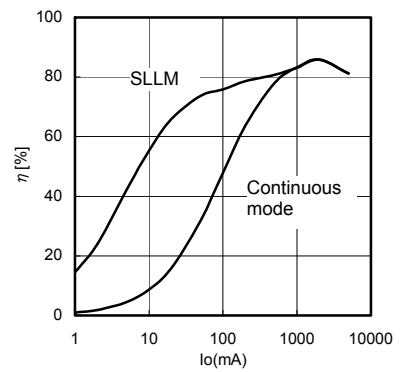
Fig.18 Io vs Efficiency (V$_{IN}$=20V)
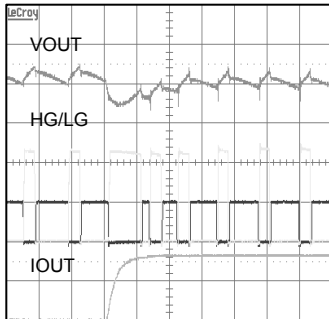
Fig.19 Load Transient Response (V$_{IN}$=7V)
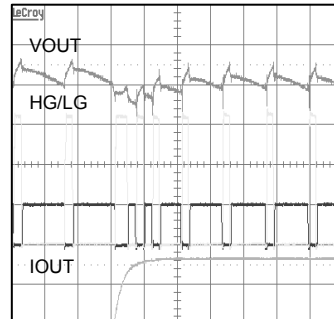
Fig.20 Load Transient Response (V$_{IN}$=12V)
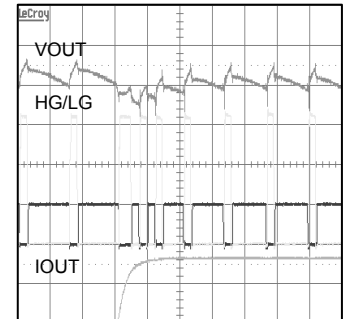
Fig.21 Load Transient Response (V$_{IN}$=19V)
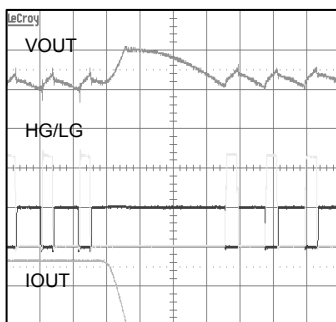
Fig.22 Load Transient Response (V$_{IN}$=7V)
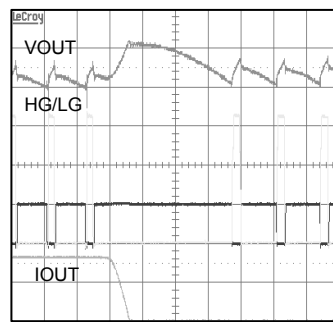
Fig.23 Load Transient Response (V$_{IN}$=12V)
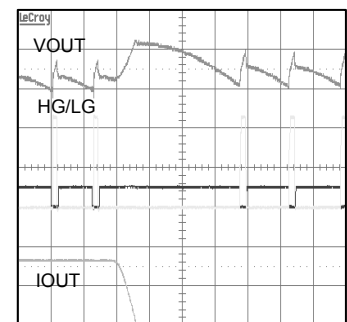
Fig.24 Load Transient Response (V$_{IN}$=19V)

●Reference Data
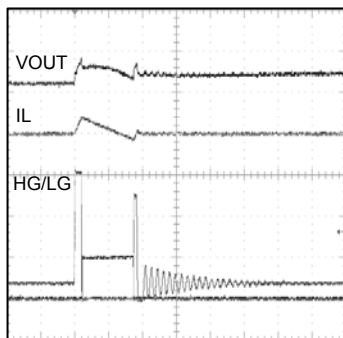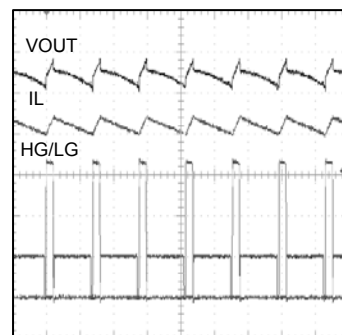

Fig.25 SLLM
(IOUT=0A)
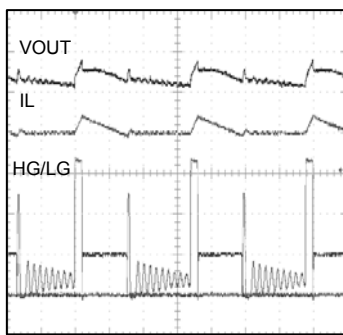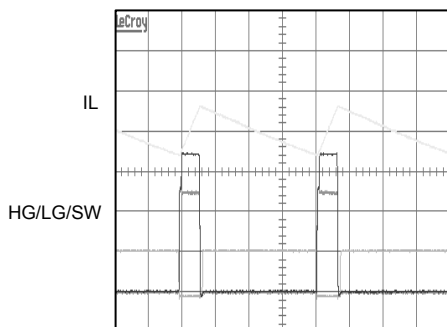

Fig.26 SLLM
(IOUT=0.4A)

Fig.27 SLLM
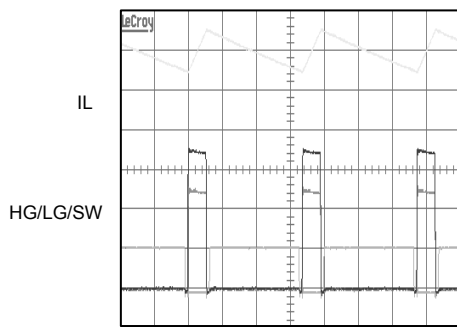(IOUT=1A)

Fig.28 Continuous MODE
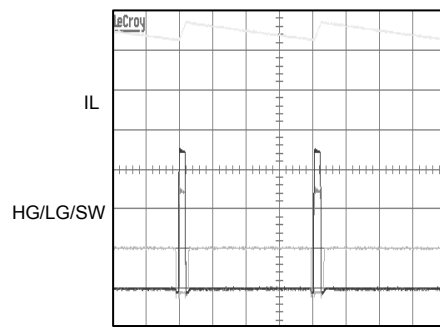(Io=0A)

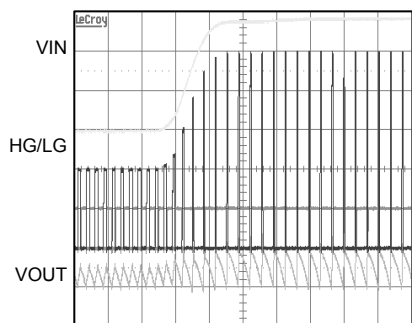Fig.29 Continuous MODE
(Io=4A)

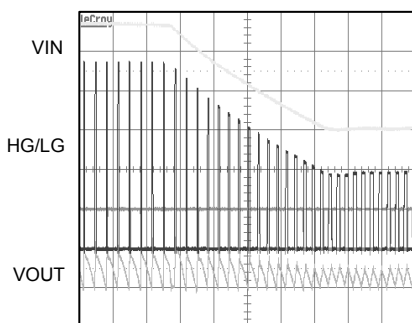Fig.30 Continuous MODE
(Io=5A)
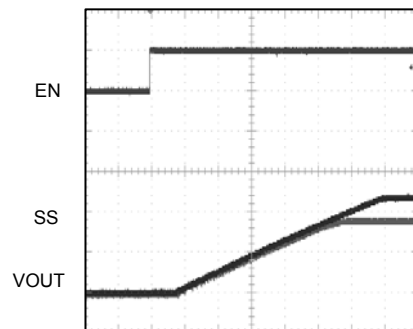

Fig.31 VIN change
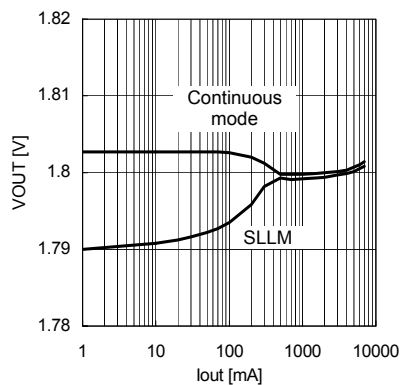(5→19V)

Fig.32 VIN change
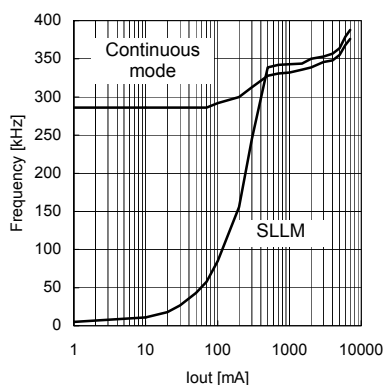(19→5V)

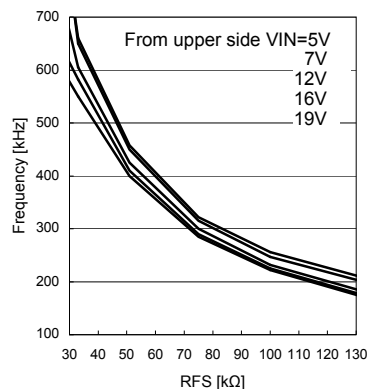Fig.33 FS VIN wake up

Fig.34 IOUT-VOUT

Fig.35 IOUT-Frequency

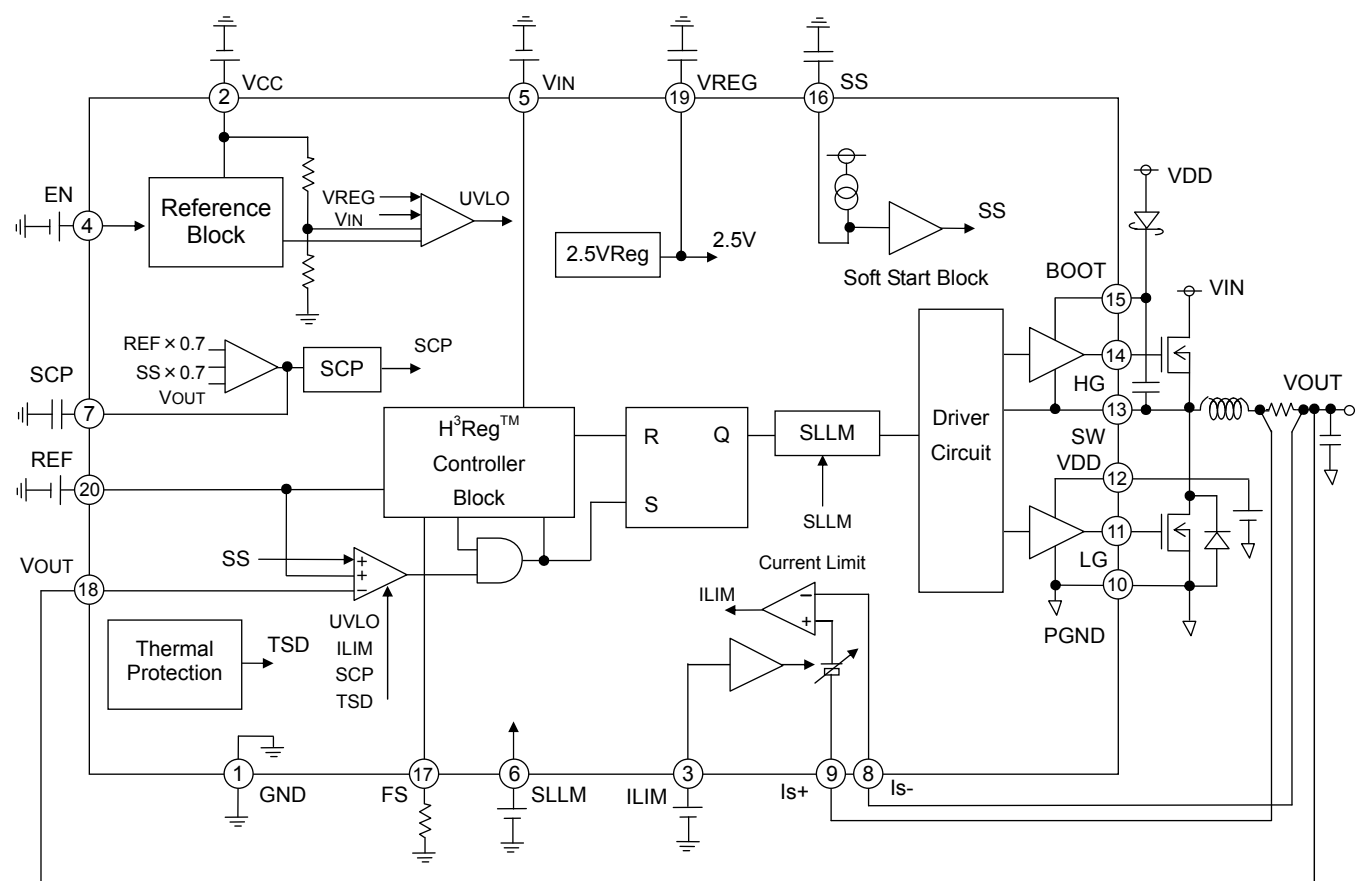Fig.36 FS resistance- Frequency

●Block Diagram

●PHYSICAL DIMENSIONS

BD9532

0.22±0.05

⊕ |0.05|M|

1PIN MARK　Lot No.

0.95MAX

0.02 +0.03 −0.02

0.22±0.05

△ |0.05|

(2.1)

0.5

(0.22)

3-(0.35)

(0.5)

(2.1)

0.6 +0.1 −0.3

(UNIT : mm)

HQFN20V
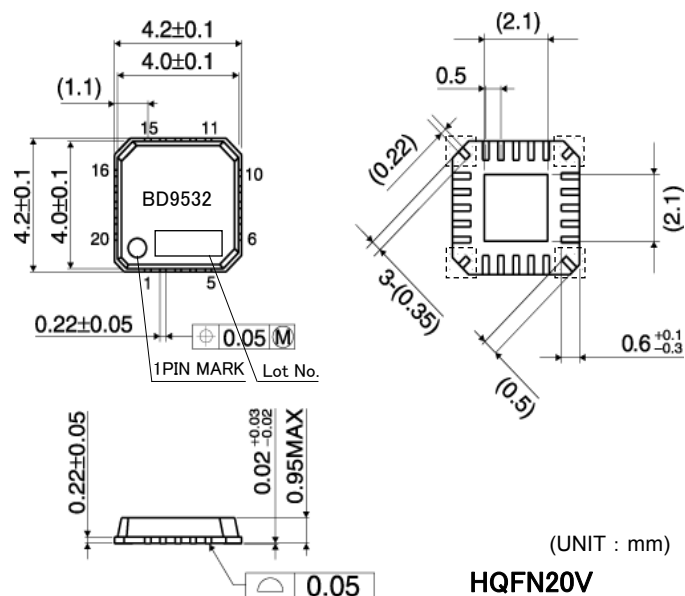
※ Mounting is not recommended to the dotted line part.

●Pin Number・Pin Name

Pin No.	Pin Name
1	GND
2	VCC
3	ILIM
4	EN
5	VIN
6	SLLM
7	SCP
8	IS-
9	IS+
10	PGND
11	LG
12	VDD
13	SW
14	HG
15	BOOT
16	SS
17	FS
18	VOUT
19	VREG
20	REF
-	FIN

Please short FIN to the 1PIN

●Pin Descriptions

・GND(1pin)
This is the ground pin for IC internal circuits. It is equivalent to FIN voltage.

・VCC(2pin)
This is the power supply pin for IC internal circuits, except the FET driver. The maximum circuit current is 900uA. The input supply voltage range is 4.5V to 5.5V. It is recommended that a 0.1uF bypass capacitor be put in this pin.

・ILIM(3pin)
BD9532EKN detects the voltage between Is+ pin and Is- pin and limits the output current (OCP). Voltage equivalent to 1/10 of the ILIM voltage is the voltage drop of external current sense resistor. A very low current sense resistor or inductor DCR can also be used for this platform.

・EN(4pin)
When EN pin voltage is at least 2.3V, the status of this switching regulator becomes active. Conversely, the status switches off when EN pin voltage goes lower than 0.8V and circuit current becomes 10uA.

・VIN(5pin)
The duty cycle is determined by input voltage and output voltage. In other words, the output voltage is affected by input voltage. Therefore, when VIN voltage fluctuates, the output voltage becomes also unstable. Since the VIN line is also the input voltage of the switching regulator, stability depends on the impedance of the voltage supply. It is recommended to establish a bypass capacitor or CR filter suitable for the actual application.

・SLLM(6pin)
This is the switch shift pin for Simple Light Load Mode. The efficiency in SLLM is improved when SLLM pin voltage goes lower than 0.5V.

・SCP(7pin)
This is the pin to adjust the timer latch time for short circuit protection. The timer circuit is active when the pin voltage becomes 70% of REF, and the output switches OFF and latched after the specified time. When the UVLO circuit is active or EN is low, this latch function is cancelled.

・Is-(8pin) ,Is+(9pin)
These pins are connected to both sides of the current sense resistor to detect output current. The voltage drop between Is+ and Is- is compared with the voltage equivalent to 1/10 of ILIM voltage. When this voltage drop reaches the specified voltage level, the output voltage goes OFF.

・PGND(10pin)
This is the power ground pin connected to the source of the low side FET.

・LG(11pin)
This is the voltage supply to drive the Gate of the low side FET. This voltage swings between VDD and PGND. High-speed Gate driving for the low side FET is achieved due to the low on-resistance (2 ohm when LG is high, 0.5 ohm when LG is low) of the driver.

・VDD(12pin)
This is the power supply pin to drive the LOW side FET. It is recommended that a 1uF bypass capacitor be established to compensate for rush current during the FET ON/OFF transition.

・SW(13pin)
This is the source pin for the high side FET. The maximum absolute ratings are 30V (from GND). SW voltage swings between VIN and GND.

・HG(14pin)
This is the voltage supply to drive the Gate of the high side FET. This voltage swings between BOOT and SW. High-speed Gate driving for the high side FET is achieved due to the low on-resistance (3 ohm when HG is high, 2 ohm when HG is low) of the driver.

・BOOT(15pin)
This is the voltage supply to drive the high side FET. The maximum absolute ratings are 35V (from GND) and 7V (from SW). BOOT voltage swings between VIN+Vcc and Vcc during active operation.

・SS(16pin)
This is the adjustment pin to set the soft start time. SS voltage is low during standby status. When EN is ON, the soft start time can be determined by the SS charge current and capacitor between SS-GND. Until SS reaches REF voltage, the output voltage is equivalent to SS voltage.

・FS(17pin)
This is the pin to adjust the switching frequency based on the resistor value. The frequency range is f=200KHz - 600KHz.

・VOUT(18pin)
This is the output voltage sense pin. It is also possible to adjust the output voltage using external resistor divider based on the equation, REF≒VOUT.

・VREG(19pin)
This is the reference voltage output pin. The voltage is 2.5V, with 100uA current ability. It is recommended that a 1uF capacitor (X5R or X7R) be established between VREG and GND. When REF is not adjusted from the external voltage supply, the REF voltage can be adjusted using the external resistor divider of VREF.

・REF(20pin)
This is the output voltage adjustment pin. It is very convenient for synchronizing external voltage supply. The IC controls the output voltage (REF≒VOUT).

●Explanation of Operation

The BD9532EKN is a synchronous buck regulator controller incorporating ROHM's proprietary H^{3}Reg^{TM} CONTROLLA control system. When V$_{OUT}$ drops due to a rapid load change, the system quickly restores V$_{OUT}$ by extending the T$_{ON}$ time interval. Thus, it serves to improve the regulator's transient response. Activating the Light Load Mode will also exercise Simple Light Load Mode (SLLM) control when the load is light, to further increase efficiency.

H^{3}Reg^{TM} control
(Normal operation)
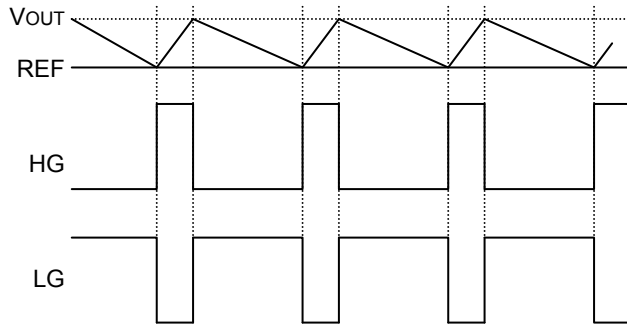
When V$_{OUT}$ falls to a threshold voltage (REF), the drop is detected, activating the H^{3}Reg^{TM} CONTROLLA system.

$$T_{ON} = \frac{REF}{V_{IN}} \times \frac{1}{f} \ [sec] \cdot\cdot\cdot (1)$$

HG output is determined with the formula above.
LG outputs until the status of V$_{OUT}$ is lower than REF after the status of HG is off.

(V$_{OUT}$ drops due to a rapid load change)
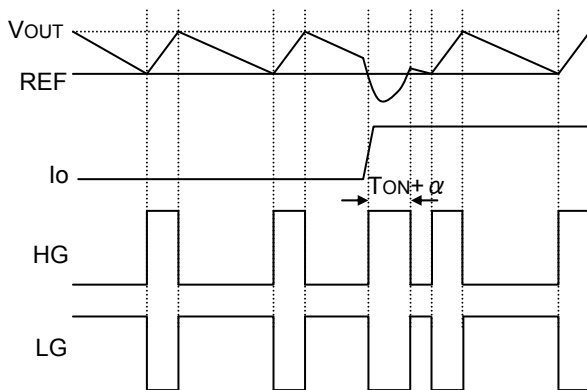
When V$_{OUT}$ drops due to a rapid load change, and the voltage remains below REF after the programmed T$_{ON}$ time interval has elapsed, the system quickly restores V$_{OUT}$ by extending the T$_{ON}$ time, improving the transient response.

(SLLM)
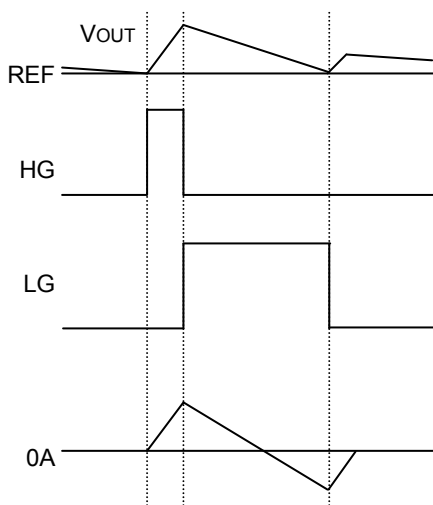
In SLLM (SLLM=0V), SLLM function is operated when LG pin is OFF and the coil current is lower than 0A (the current goes from V$_{OUT}$ to SW). And it stops to output next HG.
When V$_{OUT}$ goes lower than REF voltage again, the status of HG is ON.

●Timing Chart
 ・Soft Start Function

EN

SS

T_{SS}

V_{OUT}

IIN
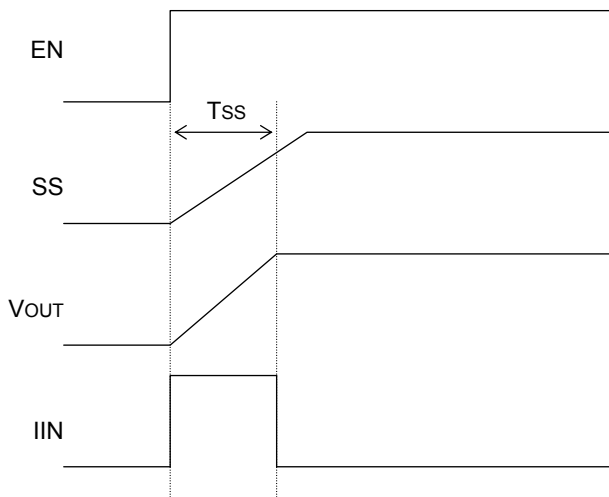
Soft start is exercised with the EN pin set high. Current control takes effect at startup, enabling a moderate output voltage "ramping start." Soft start timing and incoming current are calculated with formulas (2) and (3) below.
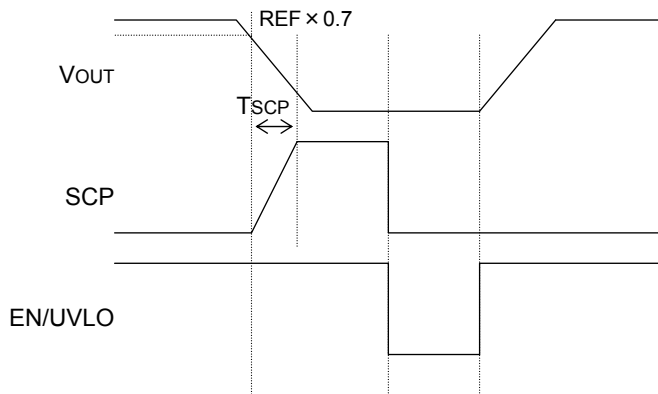
Soft start time

$$Tss = \frac{REF \times Css}{2\mu A(typ)} \quad [sec] \cdot \cdot \cdot (2)$$

Incoming current

$$I_{IN} = \frac{Co \times V_{OUT}}{Tss} \quad [A] \cdot \cdot \cdot (3)$$

(Css: Soft start capacitor;   Co: Output capacitor)

 ・Timer Latch Type Short Circuit Protection

V_{OUT}

REF × 0.7

T_{SCP}

SCP

EN/UVLO

Short protection kicks in when output falls to or below REF X 0.7. When the programmed time period elapses, output is latched OFF to prevent destruction of the IC. Output voltage can be restored either by reconnecting the EN pin or disabling UVLO. Short circuit protection time is programmed using formula (4) below.

Short protection time setting

$$Tscp = \frac{1.25(V) \times C_{SCP}}{2\mu A(typ)} \quad [sec] \cdot \cdot \cdot (4)$$

 ・Over current protection circuit

HG

t_{ON} t_{ON} T_{MAX}

LG

I_{LIMIT}

I_L
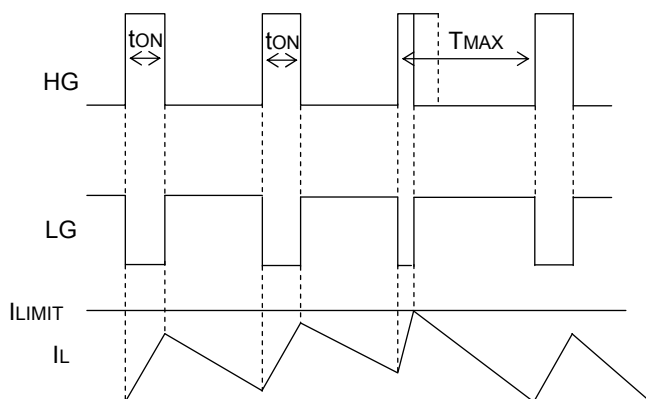
During the normal operation, when VOUT becomes less than REF Voltage, HG becomes High during the time TON. However, when inductor current exceeds I_{LIMIT} threshold, HG becomes OFF.
After MAX ON TIME, HG becomes ON again if the output voltage is lower than the specific voltage level and I_L is lower than I_{LIMIT} level.

●External Component Selection

1. Inductor (L) selection
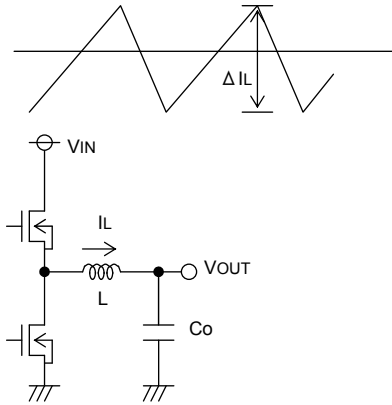
Output ripple current

The inductor value is a major influence on the output ripple current. As formula (5) below indicates, the greater the inductor or the switching frequency, the lower the ripple current.

$$\Delta I_L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [A] \cdots (5)$$

The proper output ripple current setting is about 30% of maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT}max. \quad [A] \cdots (6)$$

$$L = \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{IN} \times f} \quad [H] \cdots (7)$$

(ΔI_L: output ripple current; f: switch frequency)

※Passing a current larger than the inductor's rated current will cause magnetic saturation in the inductor and decrease system efficiency. In selecting the inductor, be sure to allow enough margin to assure that peak current does not exceed the inductor rated current value.

※To minimize possible inductor damage and maximize efficiency, choose a inductor with a low (DCR, ACR) resistance.

2.Output Capacitor (Co) Selection
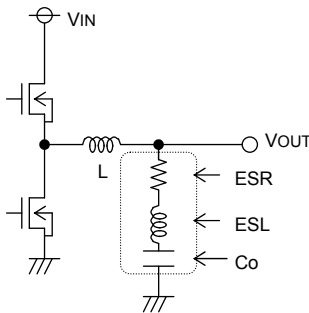
Output capacitor

When determining the proper output capacitor, be sure to factor in the equivalent series resistance required to smooth out ripple volume and maintain a stable output voltage range.

Output ripple voltage is determined as in formula (8) below.

$$\Delta V_{OUT} = \Delta I_L \times ESR + ESL \times \Delta I_L/T_{ON} \quad [V] \cdots (8)$$

(ΔI_L: Output ripple current; ESR: Co equivalent series resistance, ESR:equivalent series inductance)

※ In selecting a capacitor, make sure the capacitor rating allows sufficient margin relative to output voltage. Note that a lower ESR can minimize output ripple voltage.

Please give due consideration to the conditions in formula (9) below for output capacity, bearing in mind that output rise time must be established within the soft start time frame.

$$Co \leqq \frac{Tss \times (Limit - I_{OUT})}{V_{OUT}} \cdots (9)$$

Tss: Soft start time
Limit: Over current detection

Note: Improper capacitor may cause startup malfunctions.

3. Input Capacitor (Cin) Selection
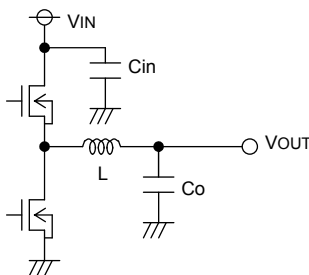
Input Capacitor

The input capacitor selected must have low enough ESR resistance to fully support large ripple output, in order to prevent extreme over current. The formula for ripple current IRMS is given in (10) below.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN}-V_{OUT})}}{V_{IN}} \quad [A] \cdots (10)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and maximize efficiency.

4. MOSFET Selection
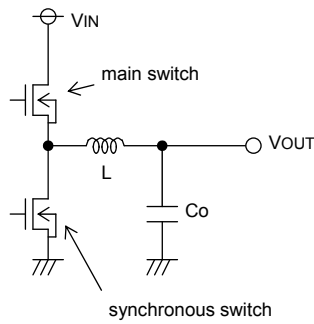
Loss on the main MOSFET

$$P_{main}=P_{RON}+P_{GATE}+P_{TRAN}$$

$$=\frac{V_{OUT}}{V_{IN}}\times R_{ON}\times I_{OUT}^2+C_{iss}\times f\times V_{DD}+\frac{V_{IN}^2\times C_{rss}\times I_{OUT}\times f}{I_{DRIVE}}\quad\cdots(11)$$
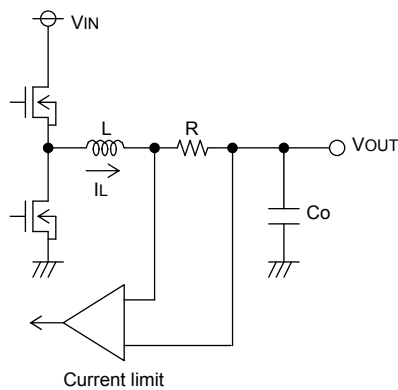
(Ron: On-resistance of FET; Ciss: FET gate capacity;
f: Switching frequency Crss: FET inverse transfer function;
I_{DRIVE}: Gate peak current)

Loss on the synchronous MOSFET

$$P_{syn}=P_{RON}+P_{GATE}$$

$$=\frac{V_{IN}-V_{OUT}}{V_{IN}}\times R_{ON}\times I_{OUT}^2+C_{iss}\times f\times V_{DD}\quad\cdots(12)$$

5. Setting Detection Resistance

The over current protection function detects the output ripple current peak value. This parameter (setting value) is determined as in formula (13) below.

$$I_{LMIT}=\frac{V_{ILIM}\times0.1}{R}\;[A]\cdots(13)$$

(V_{ILIM}: ILIM voltage;   R: Detection resistance)
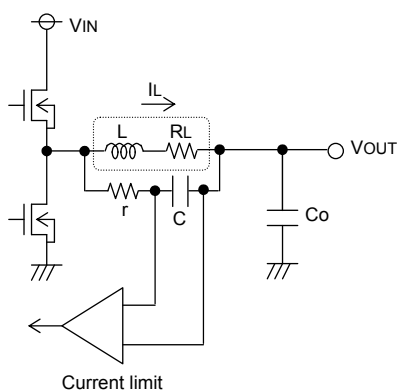
When the over current protection is detected by DCR of coil L, this parameter (setting value) is determined as in formula (14) below.
 (Application circuit:P20)

$$I_{LMIT}=V_{ILIM}\times0.1\times\frac{r\times C}{L}\;[A]\cdots(14)$$

$$(RL=\frac{L}{r\times C})$$

(V_{ILIM}:ILIM voltage   RL: the DCR value of coil)
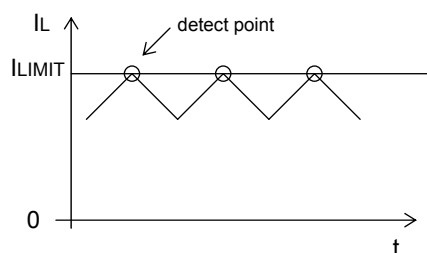
As soon as the voltage drop between Is+ and Is- generated by the inductor current becomes specific threshold, the gate voltage of the high side MOSFET becomes low.
Since the peak voltage of the inductor ripple current is detected, this operation can sense high current ripple operation caused by inductance saturated rated current and lead to high reliable systems.

6.Setting frequency
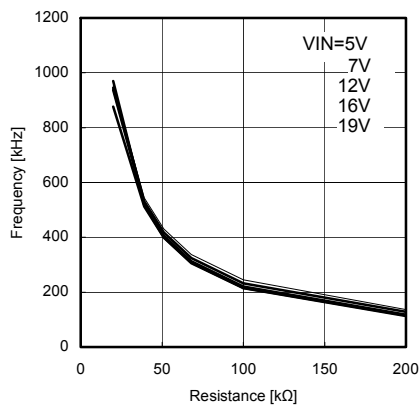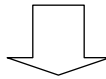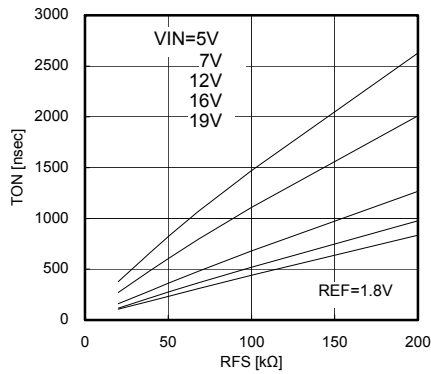
The On Time(T_{ON}) at steady state is determined by resistance value connected to FS pin.
But actually SW rising time and falling time come up due to influence of the external MOSFET gate capacity or switching speed and T_{ON} is increased.
The frequency is determined by the following formula after TON, input current and the REF voltage are fixed.

$$F= \frac{REF}{V_{IN} \times T_{ON}} \quad \cdot\cdot\cdot(15)$$

Consequently, total frequency becomes lower than the formula above.
TON is also influenced by Dead Time around the output current 0A area in continuous mode.
This frequency becomes lower than setting frequency.
It is recommended to check the steady frequency in large current area (at the point where the coil current doesn't back up).

7. Setting standard voltage (REF)
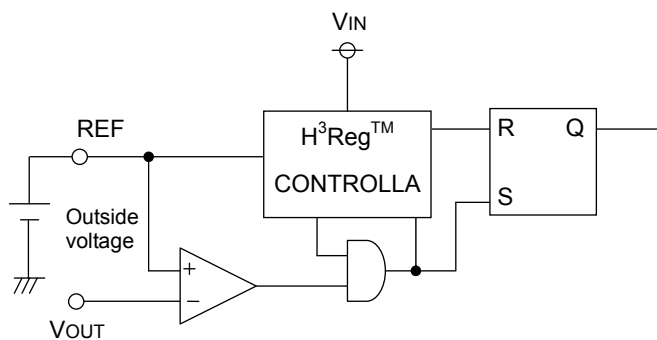
It is available to synchronize setting the reference voltage (REF) with outside supply voltage [V] by using outside power supply voltage.
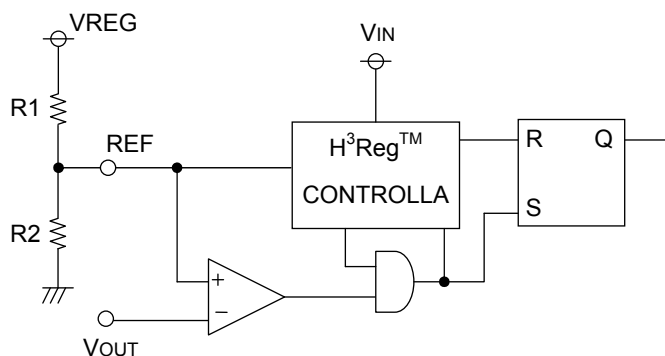
It is available to set the reference voltage (REF) by the resistance division value from VREG in case it is not set REF from an external power supply.

$$REF= \frac{R2}{R1+R2} \times VREG \ [V] \cdot\cdot\cdot(16)$$

8. Setting output voltage

This IC is operated that output voltage is REF≒VOUT.

And it is operated that output voltage is feed back to FB pin in case the output voltage is 0.7V to 2.0V.
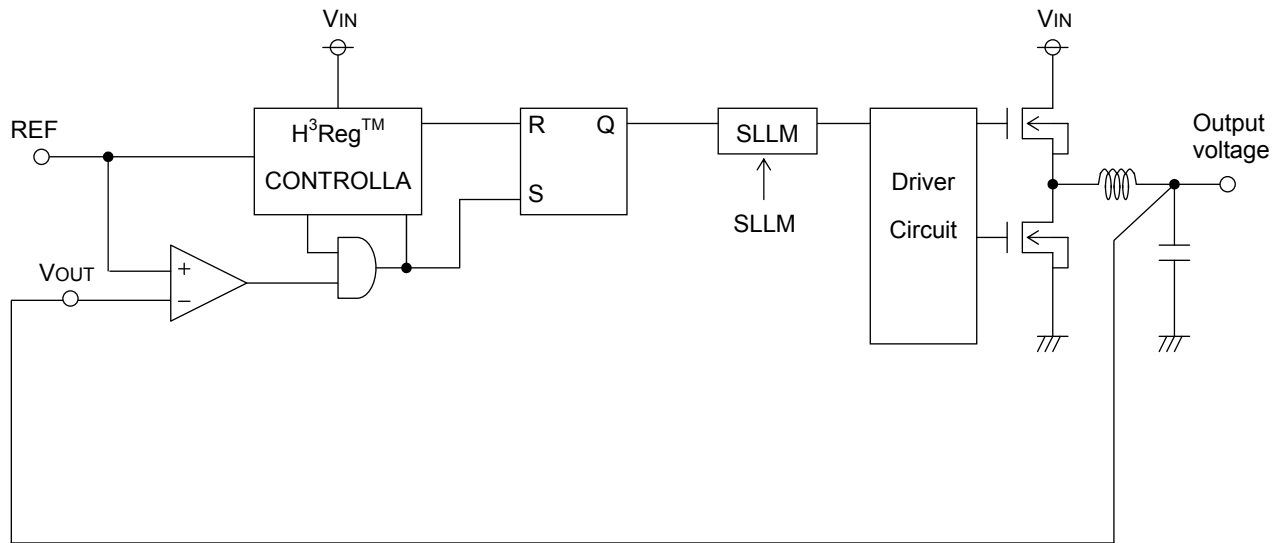
In case the output voltage range is 0.7V to 2.0V.

It is operated that the resistance division value of the output voltage is feed back to V_{OUT} pin in case the output voltage is more than 2.0V.

$$\text{output voltage} \fallingdotseq \frac{R1+R2}{R2} \times REF \ [V] \cdot\cdot\cdot (17)$$

In case the output voltage is more than 2.0V.

●I/O Equivalent Circuit
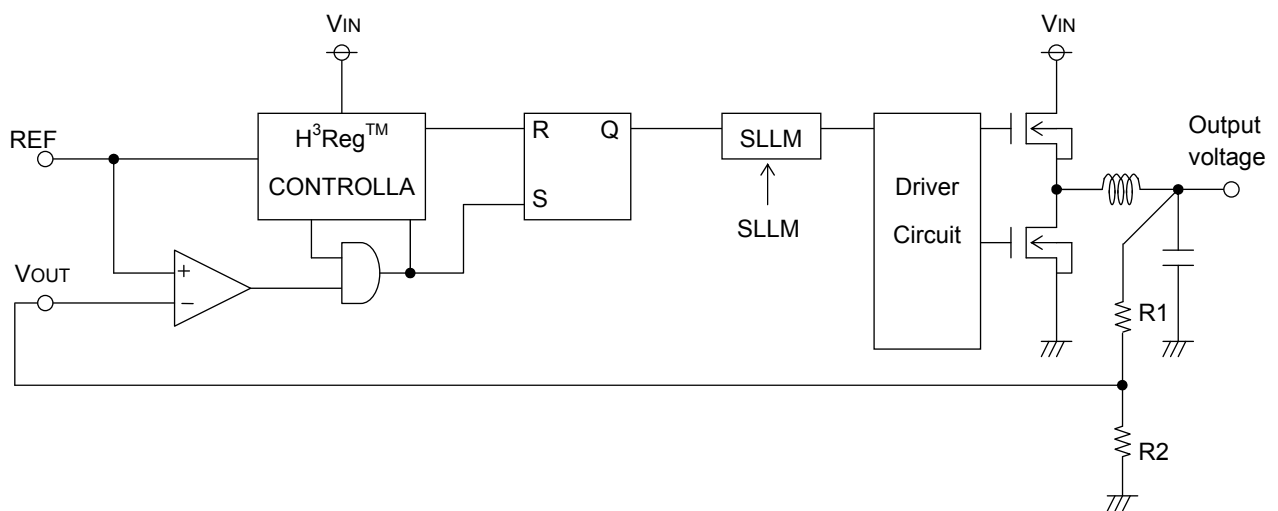
3pin (ILIM)
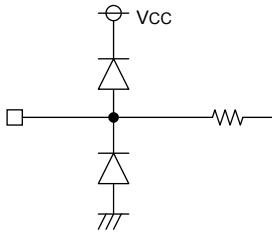
4pin (EN)
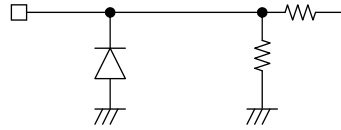
5pin (VIN)
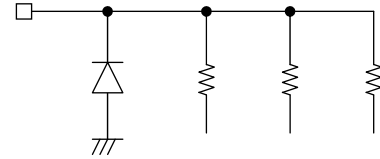
6pin (SLLM)

7pin (SCP)

8pin (Is-)
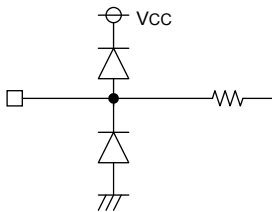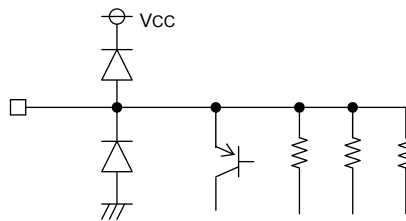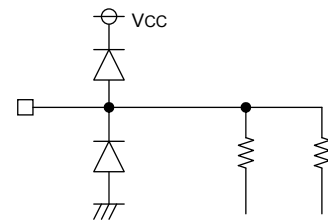
9pin (Is+)
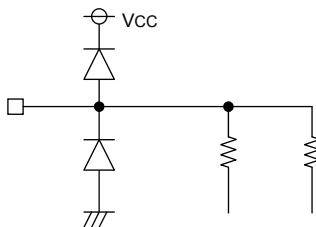
11pin (LG)
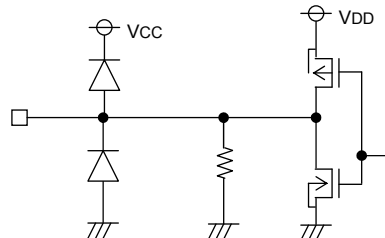
13pin (SW)
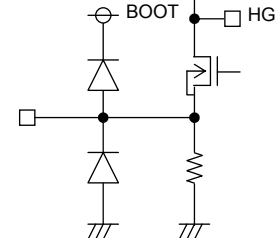
14pin(HG)
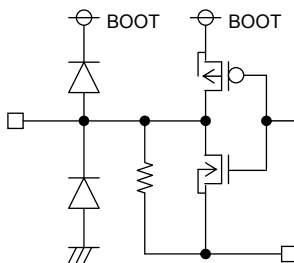
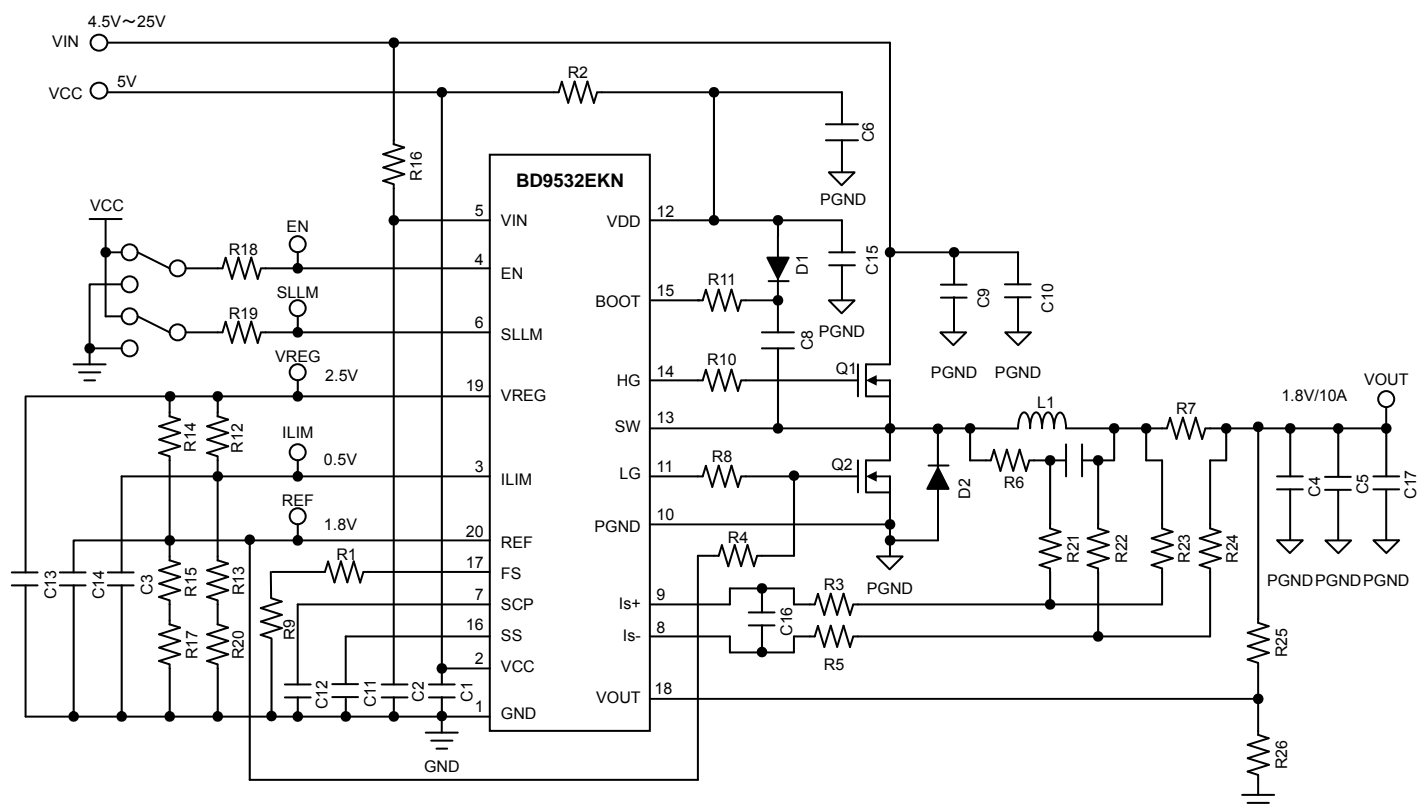15pin (BOOT)
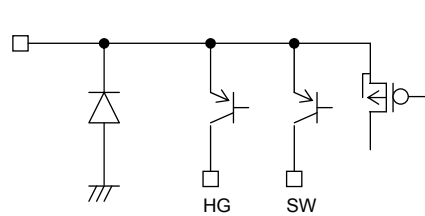
16pin (SS)
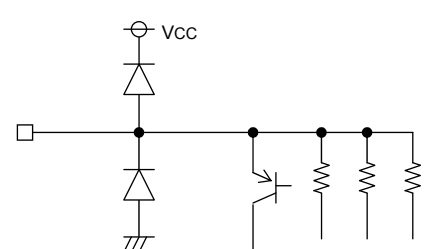
17pin (FS)
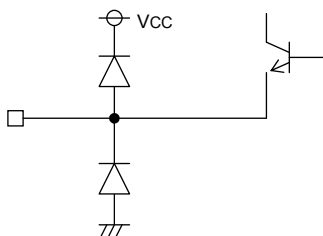
18pin (VOUT)
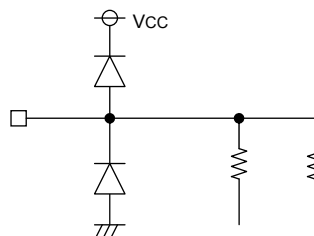
19pin (VREG)
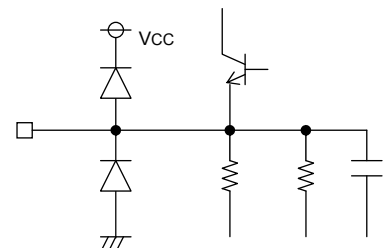
20pin (REF)
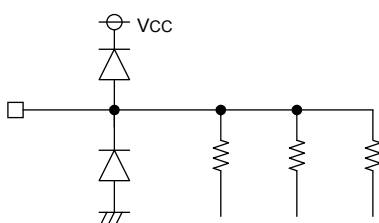
●Evaluation Board Circuit (Frequency=300kHz application circuit in Continuous mode/SLLM)

Part No	Value	Company	Part name
U1		ROHM	BD9532EKN
Q1		ROHM	RSS100N03
Q2		ROHM	RSS100N03
D1		ROHM	RB521S-30
D2		ROHM	RB051L-40
C1	1uF	KYOCERA	CM105B105K06A
C2	10nF	MURATA	GRM39X7R103K50
C3	100pF	MURATA	GRM39C0G101J50
C4			
C5			
C6	10uF	KYOCERA	CM21B106M06A
C7			
C8	0.1uF	KYOCERA	CM105B104K25A
C9	10uF	KYOCERA	CT32X5R106K25A
C10	10uF	KYOCERA	CT32X5R106K25A
C11	1000pF	MURATA	GRM39X7R102K50
C12	1500pF	MURATA	GRM39X7R152K50
C13	1uF	KYOCERA	CM105B105K06A
C14	100pF	MURATA	GRM39C0G101J50
C15	10uF	KYOCERA	CM21B106M06A
C16			
C17	470uF	SANYO	2R5TPE470ML
R1	68KΩ	ROHM	MCR03
R2	0Ω	ROHM	MCR03
R3	0Ω	ROHM	MCR03

Part No	Value	Company	Part name
R4			
R5	0Ω	ROHM	MCR03
R6			
R7	5mΩ	ROHM	PMR100
R8	0Ω	ROHM	MCR03
R9	0Ω	ROHM	MCR03
R10	0Ω	ROHM	MCR03
R11	0Ω	ROHM	MCR03
R12	200kΩ	ROHM	MCR03
R13	51kΩ	ROHM	MCR03
R14	68kΩ	ROHM	MCR03
R15	180kΩ	ROHM	MCR03
R16	1kΩ	ROHM	MCR03
R17	0Ω	ROHM	MCR03
R18	10kΩ	ROHM	MCR03
R19	10kΩ	ROHM	MCR03
R20	0Ω	ROHM	MCR03
R21			
R22			
R23	0Ω	ROHM	MCR03
R24	0Ω	ROHM	MCR03
R25	0Ω	ROHM	MCR03
R26			
L1	1.8uH	SUMIDA	CDEP104-1R8ML

●Evaluation Board Circuit (Frequency=300kHz application circuit for detecting DCR current in Continuous mode/SLLM)
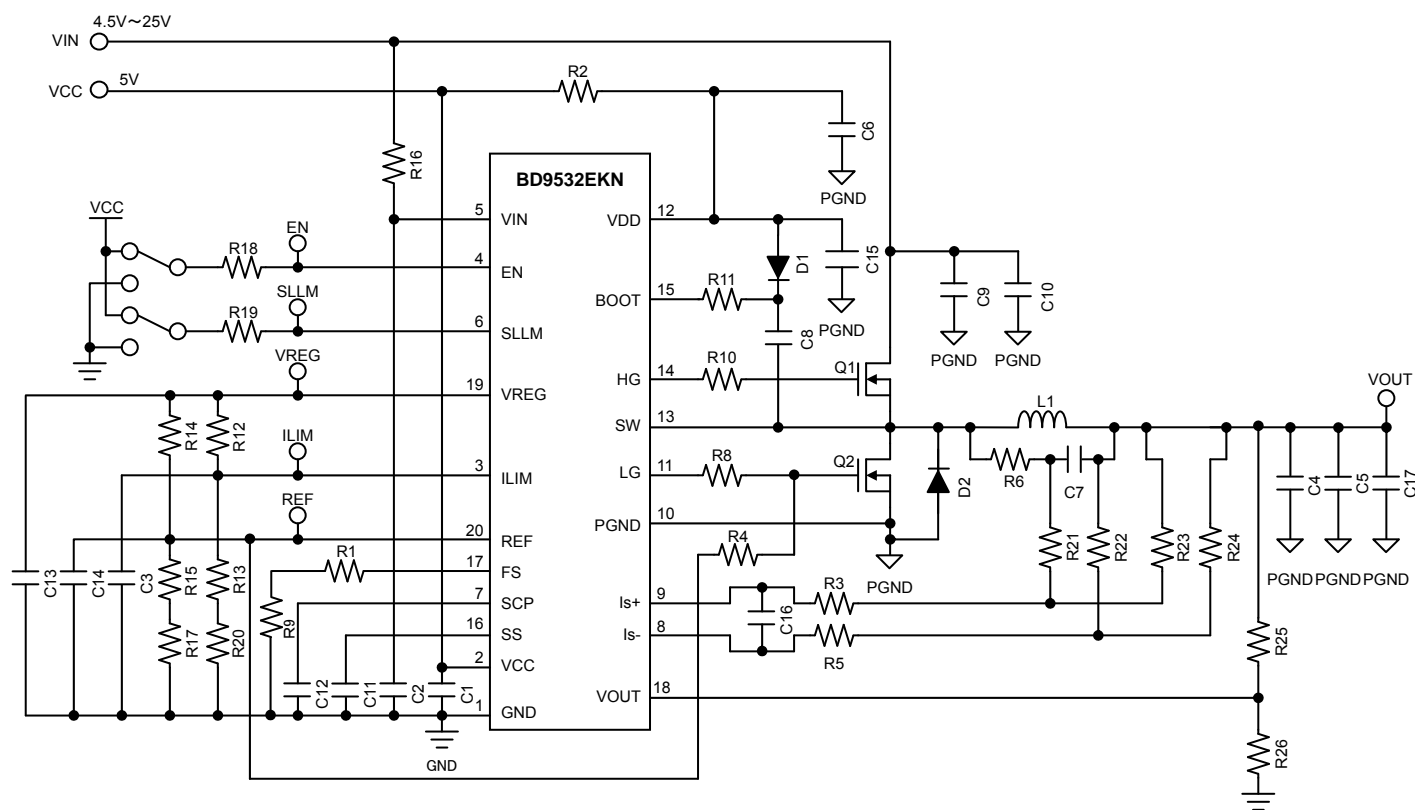
●Evaluation Board Parts List

Part No	Value	Company	Part name	Part No	Value	Company	Part name
U1		ROHM	BD9532EKN	R4			
Q1		ROHM	RSS100N03	R5	0Ω	ROHM	MCR03
Q2		ROHM	RSS100N03	R6	1kΩ	ROHM	MCR03
D1		ROHM	RB521S-30	R7			
D2		ROHM	RB051L-40	R8	0Ω	ROHM	MCR03
C1	1uF	KYOCERA	CM105B105K06A	R9	0Ω	ROHM	MCR03
C2	10nF	MURATA	GRM39X7R103K50	R10	0Ω	ROHM	MCR03
C3	100pF	MURATA	GRM39C0G101J50	R11	0Ω	ROHM	MCR03
C4				R12	51kΩ	ROHM	MCR03
C5				R13	200kΩ	ROHM	MCR03
C6	10uF	KYOCERA	CM21B106M06A	R14	68kΩ	ROHM	MCR03
C7	0.1uF	KYOCERA	CM105B104K25A	R15	180kΩ	ROHM	MCR03
C8	0.1uF	KYOCERA	CM105B104K25A	R16	1kΩ	ROHM	MCR03
C9	10uF	KYOCERA	CT32X5R106K25A	R17	0Ω	ROHM	MCR03
C10	10uF	KYOCERA	CT32X5R106K25A	R18	10kΩ	ROHM	MCR03
C11	1000pF	MURATA	GRM39X7R102K50	R19	10kΩ	ROHM	MCR03
C12	1500pF	MURATA	GRM39X7R152K50	R20	0Ω	ROHM	MCR03
C13	1uF	KYOCERA	CM105B105K06A	R21	0Ω	ROHM	MCR03
C14	100pF	MURATA	GRM39C0G101J50	R22	0Ω	ROHM	MCR03
C15	10uF	KYOCERA	CM21B106M06A	R23			
C16				R24			
C17	330uF	SANYO	6TPB330M	R25	0Ω	ROHM	MCR03
R1	68KΩ	ROHM	MCR03	R26			
R2	0Ω	ROHM	MCR03	L1	3.3uH	NEC/TOKIN	MPLC0730L3R3
R3	0Ω	ROHM	MCR03				

●Operation Notes

1. Absolute maximum ratings

    An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward

    Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines

    Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage

    The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

    Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

    Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field

    Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

    When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

    The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD9532EKN	175	15

10. Testing on application boards

    When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

11. Regarding input pin of the IC

    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
        When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
        When GND > Pin B, the P-N junction operates as a parasitic transistor.
    Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.
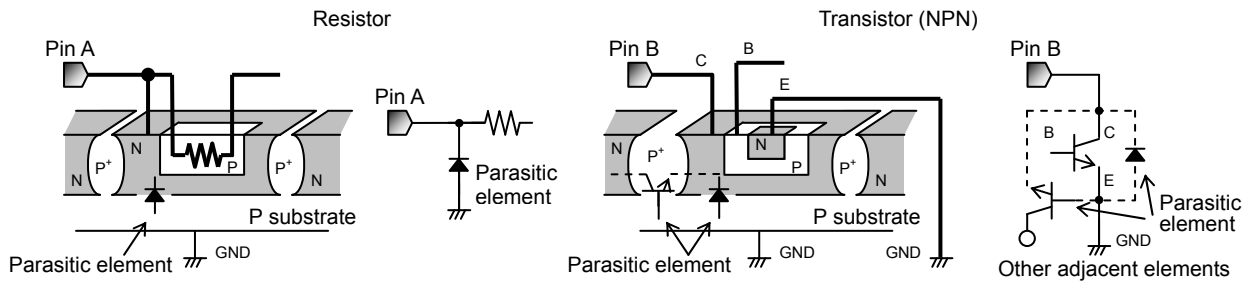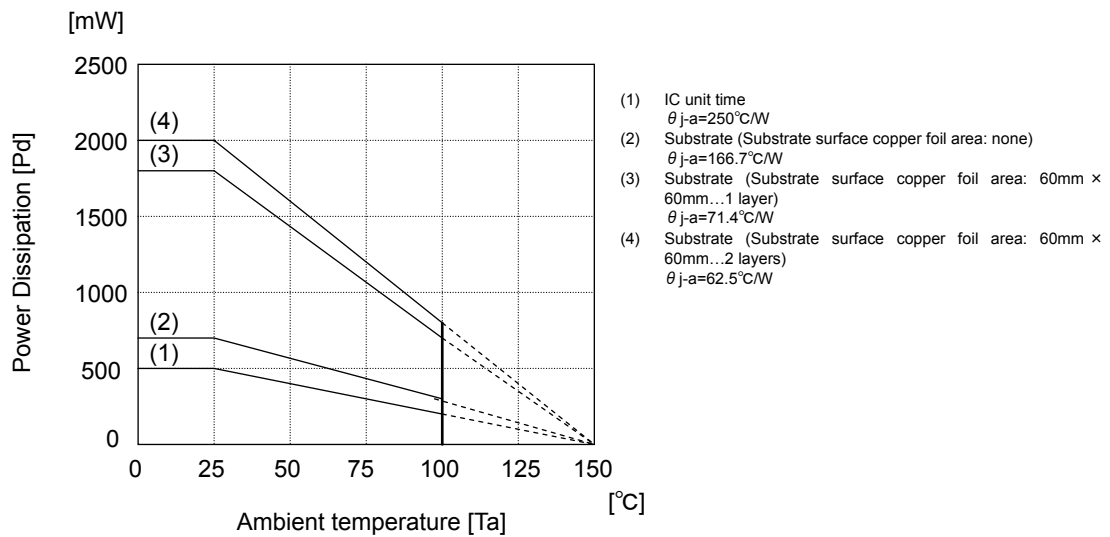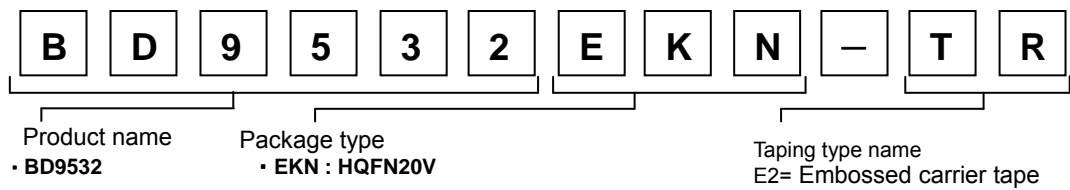
Fig. 31 Example of IC structure

12. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.
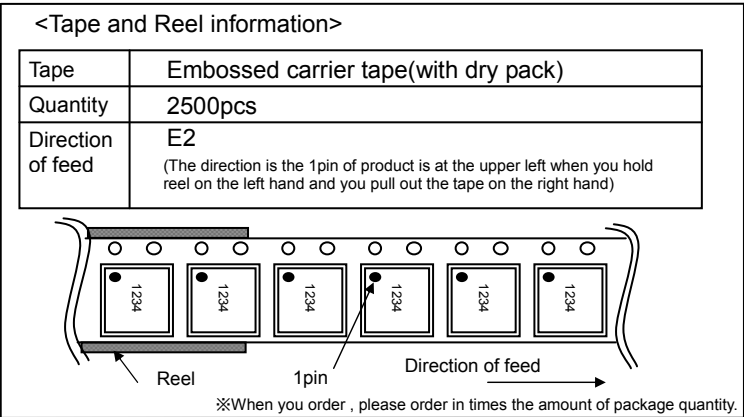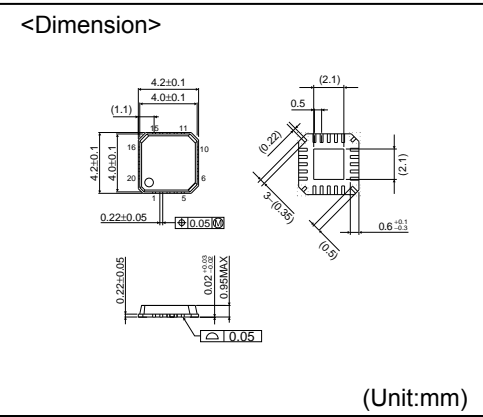
● Power Dissipation

(1) IC unit time
θ j-a=250°C/W
(2) Substrate (Substrate surface copper foil area: none)
θ j-a=166.7°C/W
(3) Substrate (Substrate surface copper foil area: 60mm × 60mm…1 layer)
θ j-a=71.4°C/W
(4) Substrate (Substrate surface copper foil area: 60mm × 60mm…2 layers)
θ j-a=62.5°C/W

● Type Designations (Selections) for Ordering

| B | D | 9 | 5 | 3 | 2 | E | K | N | – | T | R |

Product name
・ BD9532

Package type
・ EKN : HQFN20V

Taping type name
E2= Embossed carrier tape

HQFN20V

<Dimension>

4.2±0.1
4.0±0.1
(1.1)
0.5
(2.1)

(0.22)

15   11
16   10
20   6
1   5

4.2±0.1
4.0±0.1

(2.1)

3 (0.35)

0.22±0.05   ⊕ 0.05 Ⓜ

0.6 +0.1 -0.3

(0.5)

0.22±0.05   0.02 +0.03 -0.02
0.95MAX

⬠ 0.05

(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape(with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

Reel   1pin   Direction of feed

※When you order , please order in times the amount of package quantity.

The products listed in this catalog are designed to be used with ordinary electronic equipment or devices (such as audio visual equipment, office-automation equipment, communications devices, electrical appliances and electronic toys).
Should you intend to use these products with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

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