Gate Driver Providing Galvanic isolation Series

Isolation voltage 2500Vrms
1ch Gate Driver Providing Galvanic Isolation

BM60016FV-C

General Description

The BM60016FV-C is a gate driver with an isolation voltage of 2500Vrms, I/O delay time of 75ns, and minimum input pulse width of 60ns. It incorporates the Under-voltage Lockout (UVLO) function and Miller clamp function.

Key Specifications

- Isolation voltage: 2500Vrms
- Maximum gate drive voltage: 24V
- I/O delay time: 75ns(Max)
- Minimum input pulse width: 60ns

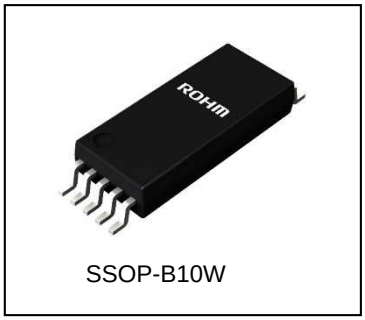
Features

- Providing Galvanic Isolation
- Active Miller Clamping
- Under-voltage Lockout function
- UL1577(pending)
- AEC-Q100 Qualified *(Note1)*

(Note 1:Grade1)

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B10W	3.5mm x10.2mm x 1.9mm



SSOP-B10W

Applications

- IGBT Gate Driver
- MOSFET Gate Driver

Typical Application Circuits

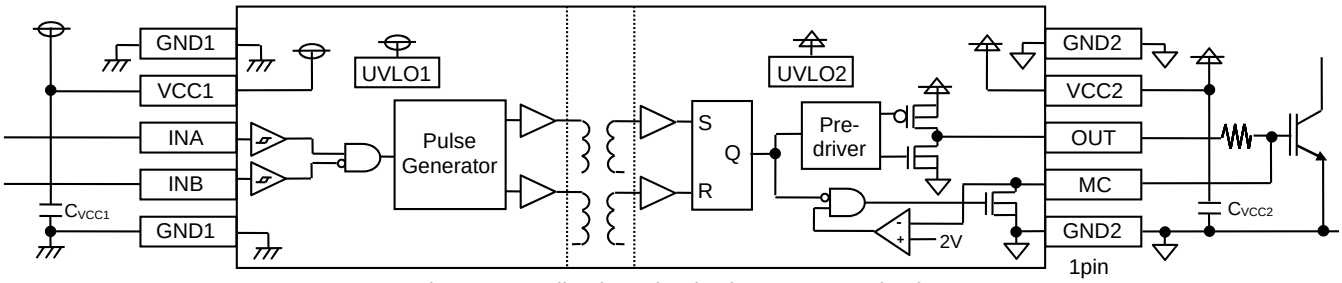


Figure 1. Application Circuits (IGBT Gate Driver)

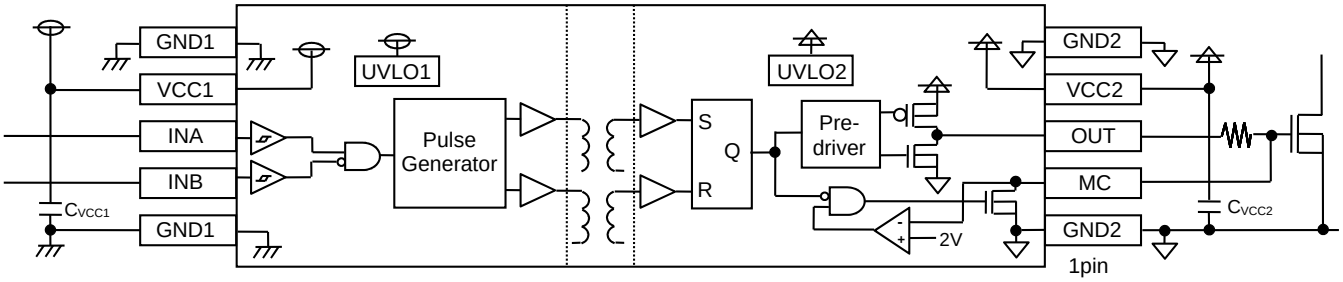


Figure 2. Application Circuits (MOSFET Gate Driver)

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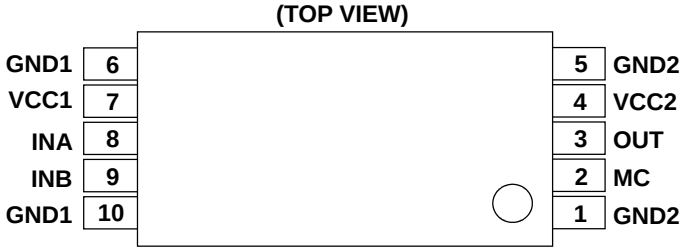
Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min.	Typ.	Max.	
VCC1	C_{VCC1}	0.1	1.0	-	µF
VCC2	C_{VCC2}	0.01	-	-	µF

Pin Configurations



Pin Descriptions

Pin No.	Pin Name	Function
1	GND2	Output-side ground pin
2	MC	Miller Clamp pin
3	OUT	Output pin
4	VCC2	Output-side power supply pin
5	GND2	Output-side ground pin
6	GND1	Input-side ground pin
7	VCC1	Input-side power supply pin
8	INA	Control input pin A
9	INB	Control input pin B
10	GND1	Input-side ground pin

Description of pins and cautions on layout of board

1) VCC1 (Input-side power supply pin)
The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2) GND1 (Input-side ground pin)
The GND1 pin is a ground pin on the input side.

3) VCC2 (Output-side power supply pin)
The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCC2 and the GND2 pins.

4) GND2 (Output-side ground pin)
The GND2 pin is a ground pin on the output side.

5) INA, INB (Control input terminal)
The INA and INB pins are used to determine output logic.

INB	INA	OUT
H	L	L
H	H	L
L	L	L
L	H	H

6) OUT (Output pin)
The OUT pin is used to drive the gate of a power device.

7) MC (Miller Clamp pin)
The MC pin is for preventing the increase in gate voltage due to the Miller current of the power device connected to the OUT pin. If the Miller Clamp function is not used, short-circuit the MC pin to the GND2 pin.

Description of functions and examples of constant setting

1) Miller Clamp function
When INA=L and OUT pin voltage < V_{MCON} (typ 2V), the internal MOSFET of the MC pin is turned ON.

INA	MC	Internal MOSFET of the MC pin
L	less than V_{MCON}	ON
H	X	OFF

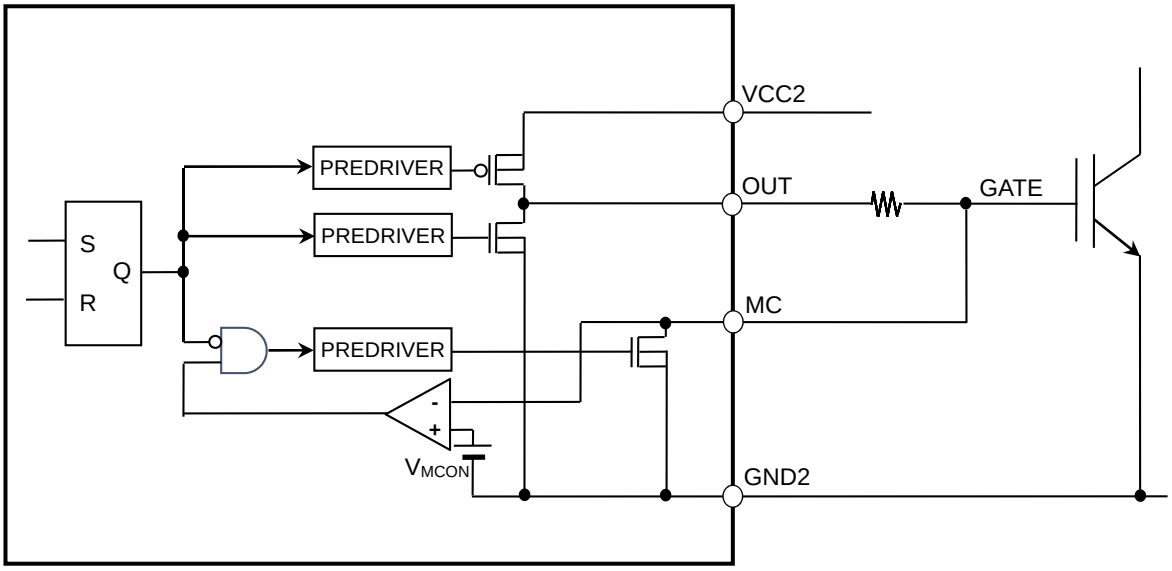


Figure 3. Block diagram of Miller Clamp function.

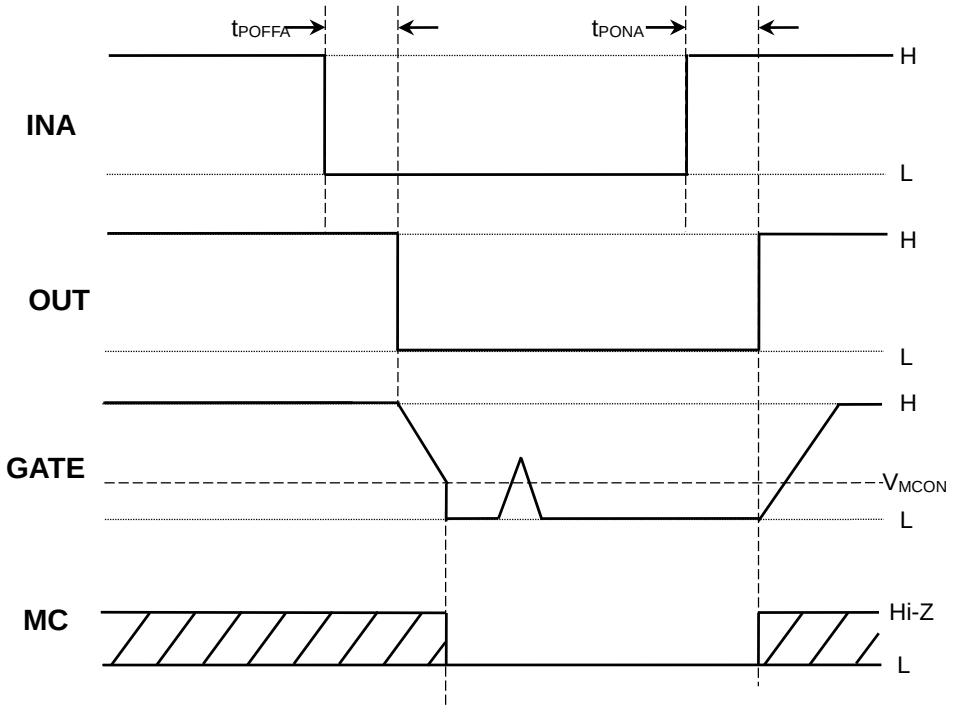


Figure 4. Timing chart of Miller Clamp function

2) Under-voltage Lockout (UVLO) function

The BM60016FV-C incorporates the Under-voltage Lockout (UVLO) function both on the low and the high voltage sides. When the power supply voltage drops to the UVLO ON voltage (low voltage side typ 3.4V, high voltage side voltage typ 8.5V), the OUT pin will output the “L” signal. In addition, to prevent malfunctions due to noises, a mask time of $t_{UVLO1MSK}$ (typ 2.5µs) and $t_{UVLO2MSK}$ (typ 2.9µs) are set on both the low and the high voltage sides.

After the UVLO is released, the input signal will take effect from the time after the input signal switches.

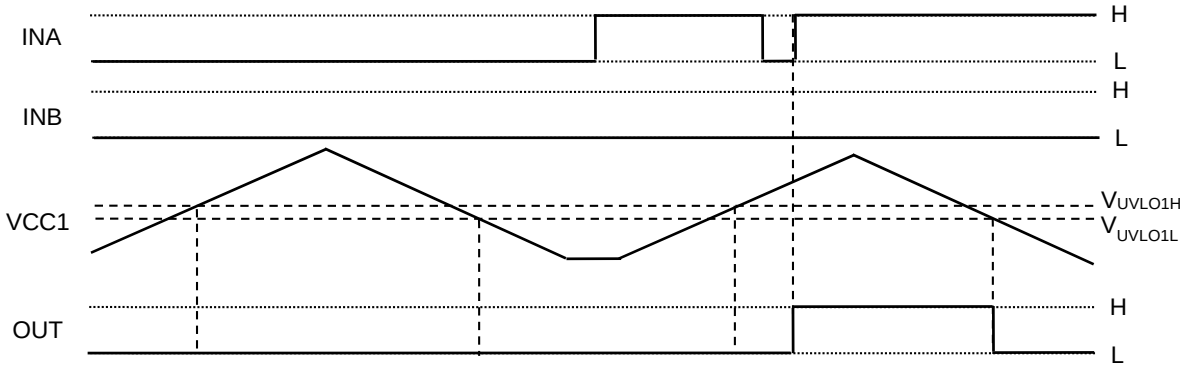


Figure 5. Input-side UVLO Function Operation Timing Chart

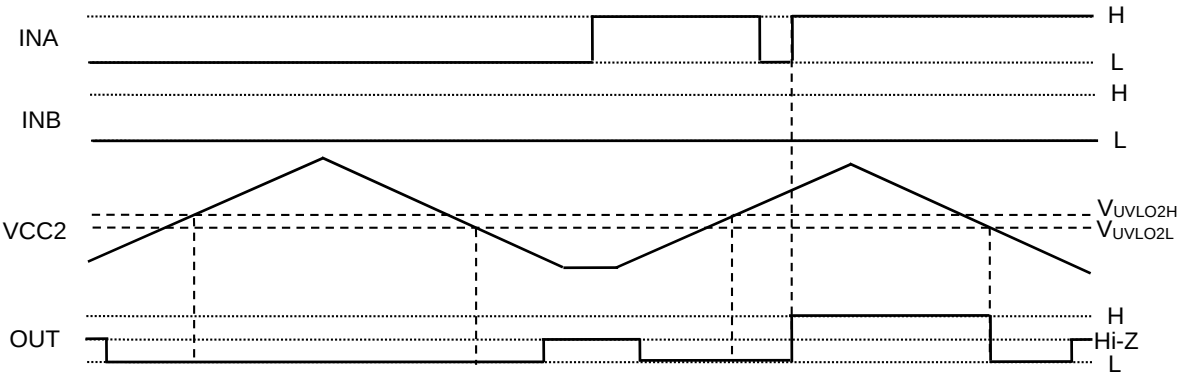


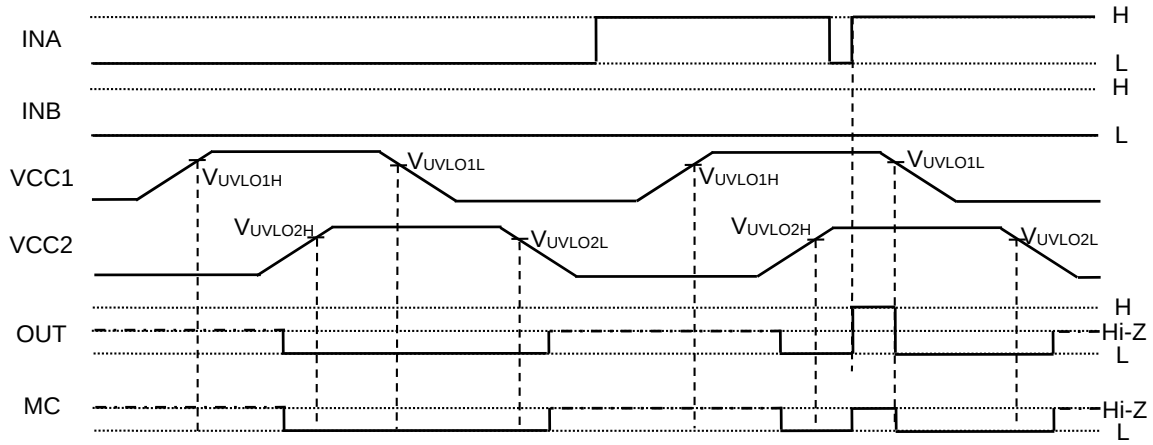
Figure 6. Output-side UVLO Function Operation Timing Chart

3) I/O condition table

No.	Status	Input				Output	
		VCC1	VCC2	INB	INA	OUT	MC
1	VCC1UVLO	UVLO	X	X	X	L	L
2	VCC2UVLO	X	UVLO	X	X	L	L
3	INB Active	○	○	H	X	L	L
4	Normal operation L input	○	○	L	L	L	L
5	Normal operation H input	○	○	L	H	H	Hi-Z

○: VCC1 or VCC2 > UVLO, X:Don't care

4) Power supply startup / shutoff sequence



- - - - - - : Since the VCC2 to GND2 pin voltage is low and the output MOS does not turn ON, the output pins become Hi-Z.

Figure 7. Power Supply Startup / Shutoff Sequence

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side Supply Voltage	V_{CC1}	-0.3～+7.0*(Note 2)*	V
Output-side Supply Voltage	V_{CC2}	-0.3～+30.0*(Note 3)*	V
INA Pin Input Voltage	V_{INA}	-0.3～+VCC1+0.3 or +7.0*(Note 2)*	V
INB Pin Input Voltage	V_{INB}	-0.3～+VCC1+0.3 or +7.0*(Note2)*	V
OUT Pin Output Current (Peak 10μs)	$I_{OUTPEAK}$	5.0*(Note 4)*	A
Operating Temperature Range	Topr	-40～+125	°C
Storage Temperature Range	Tstg	-55～+150	°C
Junction Temperature Range	Tjmax	+150	°C

(Note 2) Relative to GND1.
(Note 3) Relative to GND2.
(Note 4) Should not exceed Tj=150°C
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Thermal Resistance*(Note 5)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 7)*	2s2p*(Note 8)*	
SSOP-B10W				
Input-side Junction to Ambient	θ_{JA1}	172.1	101.8	°C/W
Output-side Junction to Ambient	θ_{JA2}	180.2	108.9	°C/W
Input-side Junction to Top Characterization Parameter*(Note 6)*	Ψ_{JT1}	32	27	°C/W
Input-side Junction to Top Characterization Parameter*(Note 6)*	Ψ_{JT2}	82	60	°C/W

*(Note 5)*Based on JESD51-2A(Still-Air)
*(Note 6)*The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
*(Note 7)*Using a PCB board based on JESD51-3.
*(Note 8)*Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Ratings (Ta= -40°C to +125°C)

Parameter	Symbol	Min.	Max.	Units
Input-side Supply Voltage	V_{CC1} *(Note 9)*	4.5	5.5	V
Output-side Supply Voltage	V_{CC2} *(Note 10)*	10	24	V

(Note 9) Relative to GND1.
(Note 10) Relative to GND2.

Insulation Related Characteristics

Parameter	Symbol	Characteristic	Units
Insulation Resistance (V_{IO}=500V)	R_S	$>10^9$	Ω
Insulation Withstand Voltage / 1min	V_{ISO}	2500	Vrms
Insulation Test Voltage / 1sec	V_{ISO}	3000	Vrms

Electrical Characteristics

(Unless otherwise specified T_a=-40°C to 125°C, V_{CC1}=4.5V to 5.5V, V_{CC2}=10V to 24V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
General						
Input side circuit current 1	I_{CC11}	0.06	0.14	0.22	mA	
Input side circuit current 2	I_{CC12}	0.10	0.20	0.30	mA	INA =10kHz, Duty=50%
Input side circuit current 3	I_{CC13}	0.15	0.30	0.45	mA	INA =20kHz, Duty=50%
Output side circuit current 1	I_{CC21}	0.28	0.46	0.64	mA	OUT=L
Output side circuit current 2	I_{CC22}	0.24	0.42	0.60	mA	OUT=H
Logic block						
Logic high level input voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB
Logic low level input voltage	V_{INL}	0	-	0.8	V	INA, INB
Logic pull-down resistance	R_{IND}	25	50	100	kΩ	INA, INB
Logic input minimum pulse width	t_{INMIN}	60	-	-	ns	INA, INB
Output						
OUT ON resistance (Source)	R_{ONH}	0.4	0.9	2.0	Ω	I_{OUT}=-40mA
OUT ON resistance (Sink)	R_{ONL}	0.2	0.6	1.3	Ω	I_{OUT}=40mA
OUT maximum current (Source)	$I_{OUTMAXH}$	3.0	4.5	-	A	VCC2=15V, Guaranteed by design
OUT maximum current (Sink)	$I_{OUTMAXL}$	3.0	3.9	-	A	VCC2=15V, Guaranteed by design
Turn ON time	t_{PONA}	35	55	75	ns	INA=PWM, INB=L
	t_{PONB}	35	55	75	ns	INA=H, INB=PWM
Turn OFF time	t_{POFFA}	35	55	75	ns	INA=PWM, INB=L
	t_{POFFB}	35	55	75	ns	INA=H, INB=PWM
Propagation distortion	t_{PDISTA}	-25	0	25	ns	$t_{POFFA} - t_{PONA}$
	t_{PDISTB}	-25	0	25	ns	$t_{POFFB} - t_{PONB}$
Rise time	t_{RISE}	-	50	-	ns	10nF between OUT-GND2
Fall time	t_{FALL}	-	50	-	ns	10nF between OUT-GND2
MC ON resistance	R_{ONMC}	0.20	0.65	1.40	Ω	I_{MC}=40mA
MC ON threshold voltage	V_{MCON}	1.8	2	2.2	V	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by design
Protection functions						
VCC1 UVLO OFF voltage	V_{UVLO1H}	3.35	3.50	3.65	V	
VCC1 UVLO ON voltage	V_{UVLO1L}	3.25	3.40	3.55	V	
VCC1 UVLO mask time	$t_{UVLO1MSK}$	1.0	2.5	5.0	µs	
VCC2 UVLO OFF voltage	V_{UVLO2H}	9.0	9.5	10.0	V	
VCC2 UVLO ON voltage	V_{UVLO2L}	8.0	8.5	9.0	V	
VCC2 UVLO mask time	$t_{UVLO2MSK}$	1.00	2.9	5.00	µs	

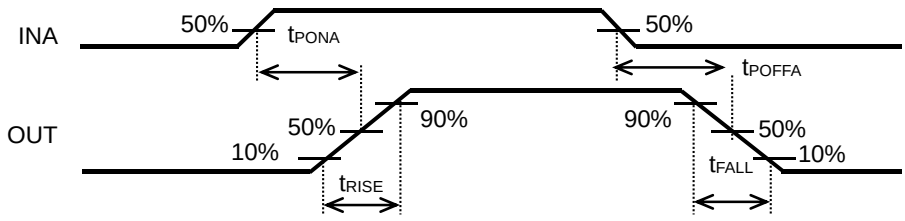


Figure 8. IN-OUT Timing Chart

Typical Performance Curves

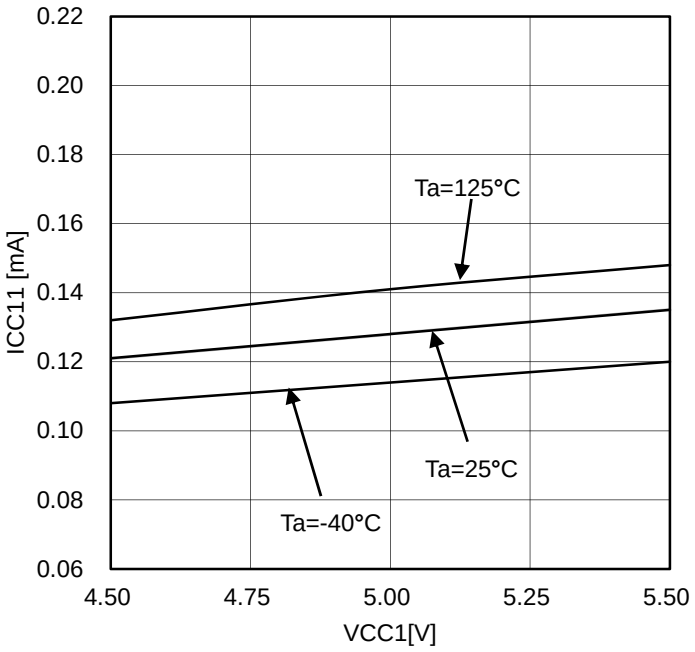


Figure 9. Input Side Circuit Current 1

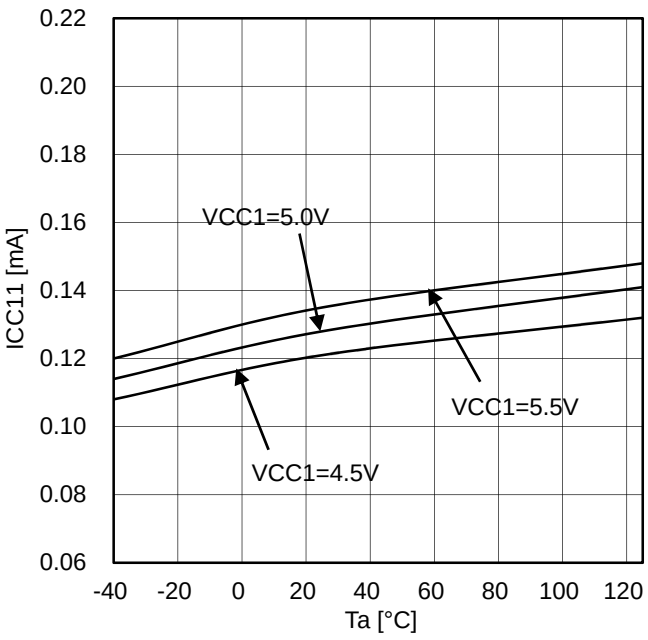


Figure 10. Input Side Circuit Current 1

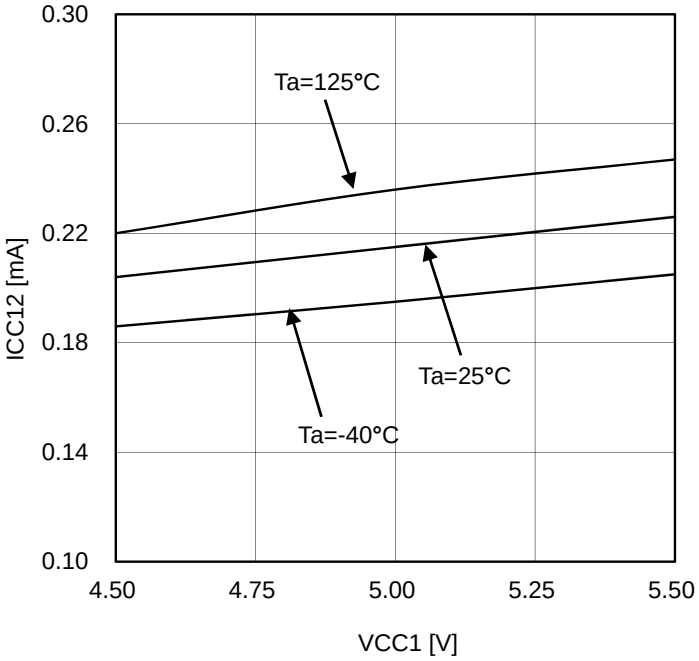


Figure 11. input Side Circuit Current 2
(at INA=10kHz, Duty=50%)

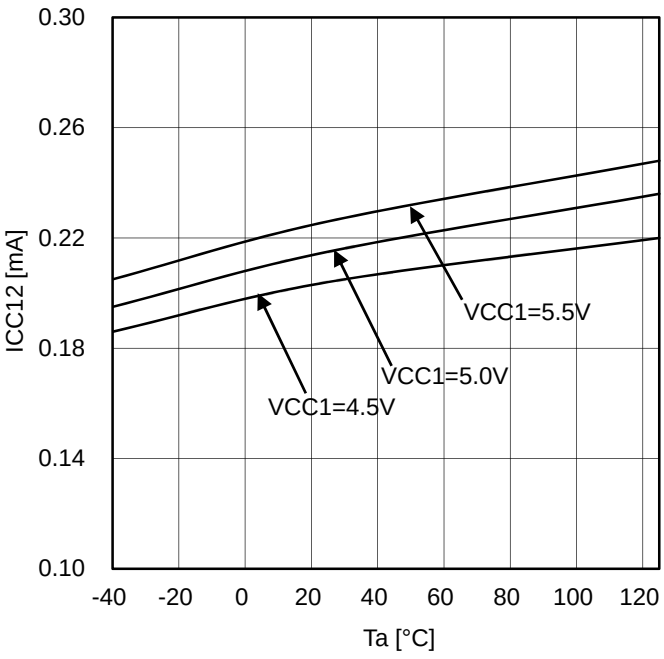


Figure 12. Input Side Circuit Current 2
（at INA=10kHz, Duty=50%）

Typical Performance Curves - continued

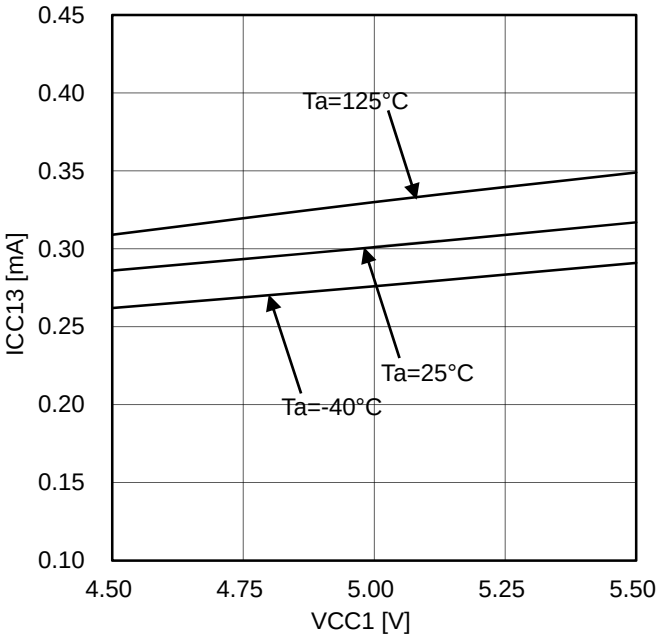


Figure 13. Input Side Circuit Current 3
(at INA=20kHz, Duty=50%)

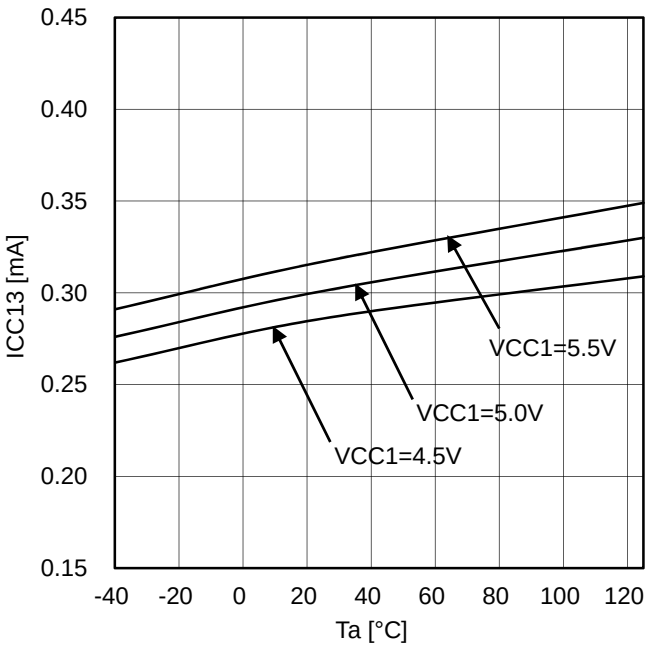


Figure 14. Input Side Circuit Current 3
（at INA=20kHz, Duty=50%）

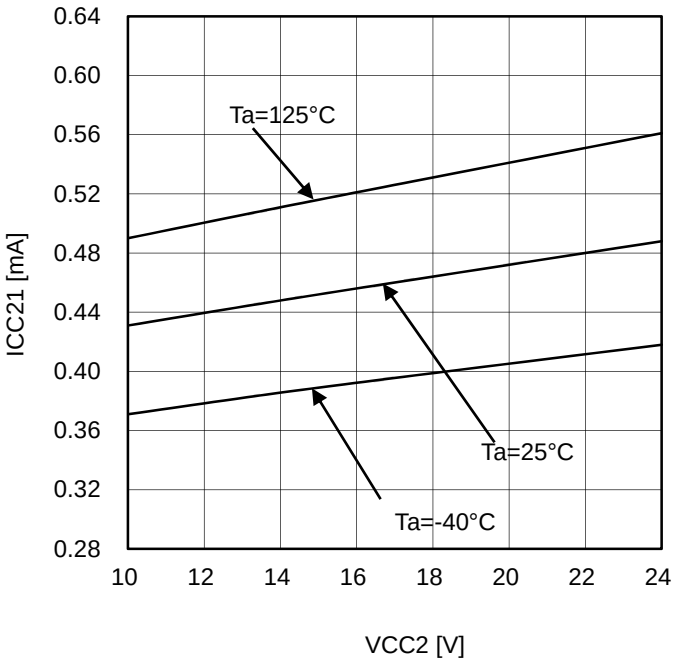


Figure 15. Output Side Circuit Current 1
(at OUT=L)

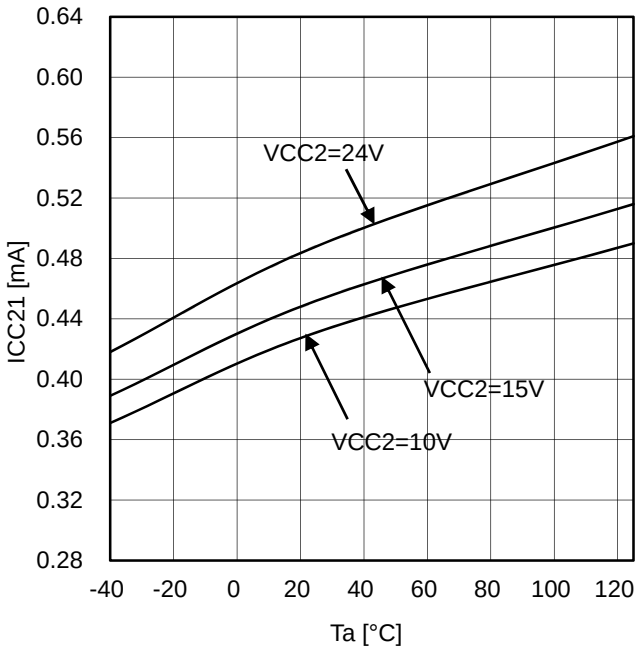


Figure 16. Output Side Circuit Current 1
（at OUT=L）

Typical Performance Curves - continued

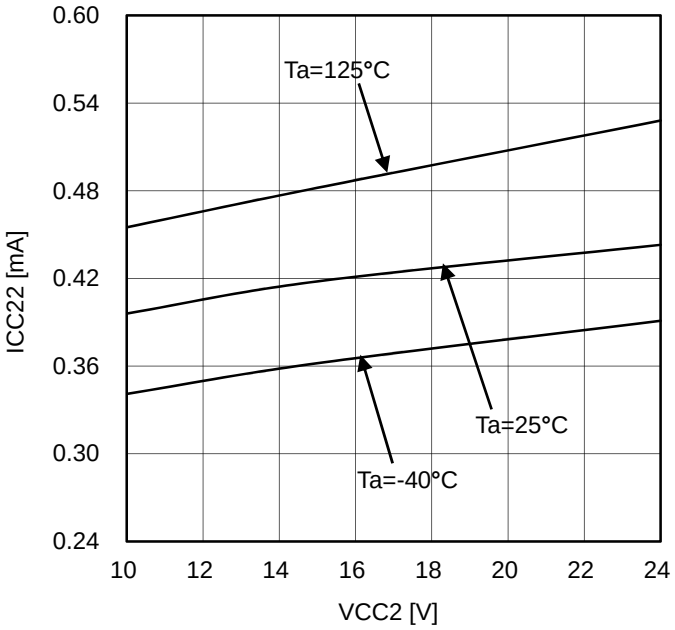


Figure 17. Output Side Circuit Current 2
(at OUT=H)

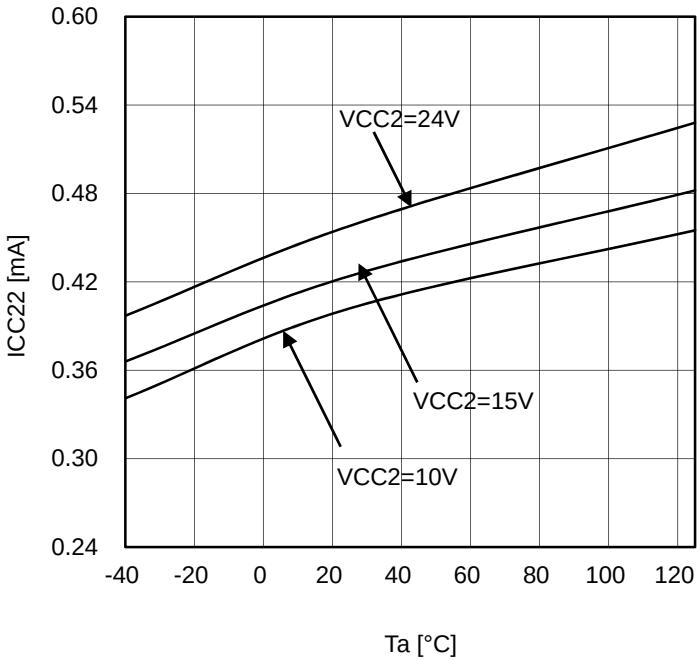


Figure 18. Output Side Circuit Current 2
(at OUT=H)

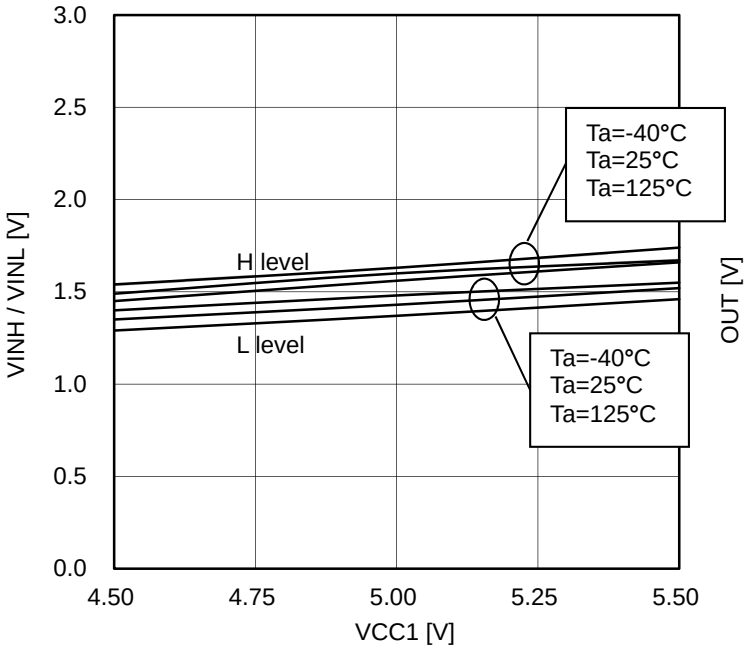


Figure 19. Logic (INA/INB) High/Low Level Voltage

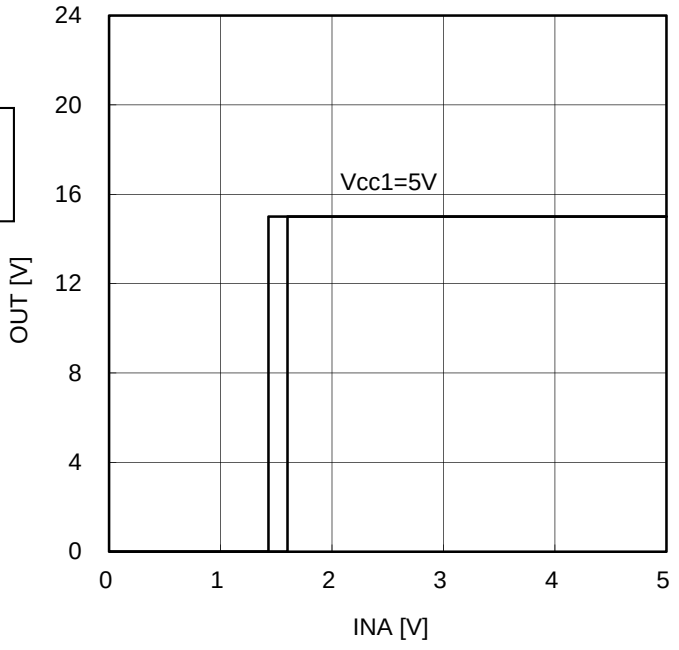


Figure 20. OUT vs Logic (INA) Input Voltage
（VCC1=5V, VCC2=15V, Ta=25°C）

Typical Performance Curves - continued

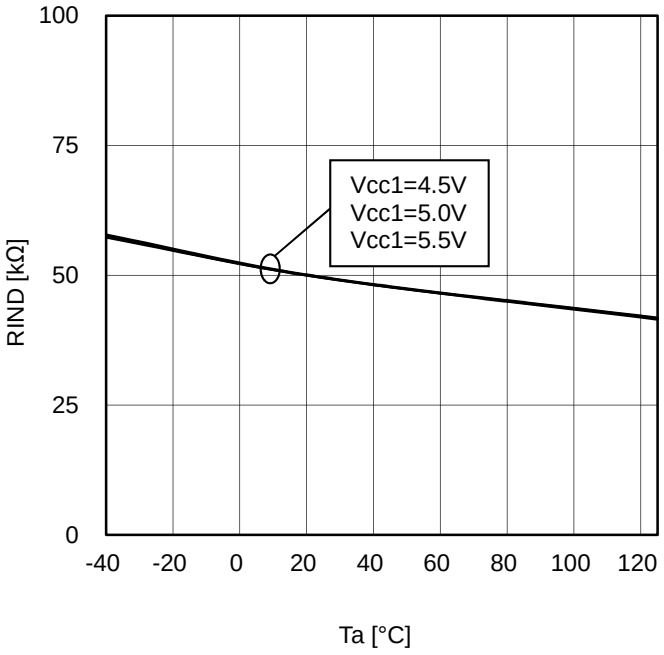


Figure 21. Logic Pull-down Resistance

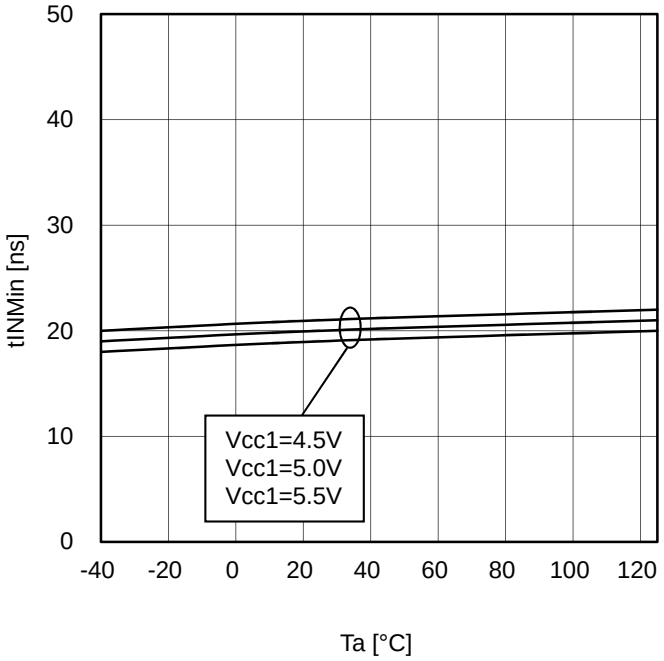


Figure 22. Logic (INA) Input Minimum Pulse Width

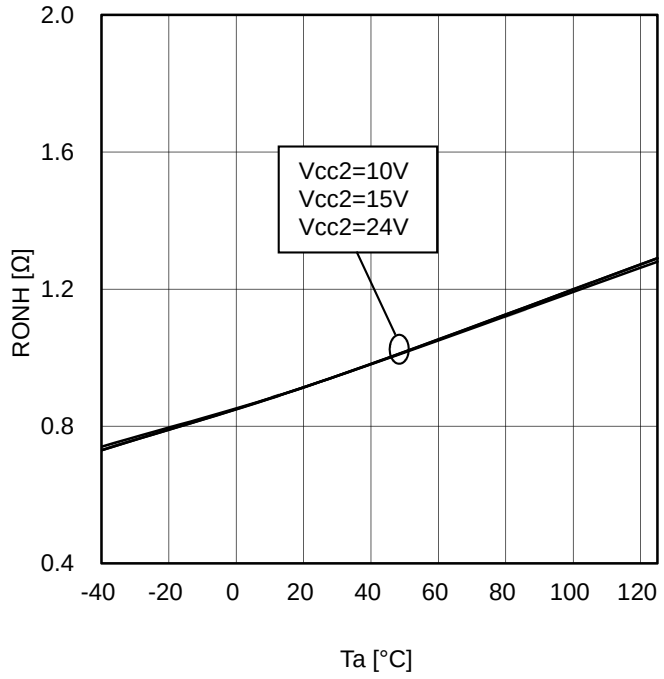


Figure 23. OUT ON Resistance (Source)

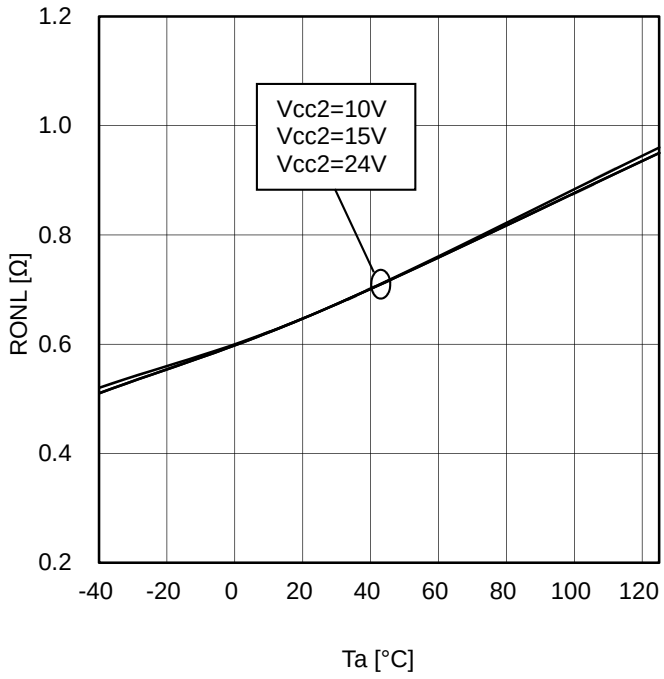


Figure 24. OUT ON Resistance (Sink)

Typical Performance Curves - continued

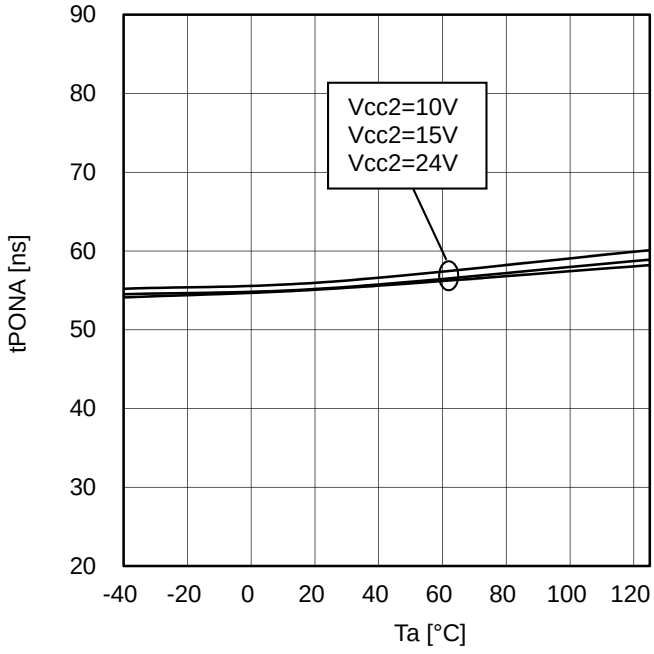


Figure 25. Turn ON Time
（INA=PWM, INB=L）

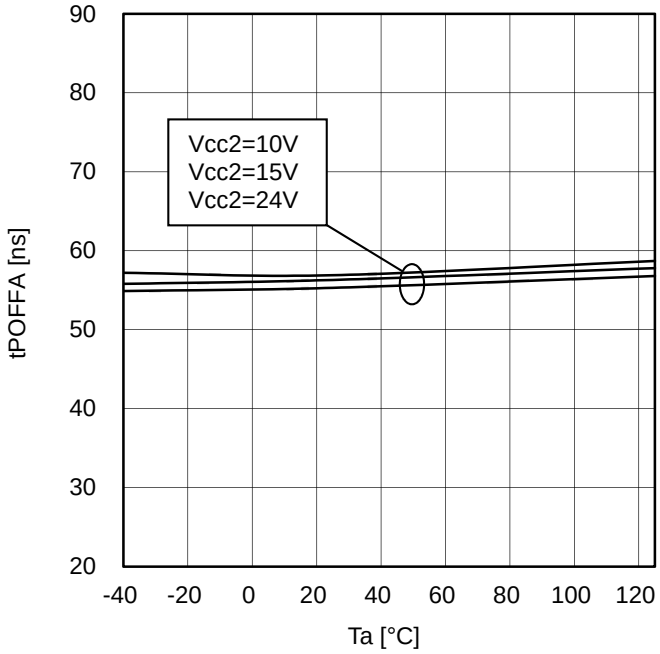


Figure 26. Turn OFF Time
（INA=PWM, INB=L）

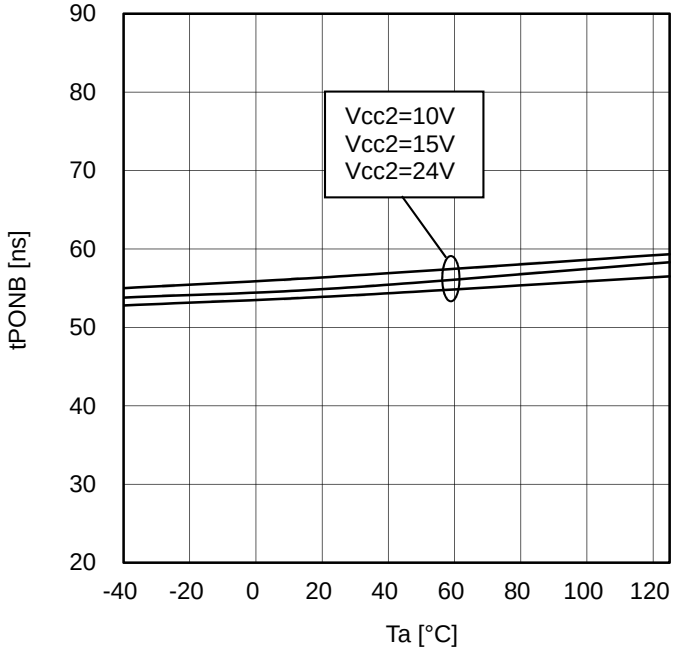


Figure 27. Turn ON Time
(INA=H, INB=PWM）

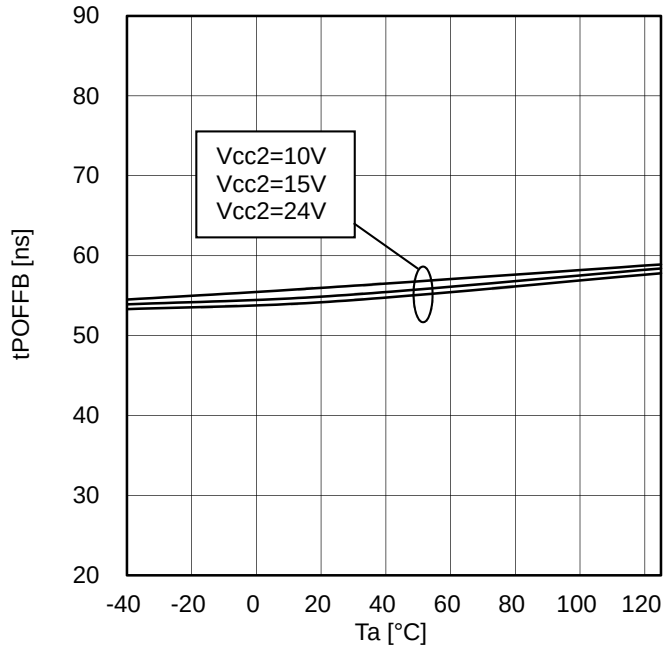


Figure 28. Turn OFF Time
（INA=H, INB=PWM）

Typical Performance Curves - continued

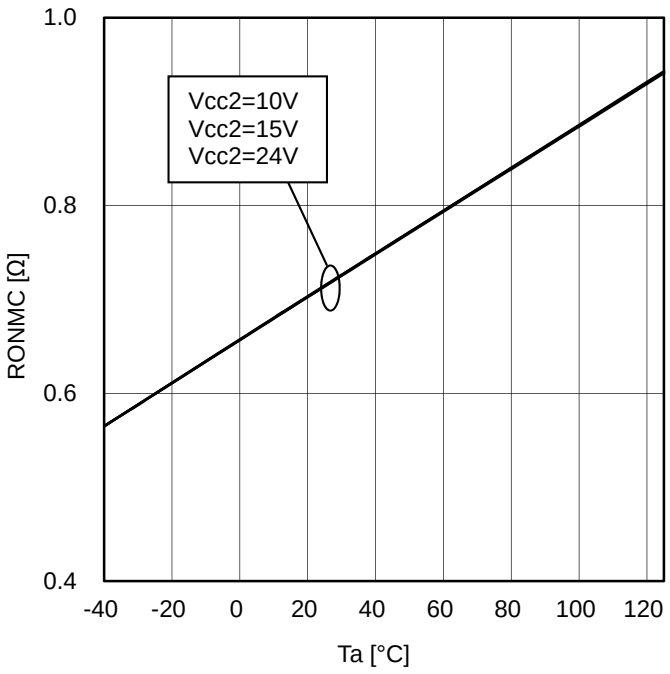


Figure 29. MC ON Resistance

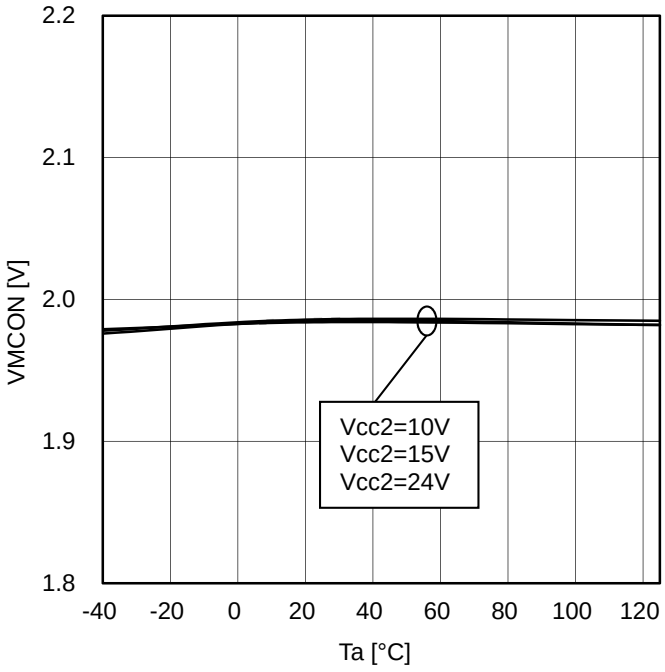


Figure 30. MC ON Threshold Voltage

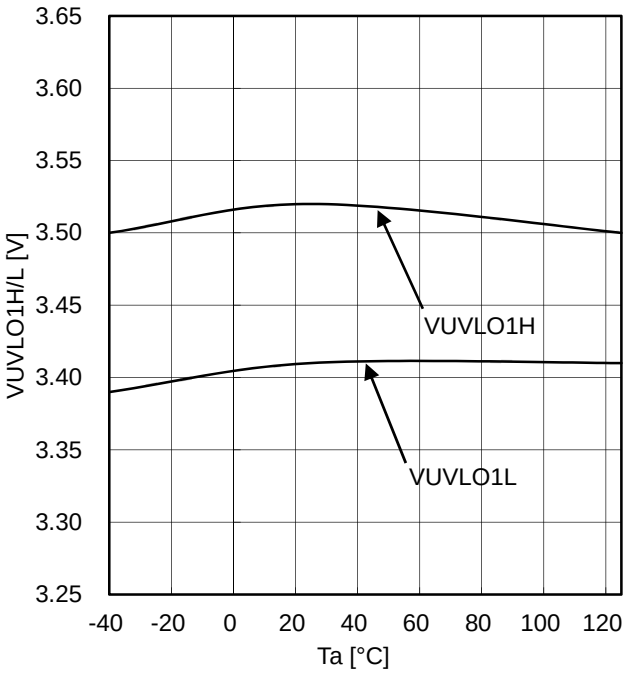


Figure 31. Input Side UVLO ON/OFF Voltage

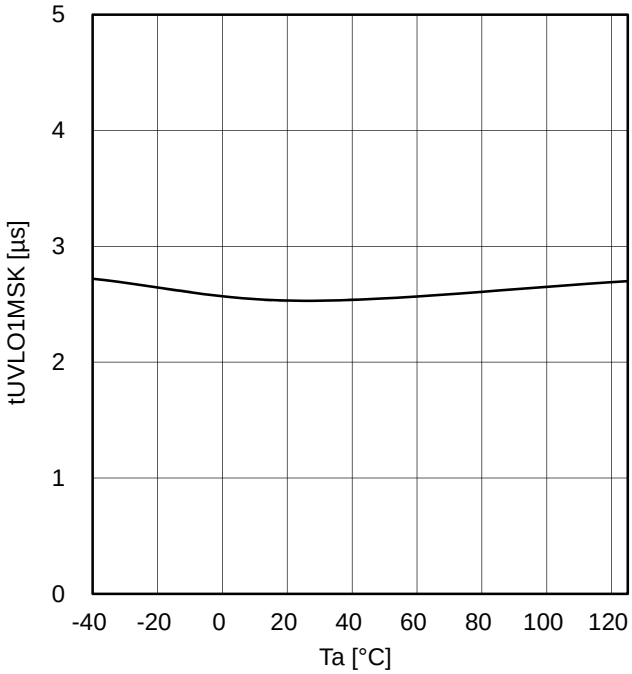


Figure 32. Input Side UVLO Mask Time

Typical Performance Curves - continued

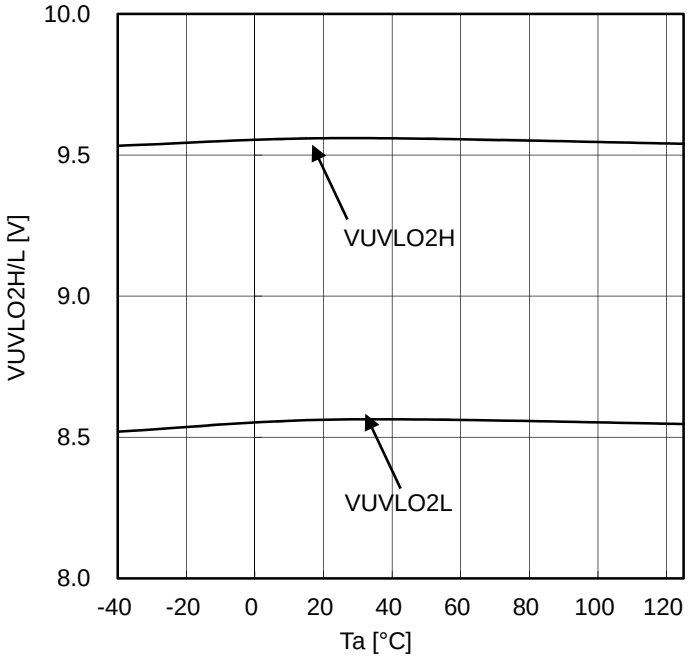


Figure 33. Output Side UVLO ON/OFF voltage

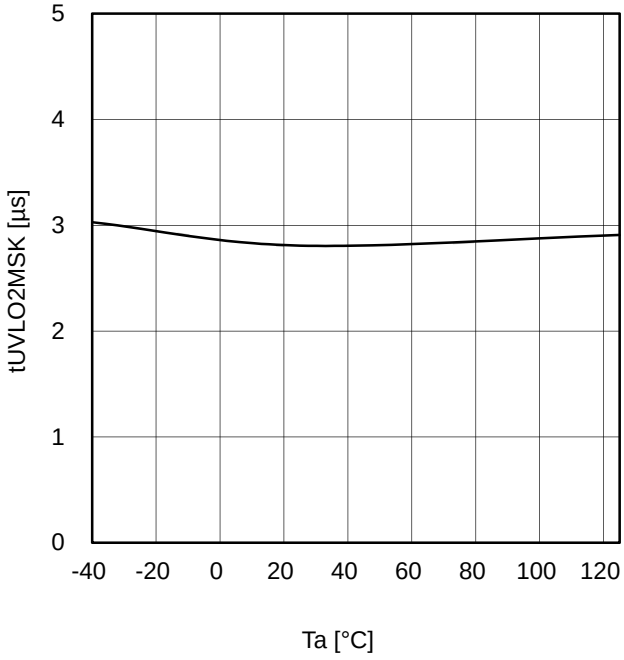


Figure 34. Output Side UVLO Mask Time

Selection of Components Externally Connected

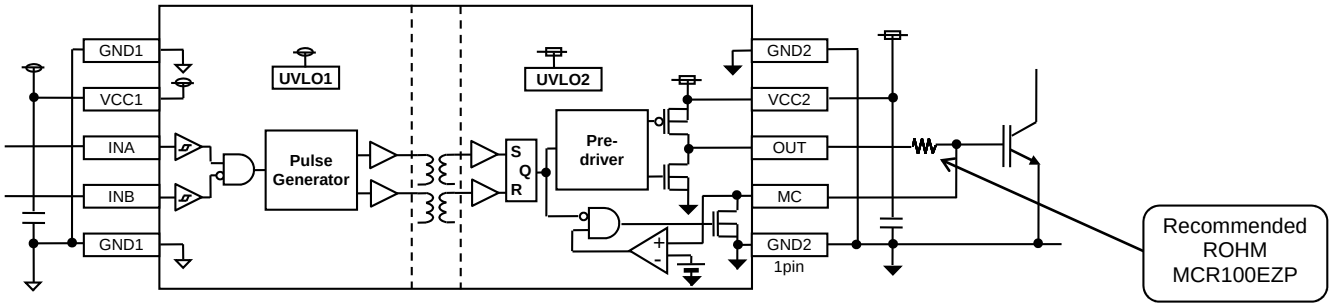


Figure 35. For Driving IGBT

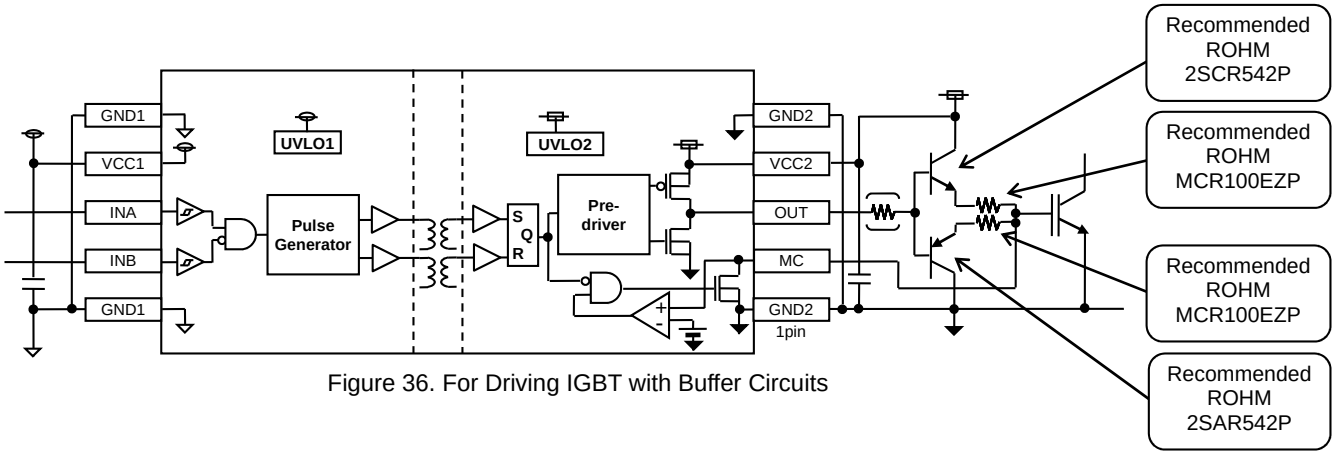


Figure 36. For Driving IGBT with Buffer Circuits

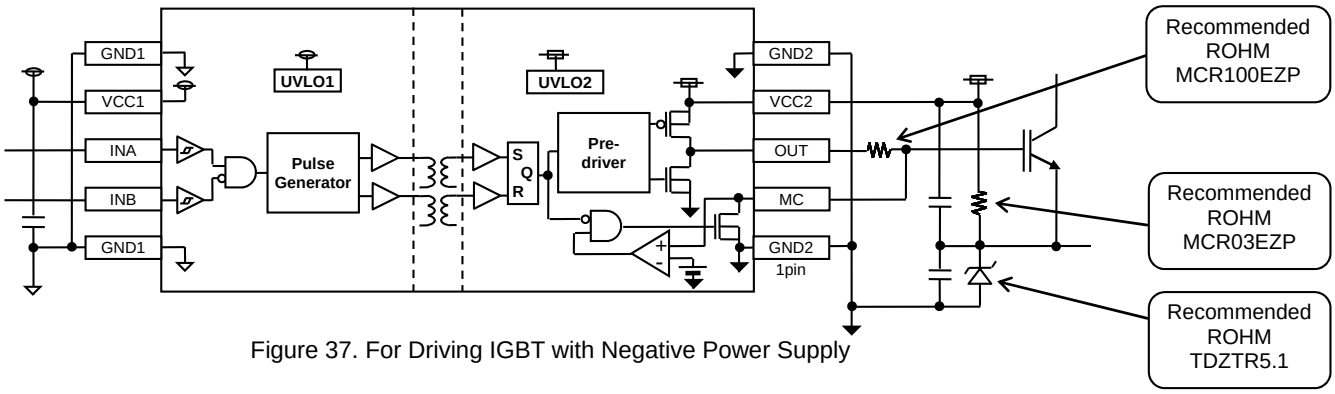


Figure 37. For Driving IGBT with Negative Power Supply

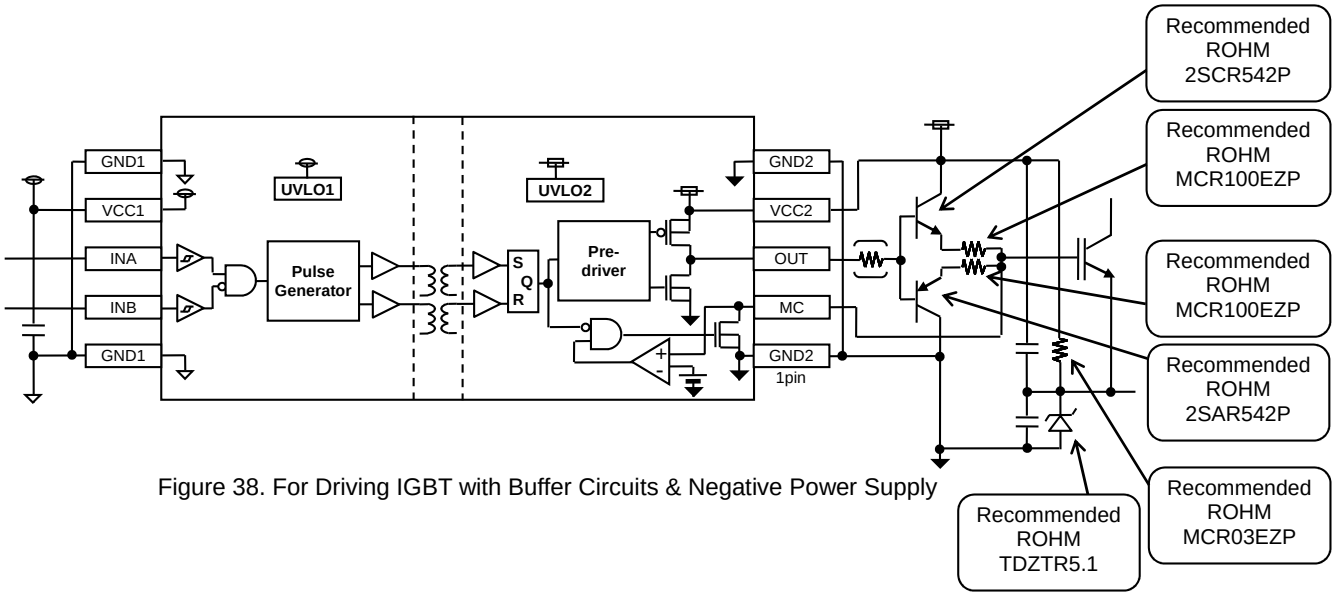


Figure 38. For Driving IGBT with Buffer Circuits & Negative Power Supply

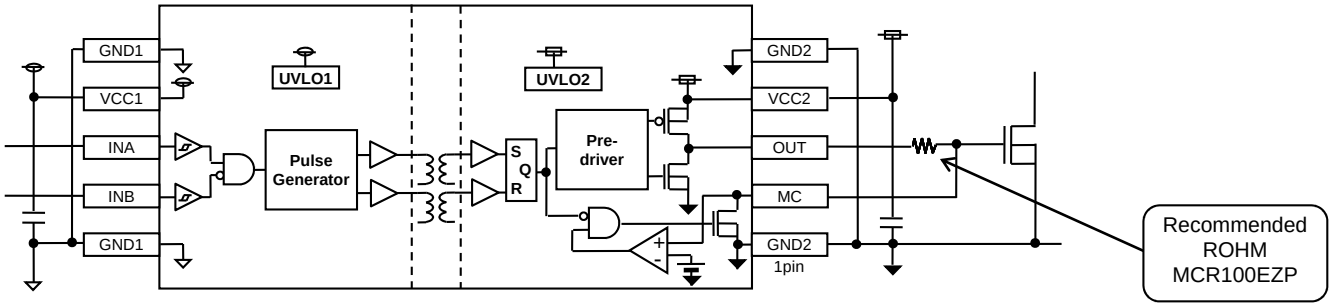


Figure 39. For Driving MOSFET

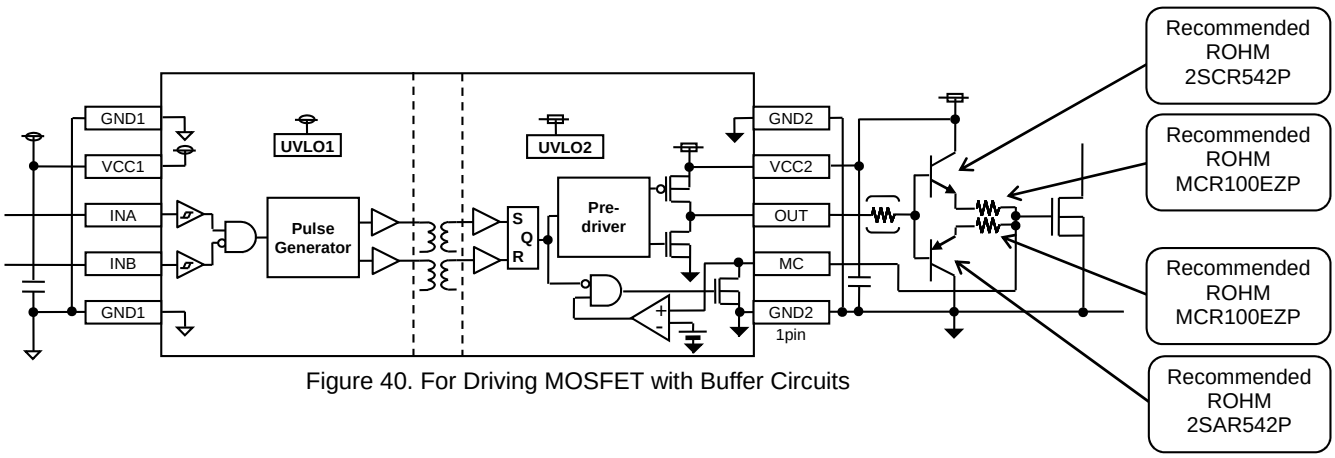


Figure 40. For Driving MOSFET with Buffer Circuits

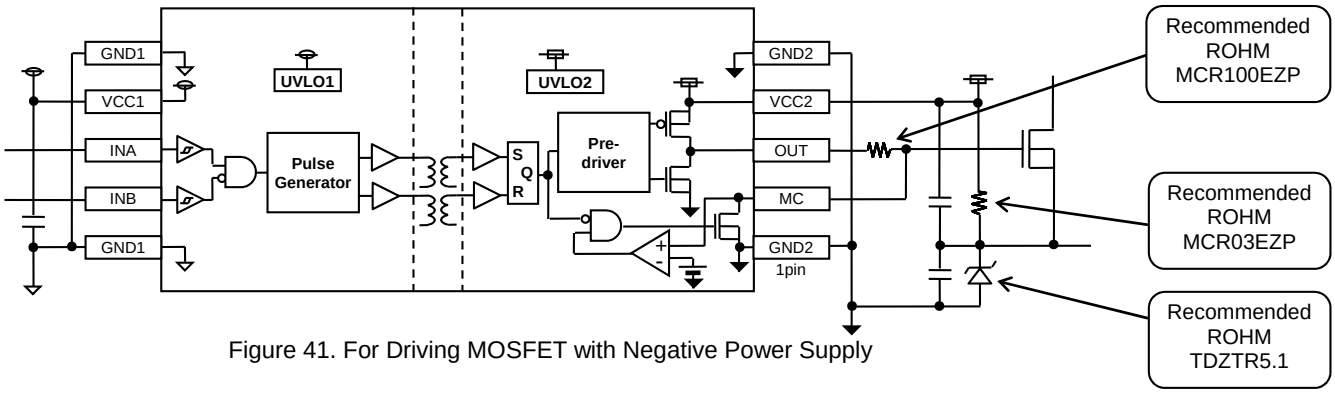


Figure 41. For Driving MOSFET with Negative Power Supply

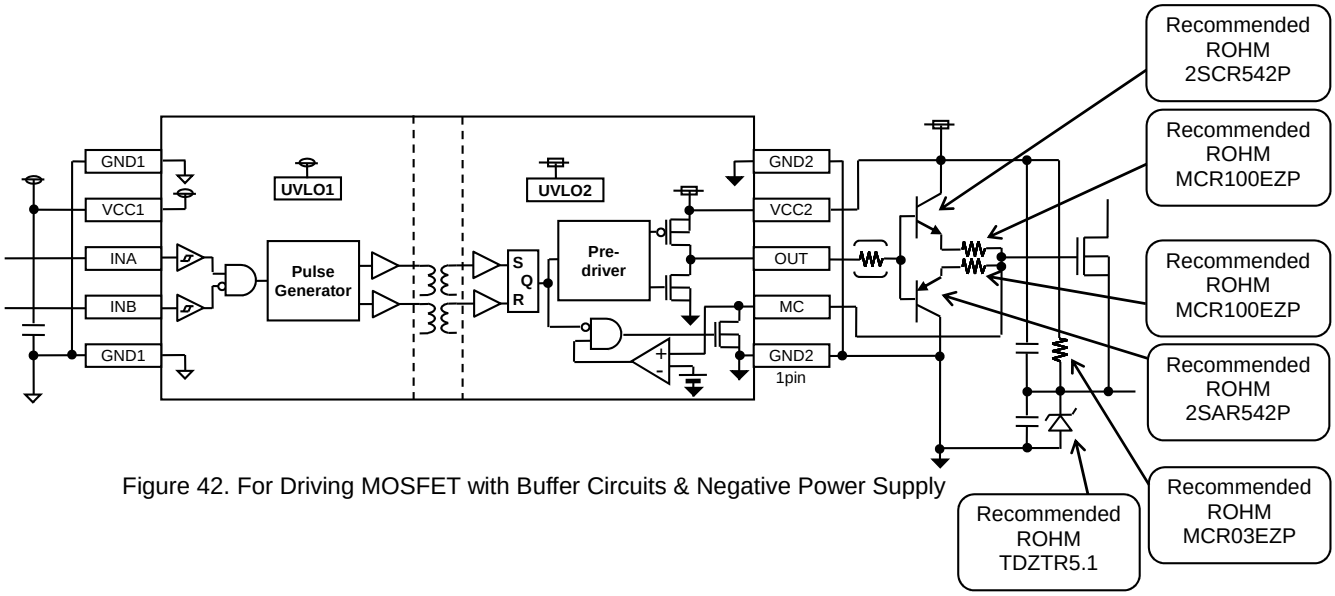
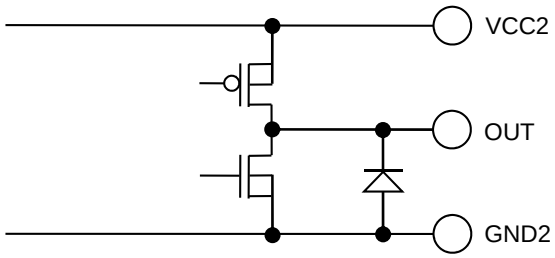
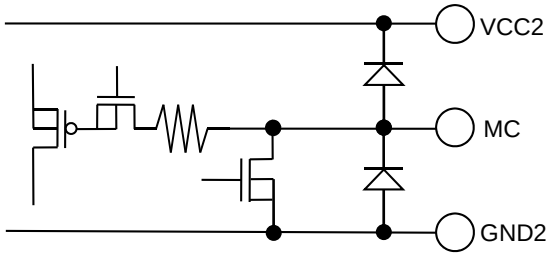
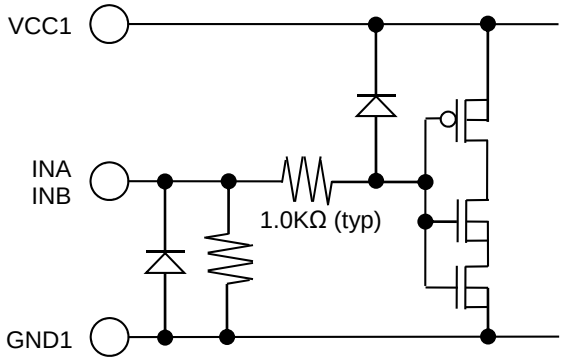


Figure 42. For Driving MOSFET with Buffer Circuits & Negative Power Supply

I/O Equivalent Circuits

Pin No	Name / Function	I/O equivalence circuits
1	OUT / Output pin	
2	MC / Miller clamp pin	
3	INA / Control input pin A / INB / Control input pin B	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Terminals

Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

12. Regarding Input Pins of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

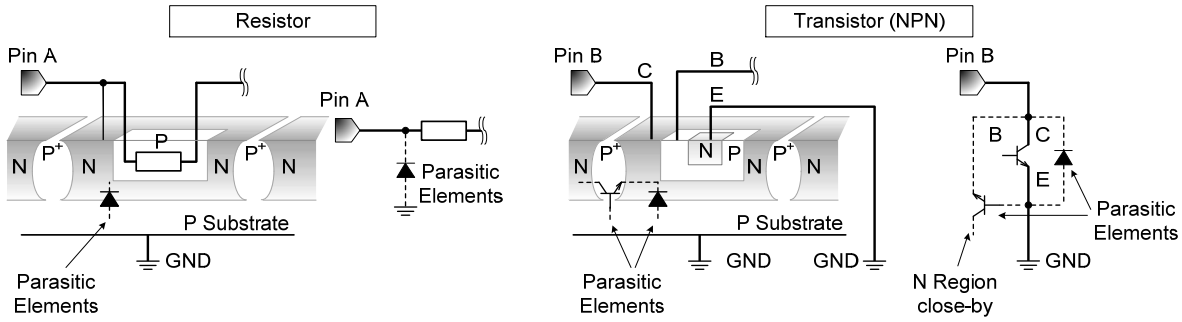


Figure 43. Example of IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

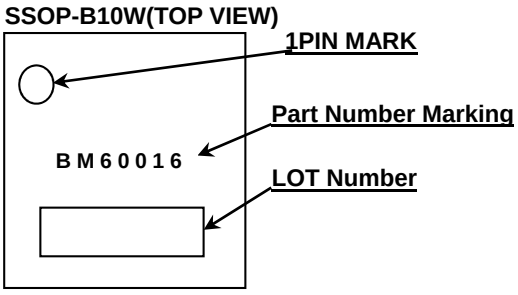
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

Ordering Information

B M 6 0 0 1 6 F V	-	CE2

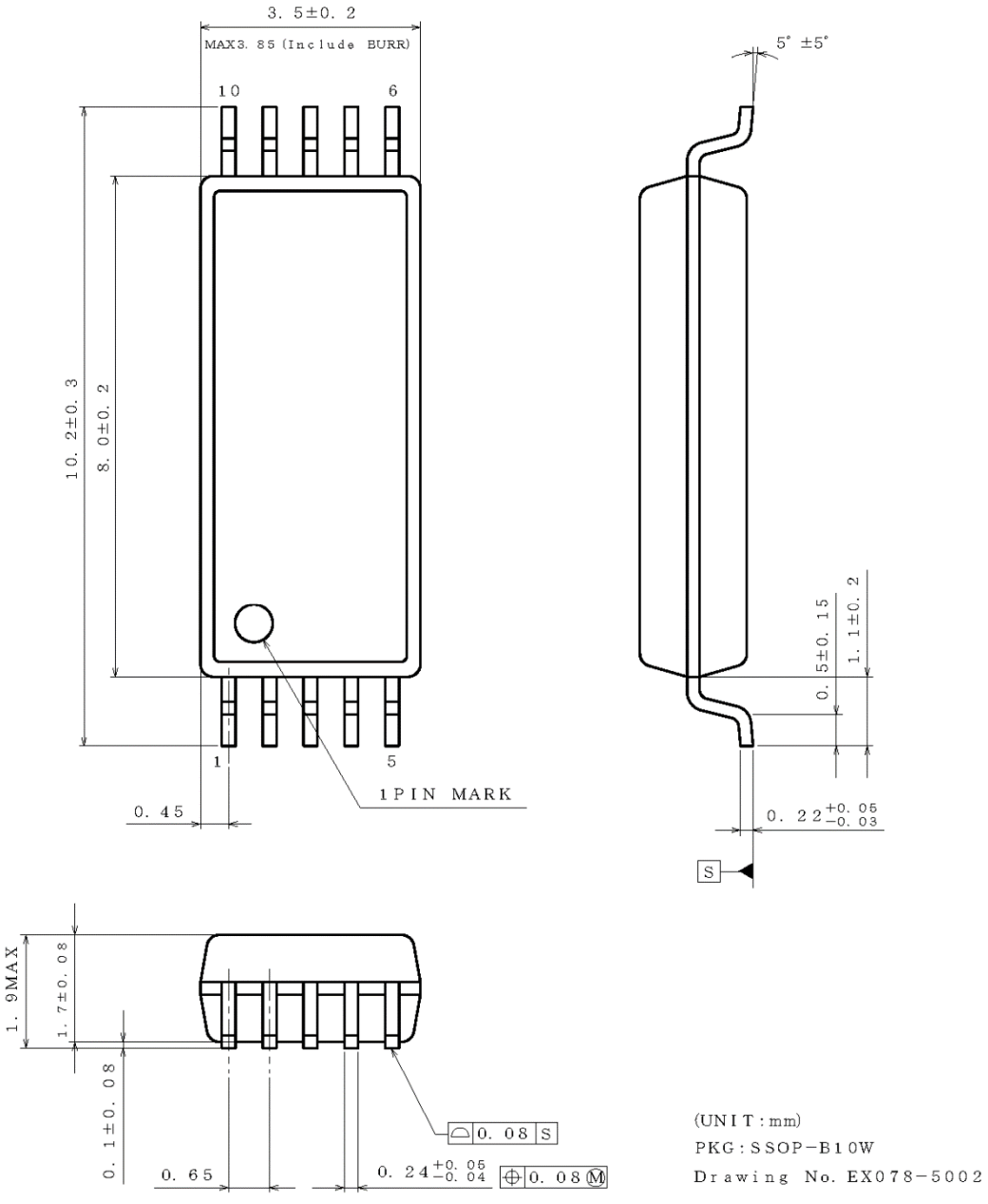
- Part Number
- Package
  FV:SSOP-B10W
- Product class
  C : for Automotive applications
  Packaging and forming specification
  E2: Embossed tape and reel

Marking Diagrams



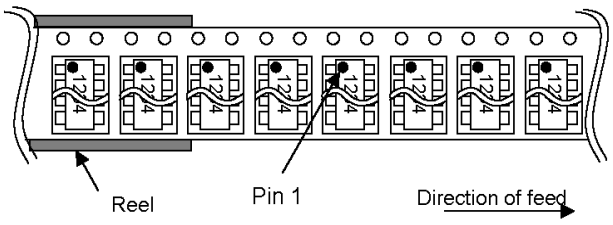
Physical Dimension, Tape and Reel Information

Package Name	SSOP-B10W



< Tape and Reel Information >

Tape	Embossed carrier tape with dry pack
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
30.May.2015	001	New Release

Notice

Precaution on using ROHM Products

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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BM60016FV-C - Web Page

Part Number	BM60016FV-C
Package	SSOP-B10W
Unit Quantity	1500
Minimum Package Quantity	1500
Packing Type	Taping
Constitution Materials List	inquiry
RoHS	Yes

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