2.5V to 5.5V, Integrated 2.0A MOSFET 2ch Buck-Boost Converter

BD8305MUV

General Description

ROHM's highly-efficient buck-boost converter IC. BD8305MUV produces buck-boost output including 3.3V from 1 cell of lithium battery with just one coil. This IC adopts an original buck-boost drive system and creates a more efficient power supply than conventional SEPIC-system or H-bridge system converters.

Features

- Highly-Efficient Buck-Boost DC/DC Converter Implemented with Just One Inductor.
- Incorporates a Soft-Start Function.
- Incorporates a Timer Latch System with Short-Circuit Protection Function.

Applications

General Portable Equipment

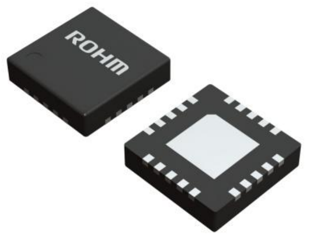
- Portable Audio
- DSC
- DVC

Key Specifications

■ Input Voltage Range:	+2.5V to +5.5V
■ Output Voltage Range:	+2.8V to +5.2V
■ Output Current:	1.0A at 3.3V 0.8A at 5.0V
■ Switching Frequency:	1MHz(Typ)
■ Pch FET ON-Resistance:	120mΩ(Typ)
■ Nch FET ON-Resistance:	100mΩ(Typ)
■ Standby Current:	0μA (Typ)
■ Operating Temperature Range:	-25°C to +85°C

Package

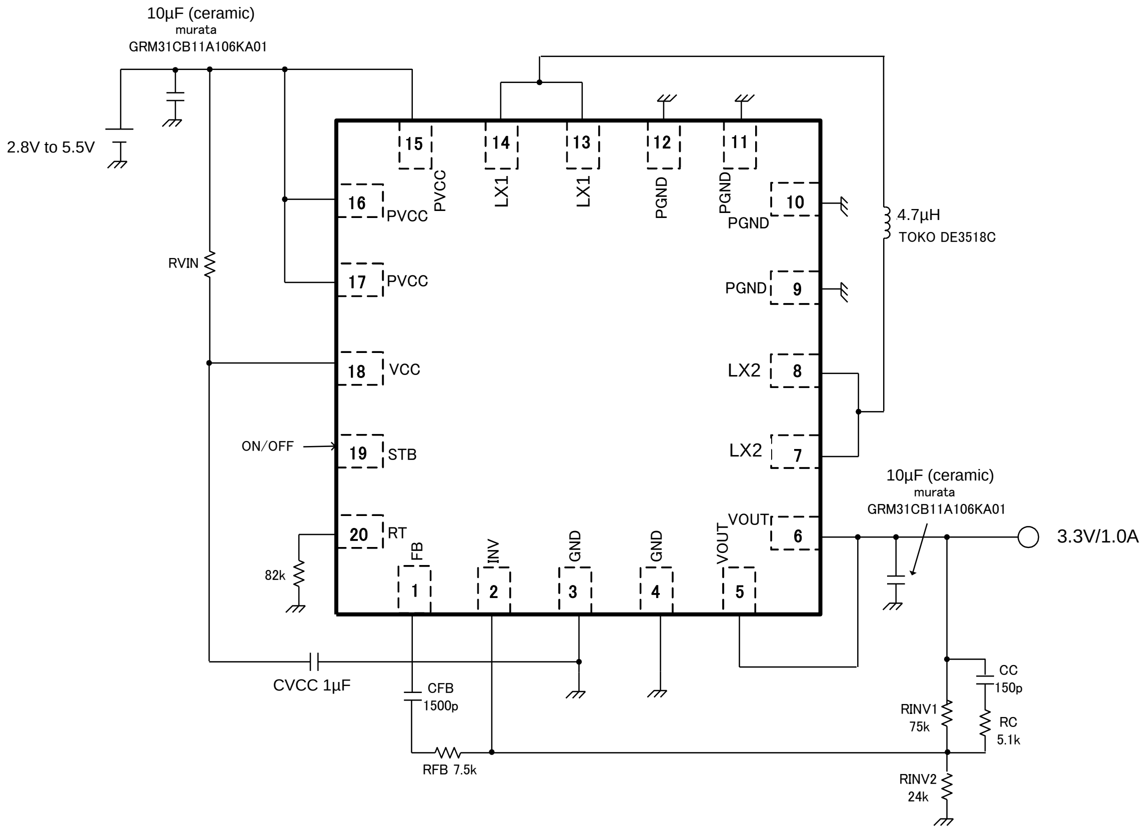
W(Typ) x D(Typ) x H(Max)



VQFN020V4040
4.00mm x 4.00mm x 1.00mm

Typical Application Circuit

Input: 2.8V to 5.5V, Output: 3.3 V / 1.0 A, Frequency 600 kHz



〇Product structure：Silicon monolithic integrated circuit 〇This product has no designed protection against radioactive rays

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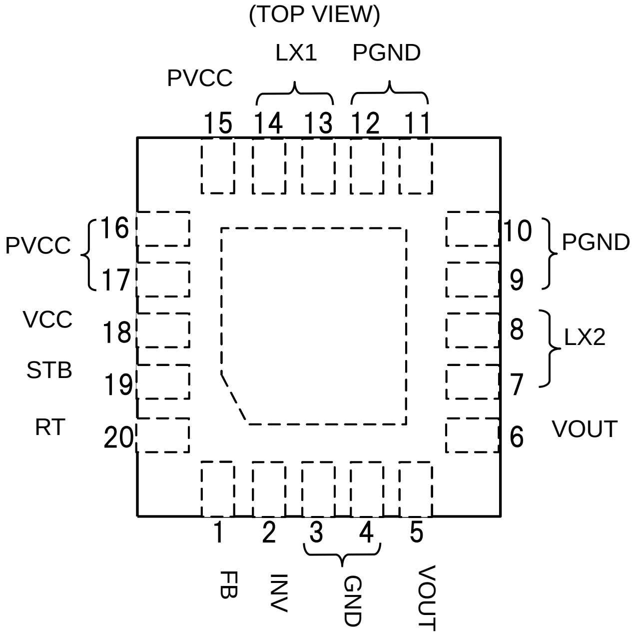
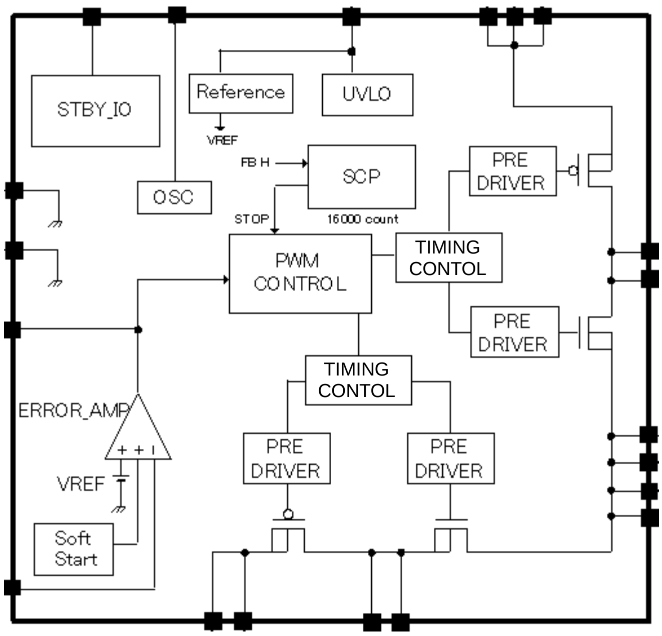
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	FB	Error AMP output terminal
2	INV	Error AMP input terminal
3 to 4	GND	Ground terminal
5 to 6	VOUT	Output voltage terminal
7 to 8	LX2	Output side coil connecting terminal
9 to 12	PGND	Power transistor ground terminal
13 to 14	LX1	Input side coil connecting terminal
15 to 17	PVCC	DC/DC converter input terminal
18	VCC	Control part power supply input terminal
19	STB	ON/OFF terminal
20	RT	Oscillation frequency set terminal

Block Diagram



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Description of Blocks

1. VREF
   This block generates ERROR AMP reference voltage. The reference voltage is set at 0.8V.

2. UVLO
   Circuit for preventing low voltage malfunction
   Prevents malfunction of the internal circuit at activation of the power supply voltage or at low power supply voltage.
   Monitors VCC pin voltage to turn OFF all output FET and DC/DC converter output when VCC voltage is lower than 2.2V, and reset the timer latch of the internal SCP circuit and soft-start circuit.

3. SCP
   Timer latch system short circuit protection circuit
   When the INV pin is set to 0.8V or lower voltage, the internal SCP circuit starts counting.
   The internal counter is in-synch with OSC, the latch circuit activates after the counter counts about 8200 pulses to turn OFF DC/DC converter output (about 8.2msec when R_{RT} =47kΩ).
   To reset the latch circuit, turn OFF the STB pin once. Then, turn it ON again or turn ON the power supply voltage again.

4. OSC
   Oscillation circuit that changes the operating frequency by external resistance of the RT pin (Pin 20).
   When R_{RT} = 47kΩ, operation frequency is set at 1MHz.

5. ERROR AMP
   Error amplifier for detecting output signals and output PWM control signals.
   The internal reference voltage is set at 0.8V.

6. PWM COMP
   Voltage-pulse width converter for controlling output voltage corresponding to input voltage.
   Comparing the internal SLOPE waveform with the ERROR AMP output voltage, PWM COMP controls the pulse width and outputs to the driver.
   Max Duty and Min Duty are set at the primary side and the secondary side of the inductor respectively, which are as follow:

Primary Side (LX1)	Max Duty	:	100%,
	Min Duty	:	0%
Secondary Side (LX2)	Max Duty	:	100%,
	Min Duty	:	About 15%

7. SOFT START
   Circuit for preventing in-rush current at startup by bringing the output voltage of the DC/DC converter into a soft-start
   Soft-start time is in-synch with the internal OSC, and the output voltage of the DC/DC converter reaches the set voltage after about 1000 pulses (About 1msec when R_{RT} = 47kΩ).

8. PRE DRIVER
   CMOS inverter circuit for driving the built-in Pch/Nch FET. Dead time is provided for preventing feed-through during switching. The dead time is set at about 15nsec for each individual SWs.

9. STBY_IO
   Voltage applied on STB pin (Pin 19) to control ON/OFF of IC.
   Turned ON when a voltage of 1.5V or higher is applied and turned OFF when the terminal is open or 0V is applied.
   Incorporates approximately 400kΩ pull-down resistance.

10. Pch/Nch FET SW
    Built-in FET SW for switching the coil current of the DC/DC converter. Pch FET is about 120mΩ and Nch is 100mΩ.
    Since the current rating of this FET is 2A, it should be used within a range of 1.6A in total including the DC current and ripple current of the coil.

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Maximum Applied Power Voltage	V_{CC},PV_{CC}	7.0	V
Maximum Input Current	I_{INMAX}	2.0	A
Maximum Input Voltage	V_{LX1}	7.0	V
	V_{LX2}	7.0	V
Power Dissipation	Pd	0.70 (Note 1)	W
Storage Temperature Range	Tstg	-55 to +150	ºC
Junction Temperature	Tjmax	150	ºC

(Note 1) When installed on a 70.0 mm x 70.0 mm x 1.6 mm glass epoxy board. The rating is reduced by 5.6 mW/°C at Ta = 25°C or more.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Power Supply Voltage Range	V_{CC}	+2.5 to +5.5	V
Output Voltage Range	V_{OUT}	+2.8 to +5.2	V
Operating Temperature Range	Topr	-25 to +85	ºC

Electrical Characteristics (Unless otherwise specified, Ta = 25°C, V_{CC} = 3.7V)

Parameter		Symbol	Limit Min	Limit Typ	Limit Max	Unit	Conditions
[UVLO]							
Threshold Voltage Detection		V_{UV}	-	2.25	2.45	V	VCC monitor
Hysteresis Range		ΔV_{UVHY}	50	100	150	mV	
[Oscillator]							
Oscillation Frequency		f_{OSC}	0.8	1.0	1.2	MHz	R_{RT}=47kΩ
[Error AMP]							
INV Threshold Voltage		V_{INV}	0.790	0.800	0.810	V	
Input Bias Current		I_{INV}	-50	0	+50	nA	V_{CC}=7.0V , V_{INV}=3.5V
Soft-Start Time		t_{SS}	0.6	1.00	1.4	msec	R_{RT}=47kΩ
Output Source Current		I_{EO}	10	20	30	µA	V_{INV}=0.5V , V_{FB} =1.5V
Output Sink Current		I_{EI}	0.7	1.5	3.0	mA	V_{INV}=1.1V , V_{FB} =1.5V
[PWM Comparator]							
LX1 Max Duty		D_{MAX1}	-	-	100	%	
LX2 Max Duty		D_{MAX2}	77	85	93	%	
[Output]							
LX1 PMOS ON-Resistance		R_{ON1P}	-	120	200	mΩ	V_{GS}=3.0V
LX1 NMOS ON-Resistance		R_{ON1N}	-	100	160	mΩ	V_{GS}=3.0V
LX2 PMOS ON-Resistance		R_{ON2P}	-	120	200	mΩ	V_{GS}=3.0V
LX2 NMOS ON-Resistance		R_{ON2N}	-	100	160	MΩ	V_{GS}=3.0V
LX1 OCP Threshold		I_{OCP}	1.6	2.4	-	A	PV_{CC}=3.0V
LX1 Leak Current		I_{LEAK1}	-1	0	+1	µA	
LX2 Leak Current		I_{LEAK2}	-1	0	+1	µA	
[STB]							
STB Pin Control Voltage	Enable	V_{STBH}	1.5	-	5.5	V	
	Disable	V_{STBL}	-0.3	-	+0.3	V	
STB Pin Pull-Down Resistance		R_{STB}	250	400	700	kΩ	
[Circuit Current]							
Standby Current	VCC Pin	I_{STB1}	-	-	1	µA	
	PVCC Pin	I_{STB2}	-	-	1	µA	
	VOUT Pin	I_{STB3}	-	-	1	µA	
VCC Circuit Current		I_{CC1}	-	500	750	µA	V_{INV}=1.2V
PVCC Circuit Current		I_{CC2}	-	10	20	µA	V_{INV}=1.2V

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Typical Performance Curves

(Unless otherwise specified, Ta = 25°C, V_{CC} = 3.7V)

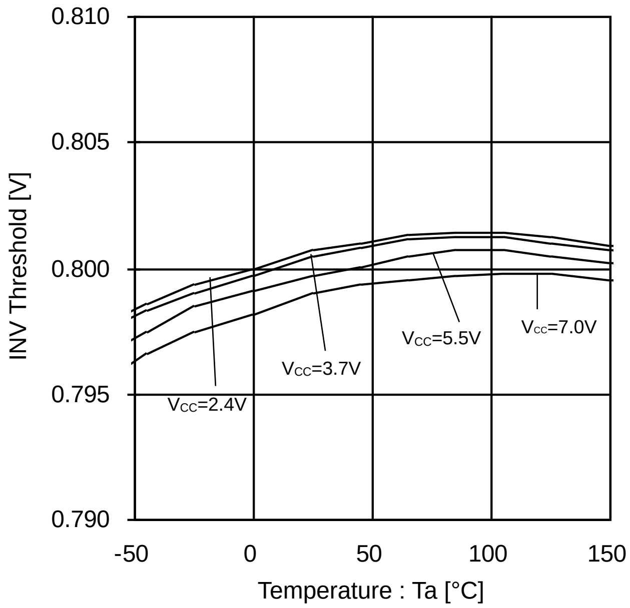

Figure 1. INV Threshold vs Temperature

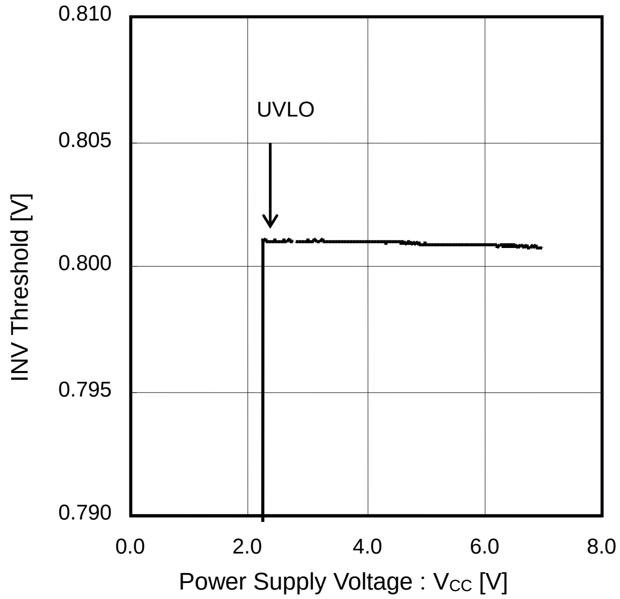

Figure 2. INV Threshold vs Power Supply Voltage
(Power Supply Property)

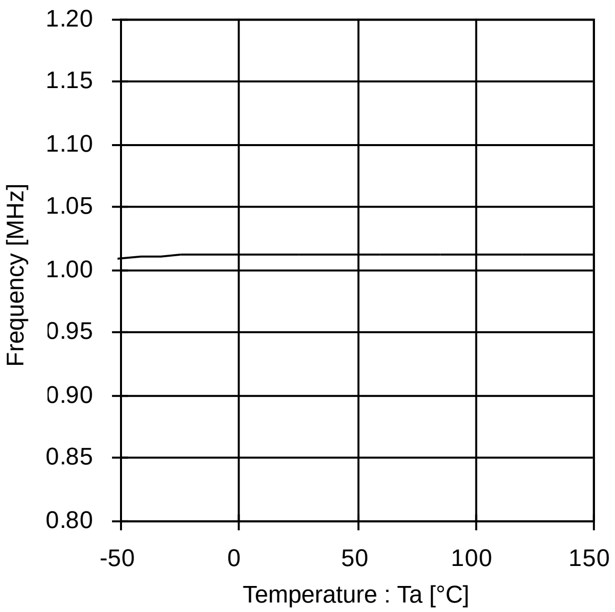

Figure 3. Frequency vs Temperature

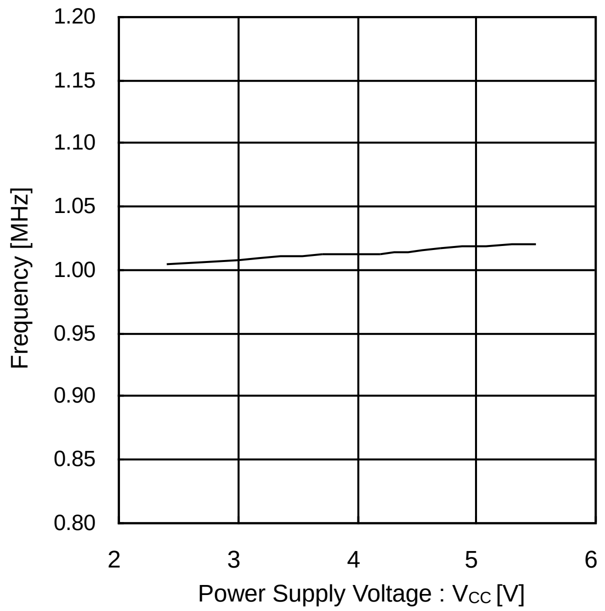

Figure 4. Frequency vs Power Supply Voltage
(Power Supply Property)

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Typical Performance Curves – continued

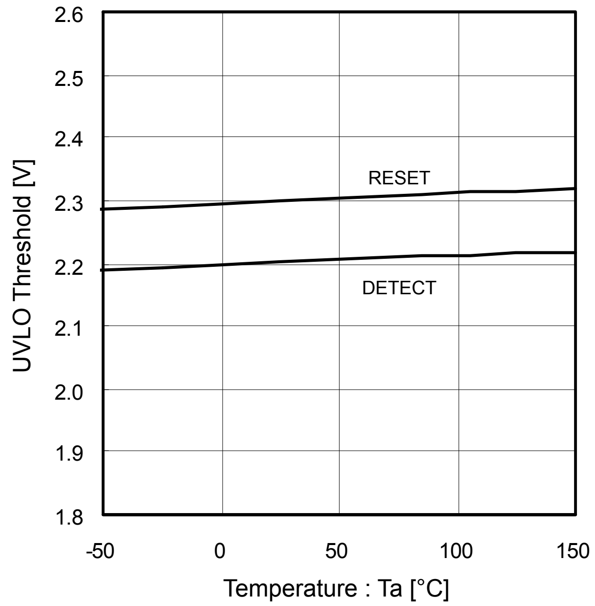

Figure 5. UVLO Threshold vs Temperature

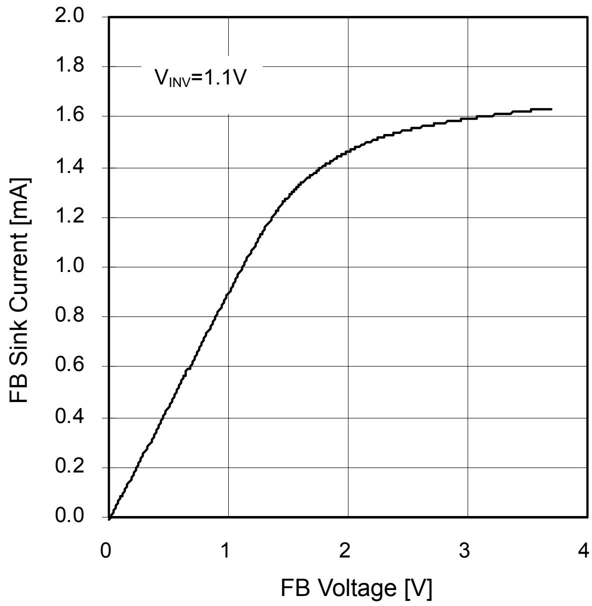

Figure 6. FB Sink Current vs FB Voltage

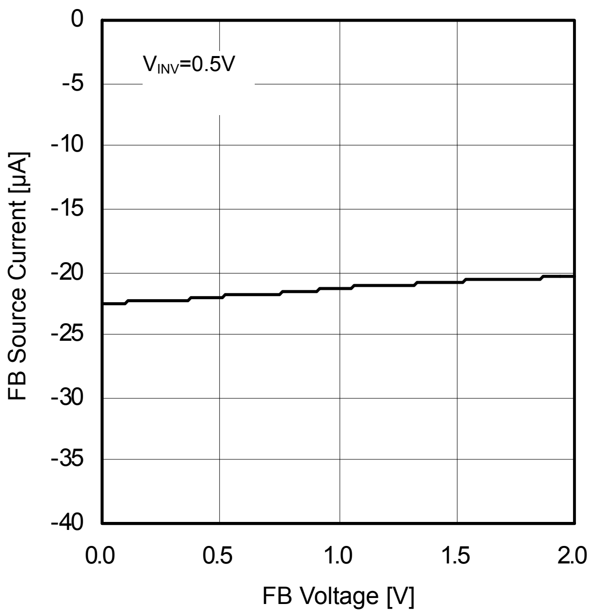

Figure 7. FB Source Current vs FB Voltage

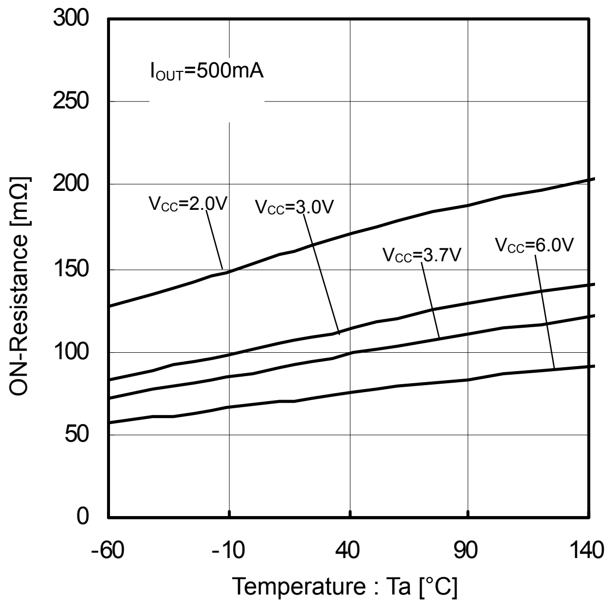

Figure 8. ON-Resistance vs Temperature
(Lx1 Pch FET ON Resistance)

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Typical Performance Curves – continued

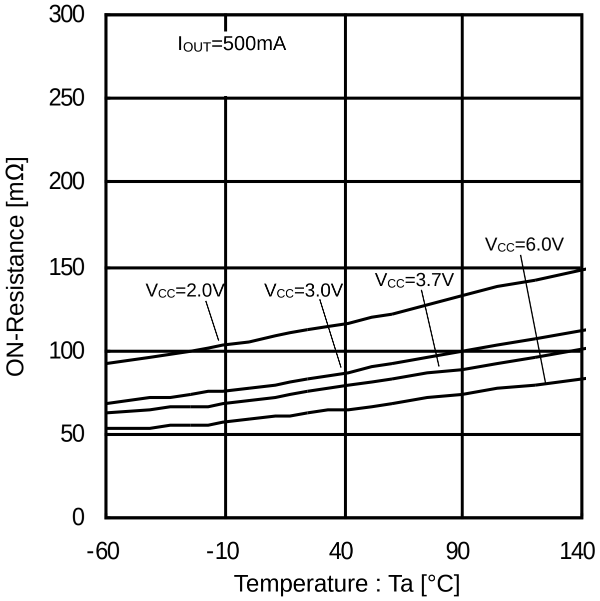

Figure 9. ON-Resistance vs Temperature (Lx1 Nch FET ON Resistance)

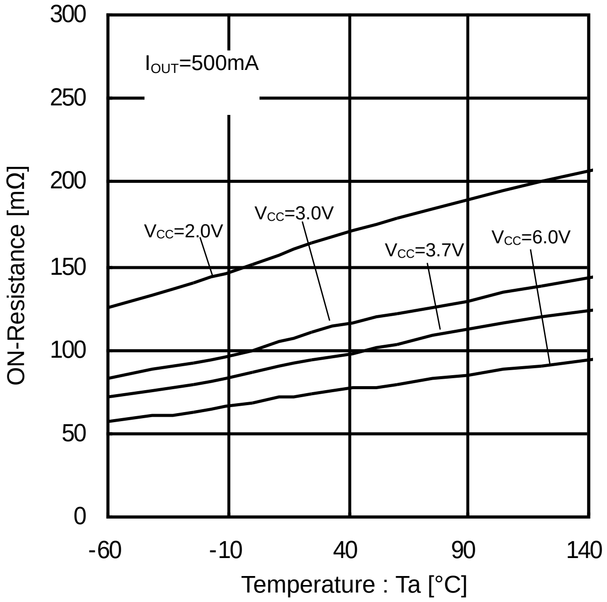

Figure 10. ON-Resistance vs Temperature (Lx2 Pch FET ON Resistance)

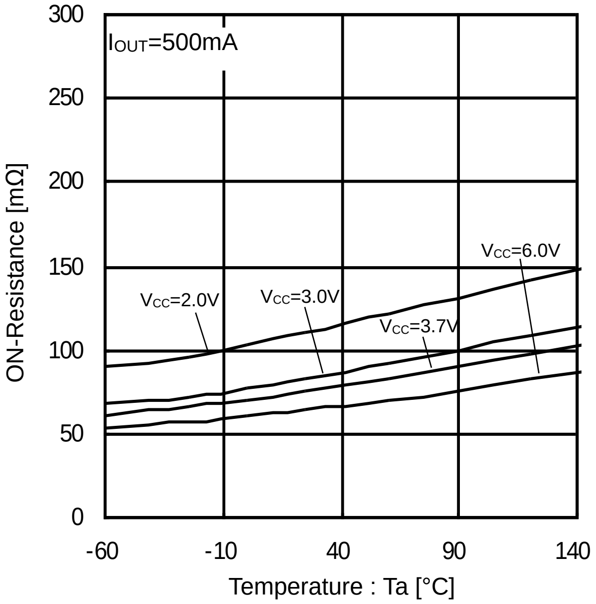

Figure 11. ON-Resistance vs Temperature (Lx2 Nch FET ON Resistance)

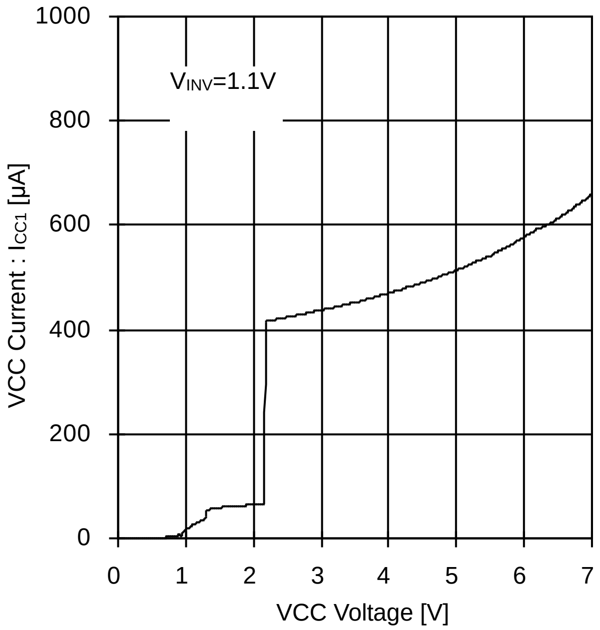

Figure 12. VCC Input Current vs VCC Voltage

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Typical Performance Curves – continued

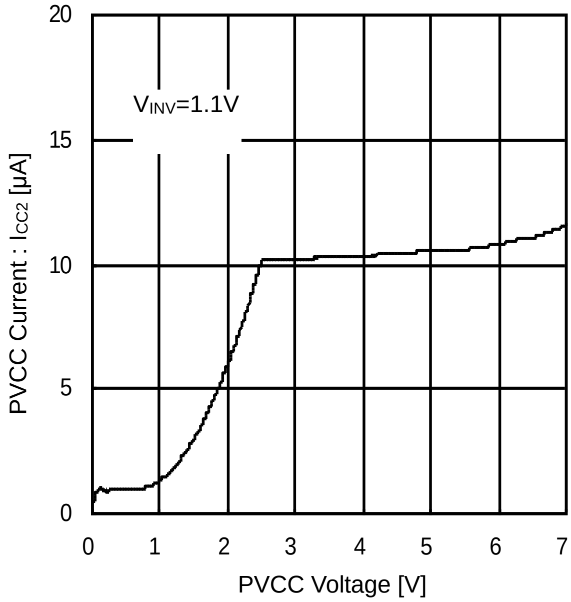

Figure 13. PVCC Input Current vs PVCC Voltage

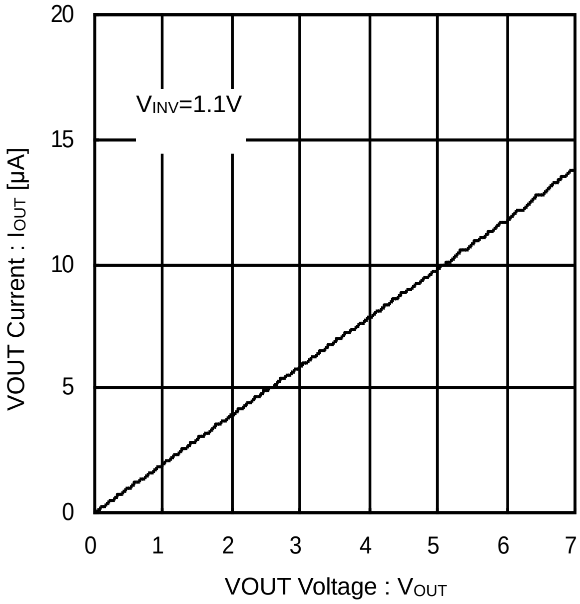

Figure 14. VOUT Input Current vs VOUT Voltage

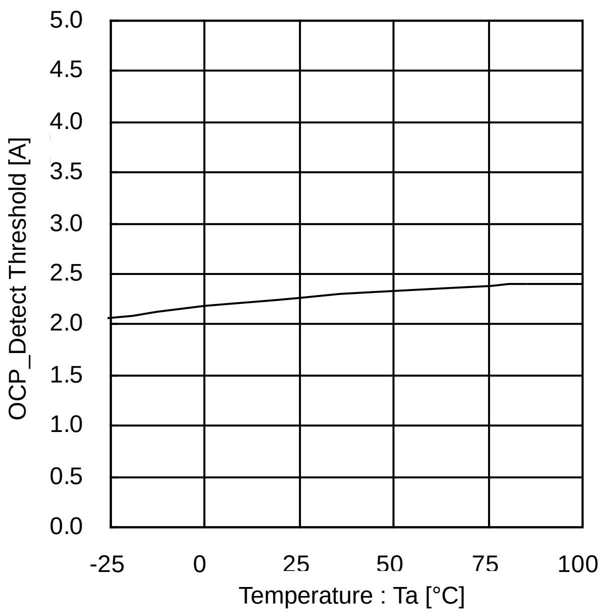

Figure 15. OCP Detect Threshold vs Temperature

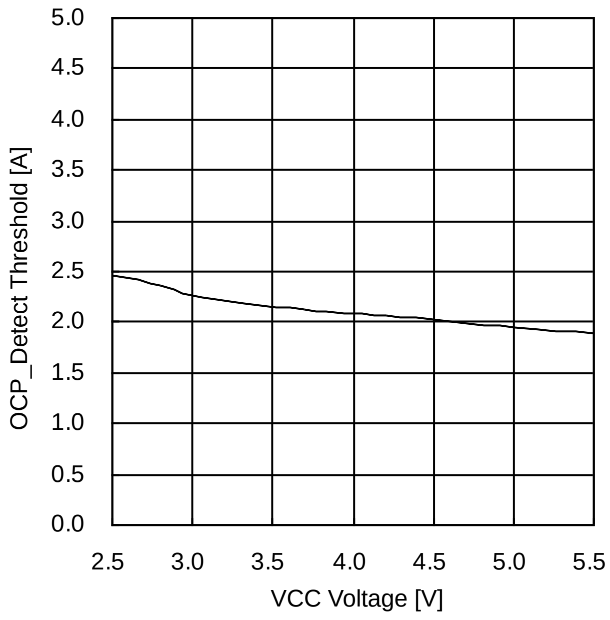

Figure 16. OCP Detect Threshold vs VCC Voltage

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Application Information

1. Example of Application1 Input: 2.8V to 5.5V, Output: 3.3V / 1.0A, Frequency 600 kHz

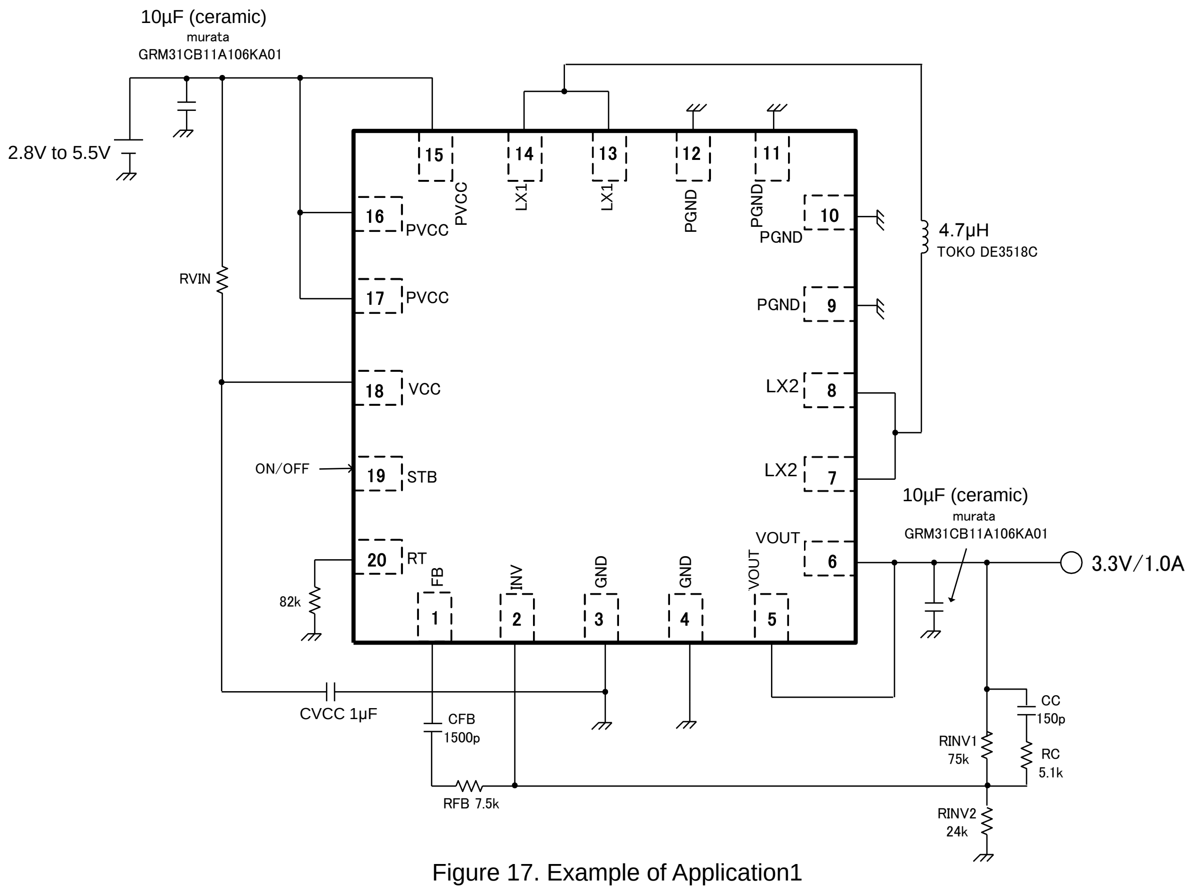

Figure 17. Example of Application1

2. Example of Application2 Input: 2.8V to 5.5 V, output: 4.0 V / 1.0 A, frequency 1MHz

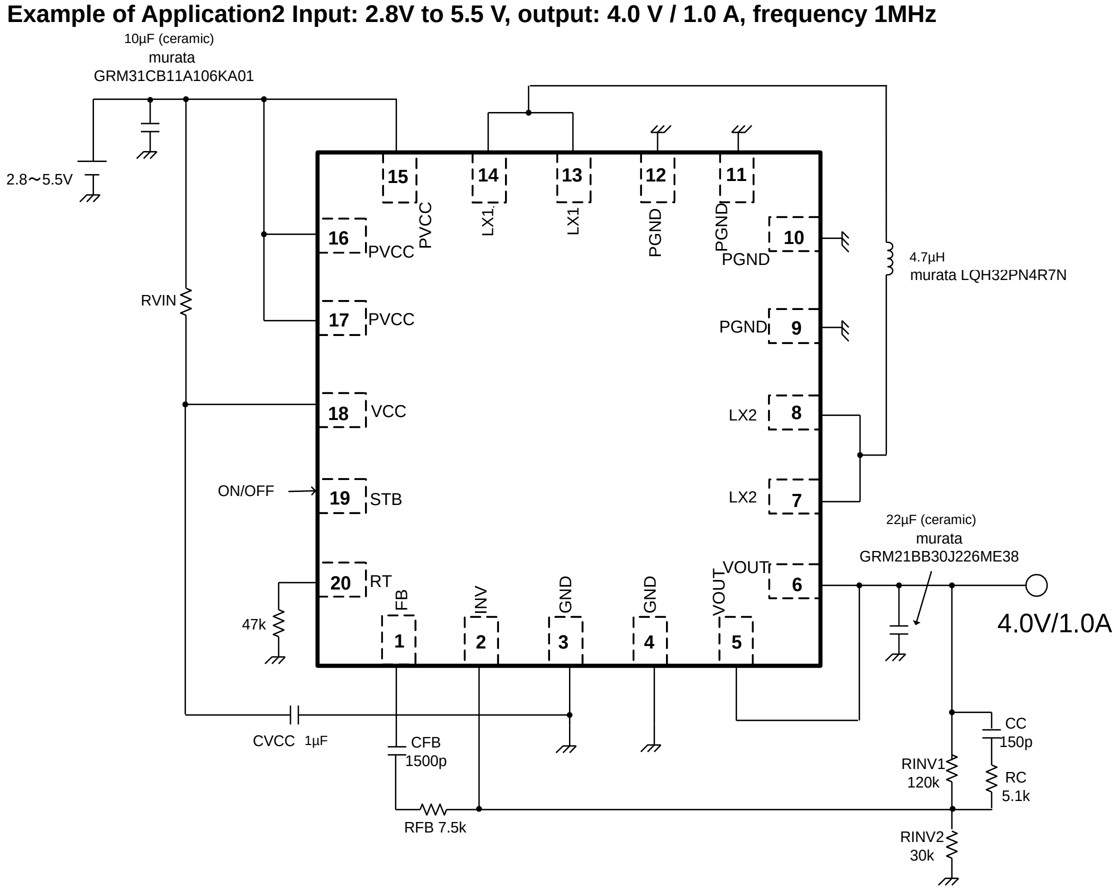

Figure 18. Example of Application2

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3. Example of Board Layout

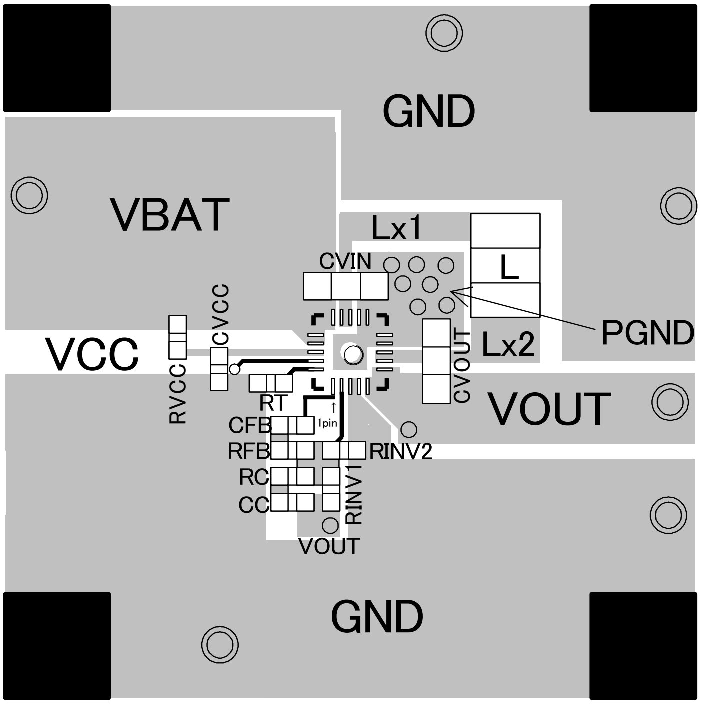

Figure 19. Example of Board Layout

4. Reference Application Data

(Example of Application 1)

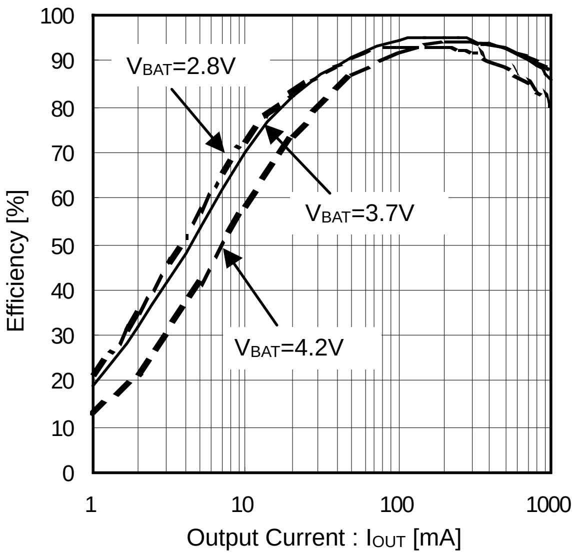

Figure 20. Efficiency vs Output Current
(Power Conversion Efficiency)

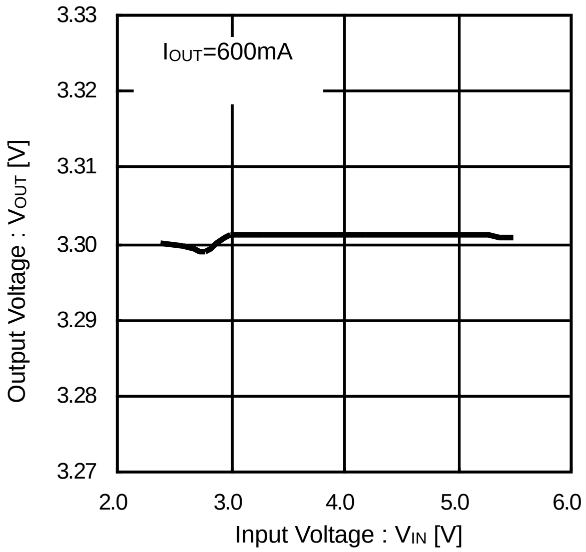

Figure 21. Output Voltage vs Input Voltage
(Line Regulation)

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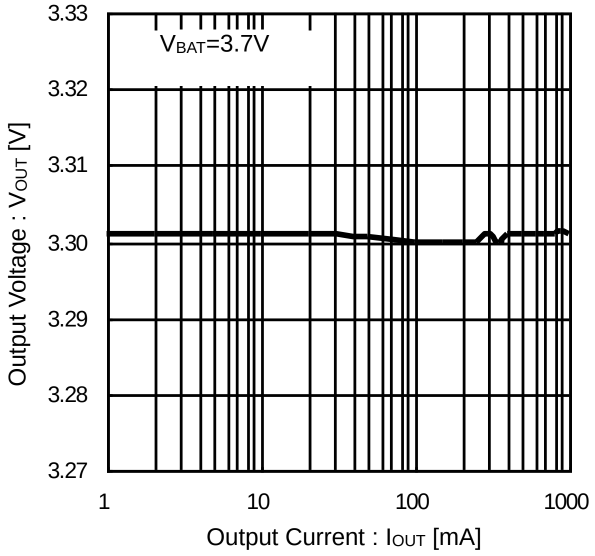

Figure 22. Output Voltage vs Output Current
(Load Regulation)

(Example of Application 2)

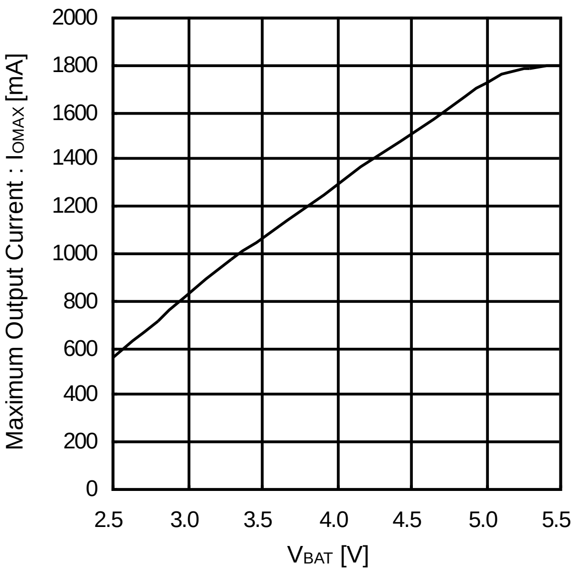

Figure 23. Maximum Output Current vs VBAT

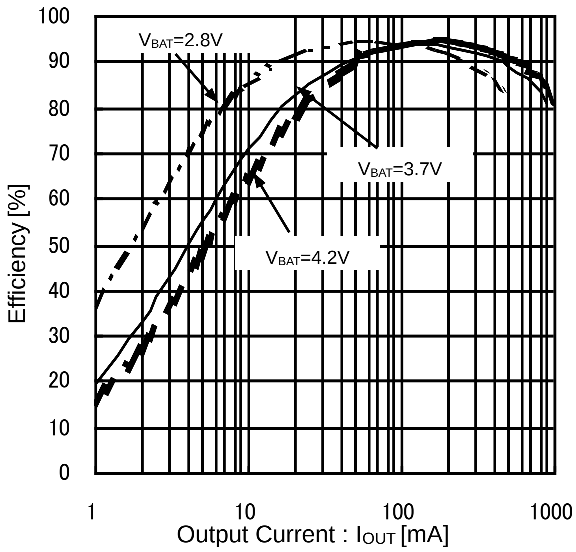

Figure 24. Efficiency vs Output Current
(Power Conversion Efficiency)

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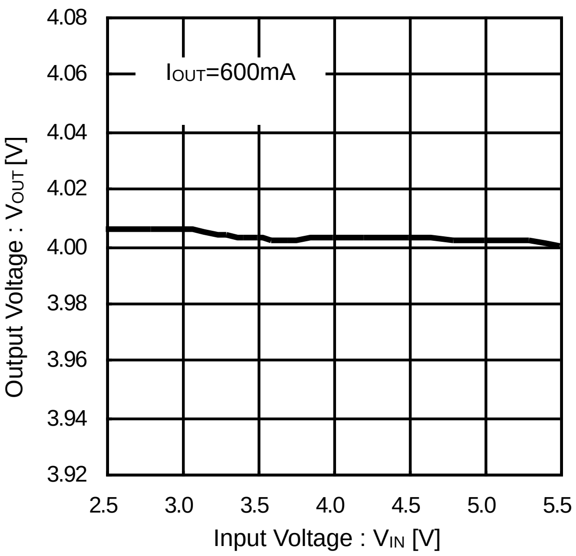

Figure 25. Output Voltage vs Input Voltage (Line Regulation)

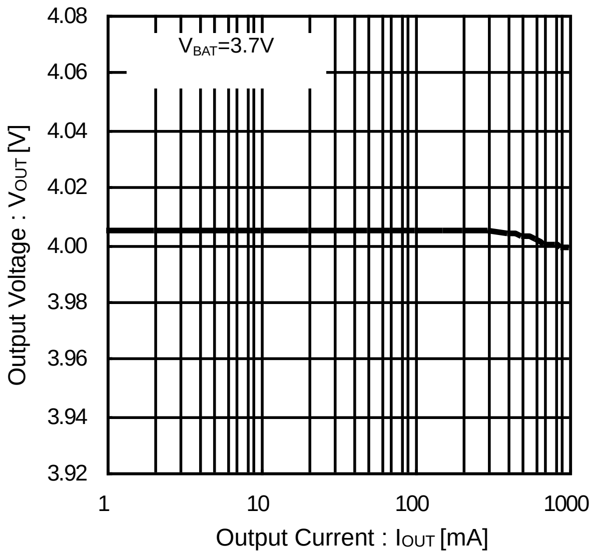

Figure 26. Output Voltage vs Output Current (Load Regulation)

5. Selection of Parts for Applications

(1) Output Inductor

A shielded inductor that satisfies the current rating (current value, I_{PEAK} as shown in the drawing below) and has a low DCR (direct current resistance component) is recommended.
Inductor values affect output ripple current greatly.
Ripple current can be reduced as the coil (L) value becomes larger and the switching frequency becomes higher as shown in the equations below.

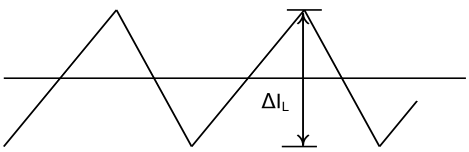

Figure 27. Ripple Current

$$I_{PEAK} = I_{OUT} \times (V_{OUT} / V_{IN}) / \eta + \Delta I_L / 2 \quad [A] \qquad (1)$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad [A] \quad \text{(in step-down mode)} \qquad (2)$$

$$\Delta I_L = \frac{|(V_{IN} - V_{OUT})|}{L} \times \frac{V_{OUT} \times 2 \times 0.85}{(V_{IN} + V_{OUT})} \times \frac{1}{f} \quad [A] \quad \text{(in step-up/down mode)} \qquad (3)$$

$$\Delta I_L = \frac{(V_{OUT} - V_{IN})}{L} \times \frac{V_{IN}}{V_{OUT}} \times \frac{1}{f} \quad [A] \quad \text{(in step-up mode)} \qquad (4)$$

Where:
η is the Efficiency,
ΔI_L is the Output ripple current,
f is the Switching frequency

As a guide, output ripple current should be set at about 20% to 50% of the maximum output current.

(Note) Current flow that exceeds the coil rating brings the coil into magnetic saturation, which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

(2) Output Capacitor

A ceramic capacitor with low ESR is recommended for output in order to reduce output ripple.
There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration.
Output ripple voltage when ceramic capacitor is used is obtained by the following equation.

$$V_{PP} = \Delta I_L \times \frac{1}{2\pi \times f \times C_O} + \Delta I_L \times R_{ESR} \quad [V] \quad \cdots (5)$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

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(3) Setting of Oscillation Frequency
Oscillation frequency can be set using a resistance value connected to the RT pin (Pin 20).
Oscillation frequency is set at 1MHz when R_{RT} = 47kΩ, wherein frequency is inversely proportional to the RT value.
See Figure 28 for the relationship between RT and frequency.
Soft-start time changes along with oscillation frequency.
See Figure 29 for the relationship between RT and soft-start time.

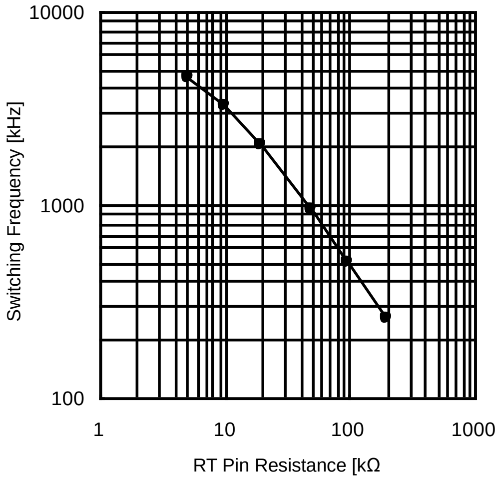


Figure 28. Oscillation Frequency vs RT Pin Resistance

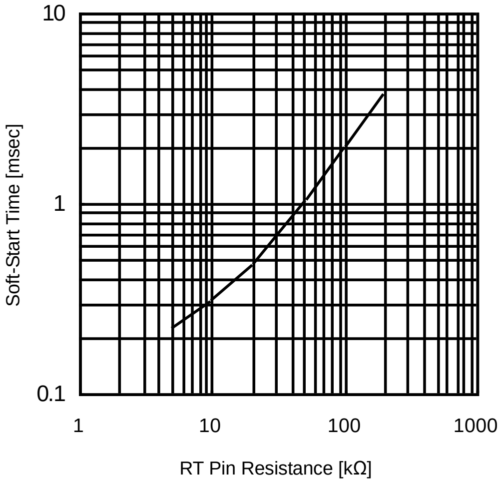
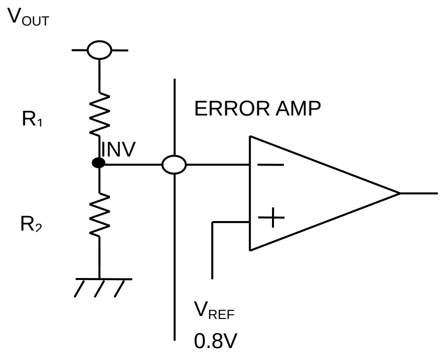


Figure 29. Soft-Start Time vs RT Pin Resistance

Note that the above example of frequency setting is just a design target value, and may differ from the actual equipment.

(4) Output Voltage Setting
The internal reference voltage of the ERROR AMP is 0.8V.
Output voltage should be obtained by referring to Equation (8) of Figure 30.



$$V_{OUT} = \frac{(R_1 + R_2)}{R_2} \times 0.8 \quad [V] \cdot\cdot\cdot \quad (8)$$

Figure 30. Setting of Feedback Resistance

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(5) Determination of Phase Compensation
Condition for stable application
The condition for feedback system stability under negative feedback is as follows:

(a) Phase delay is 135 °or less when gain is 1 (0dB) (Phase margin is 45° or higher)
Since DC/DC converter application is sampled according to the switching frequency, the Gain-BW of the whole system (frequency at which gain is 0 dB) must be set to be equal to or lower than 1/5 of the switching frequency.
In summary, target property of applications is as follows:

(b) Phase delay must be 135°or lower when gain is 1 (0dB) (Phase margin is 45° or higher).

(c) The Gain-BW at that time (frequency when gain is 0dB) must be equal to or lower than 1/5 of the switching frequency.
For this reason, switching frequency must be increased to improve responsiveness.

One of the points to secure stability by phase compensation is to cancel the secondary phase delay (-180°) generated by LC resonance of the secondary phase lead (i.e. put two phase leads).
Since Gain-BW is determined by the phase compensation capacitor attached to the error amplifier, when it is necessary to reduce Gain-BW, the capacitor should be made larger.

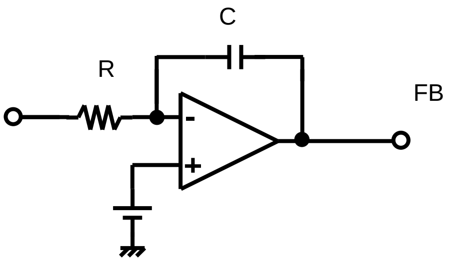
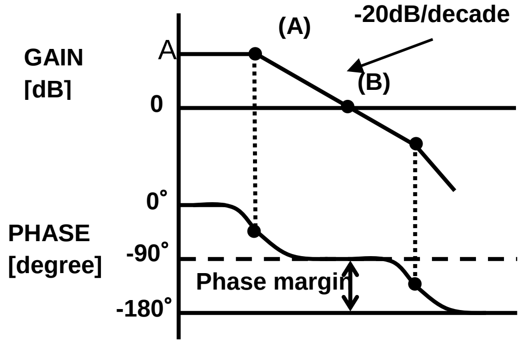


Figure 31. General Integrator

Error AMP is a low-pass filter because phase compensation such as (1) and (2) is performed. For DC/DC converter application, R is a parallel feedback resistance.



Point (A) $f_P = \frac{1}{2\pi RCA}$ $[Hz]$ (9)

Point (B) $f_{GBW} = \frac{1}{2\pi RC}$ $[Hz]$ (10)

Figure 32. Frequency Property of Integrator

Phase compensation when an output capacitor with a low ESR such as ceramic capacitor is used is as follows:
When an output capacitor with low ESR (several tens of mΩ) is used for output, the secondary phase lead (two phase leads) must be put to cancel the secondary phase lead caused by LC. One example of phase compensation methods is as follows:

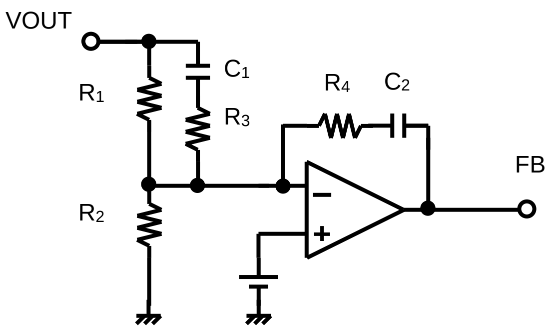


Figure 33. Example of Setting of Phase Compensation

$$Phaselead\ fz1 = \frac{1}{2\pi R_1 C_1} \quad [Hz] \tag{11}$$

$$Phaselead\ fz2 = \frac{1}{2\pi R_4 C_2} \quad [Hz] \tag{12}$$

$$Phasedelay\ fp1 = \frac{1}{2\pi R_3 C_1} \quad [Hz] \tag{13}$$

$$LC\ resonance frequency = \frac{1}{2\pi\sqrt{(LC)}} \quad [Hz] \tag{14}$$

For setting of phase-lead frequency, both of them should be put near the LC resonance frequency.
When Gain-BW frequency becomes too high due to the secondary phase lead, it may be stabilized by setting the primary phase delay to a frequency slightly higher than the LC resonance frequency by R_3 to compensate it.

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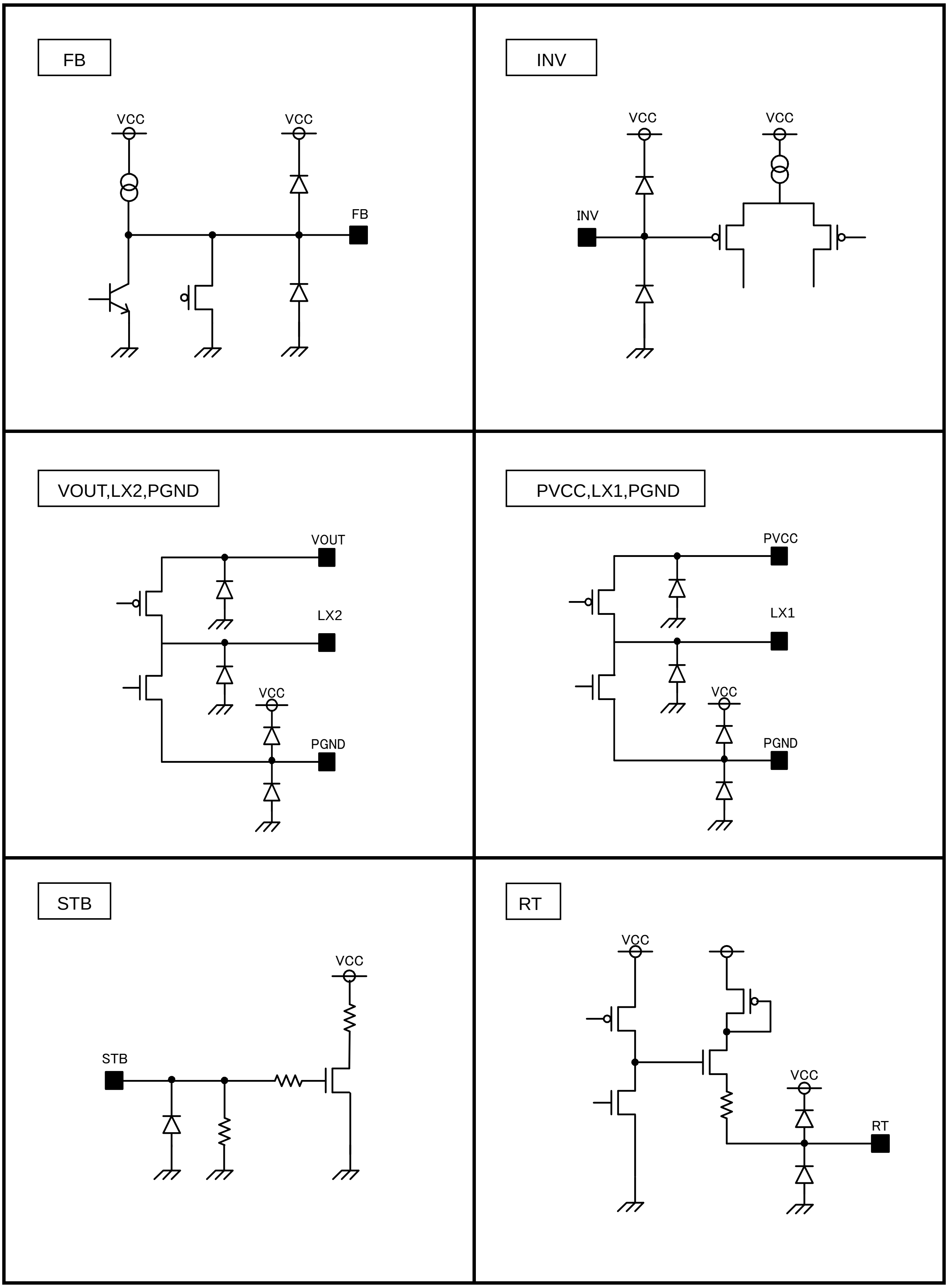
I/O Equivalent Circuits



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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

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Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

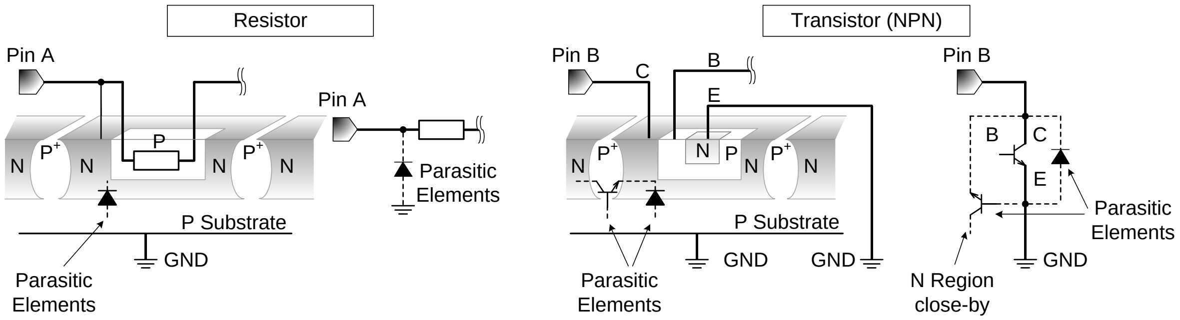

Figure 34. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

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Ordering Information

B D 8 3 0 5 M U V - E 2

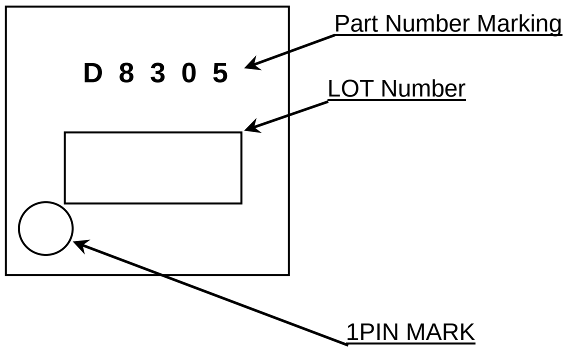
Part Number

Package
MUV: VQFN020V4040

Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram

VQFN020V4040 (TOP VIEW)



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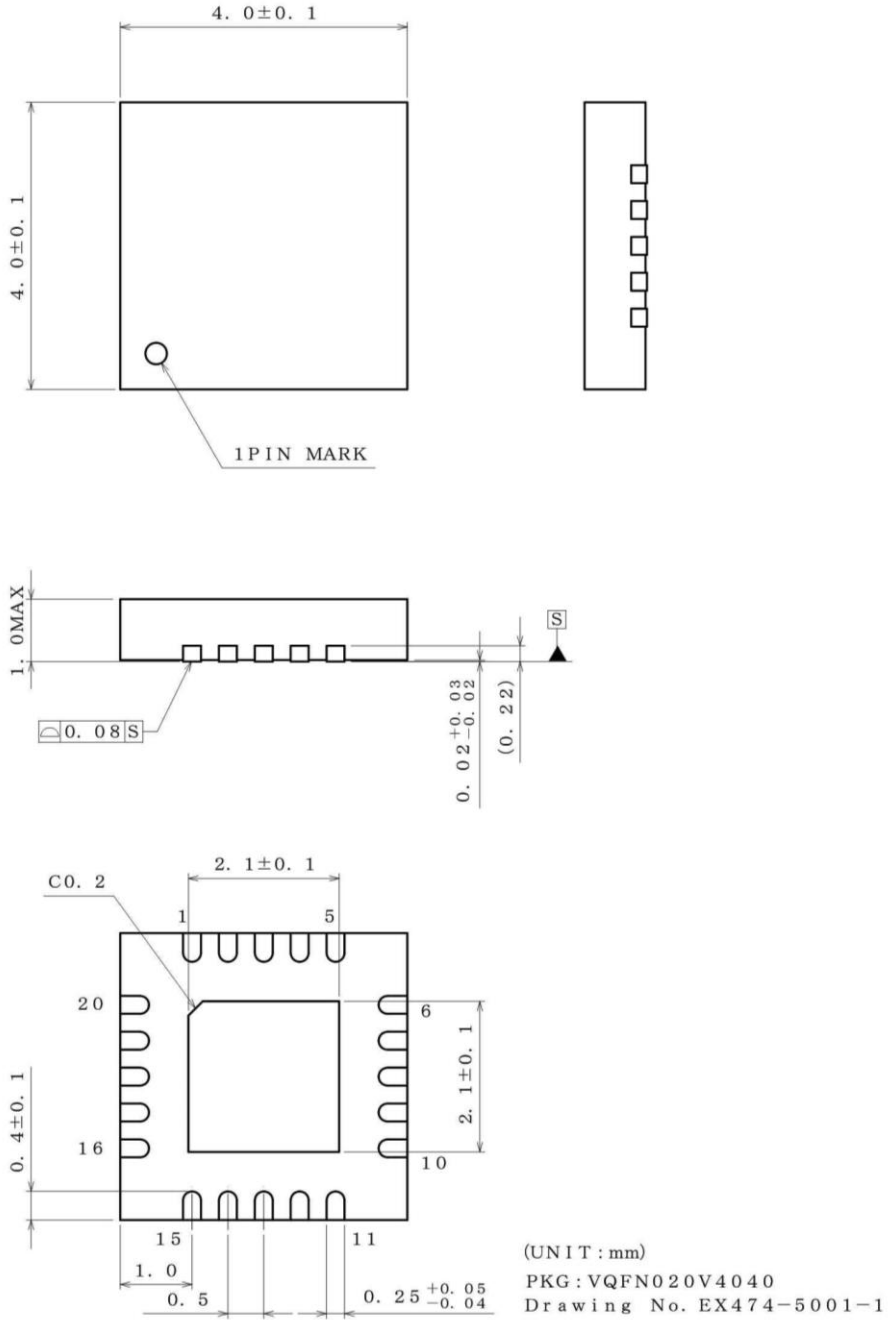
Physical Dimension, Tape and Reel Information

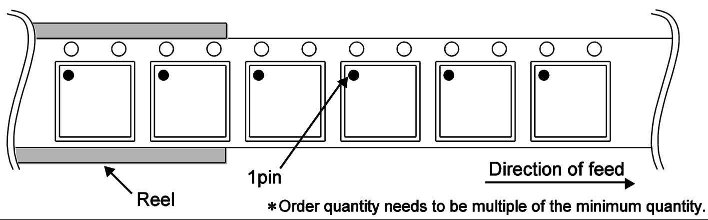
Package Name	VQFN020V4040



(UNIT : mm)
PKG : VQFN020V4040
Drawing No. EX474−5001−1

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
26.Nov.2014	001	New Release

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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