Standard LCD Segment Driver

BU9794AKV MAX 200 segments (SEG50×COM4)

●Features

- Integrated RAM for display data (DDRAM) : 50 × 4bit (Max 200 Segment)
- LCD drive output : 4 Common output, 50 Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design
- Independent power supply for LCD driving

●Key Specifications

- Supply Voltage Range: +2.5V to +5.5V
- LCD drive power supply Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 200 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

●Applications

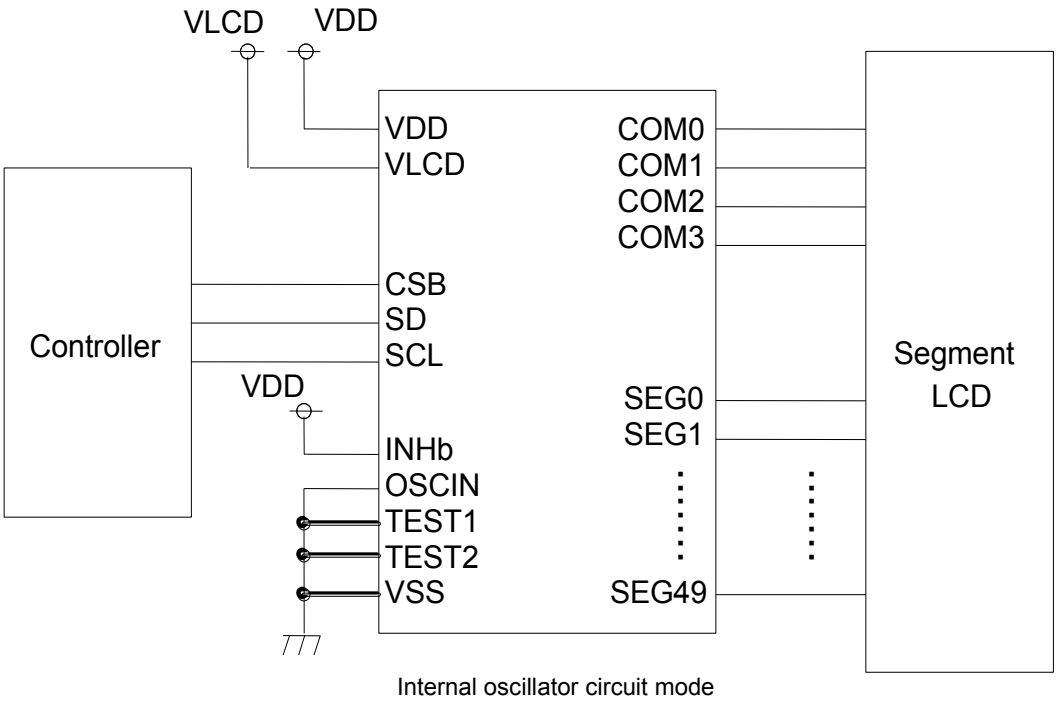
- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment, etc.

●Package

W (Typ.) x D (Typ.) x H (Max.)

VQFP64
12.00mm x 12.00mm x 1.60mm

●Typical Application Circuit



Internal oscillator circuit mode

Figure 1. Typical application circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed for protection against radioactive rays.

●Block Diagram / Pin Configuration / Pin Description

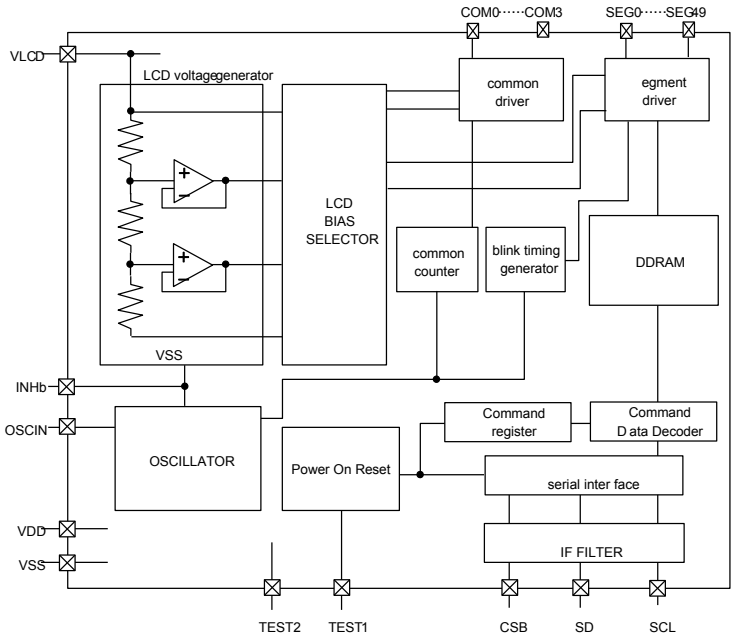


Figure 2. Block Diagram

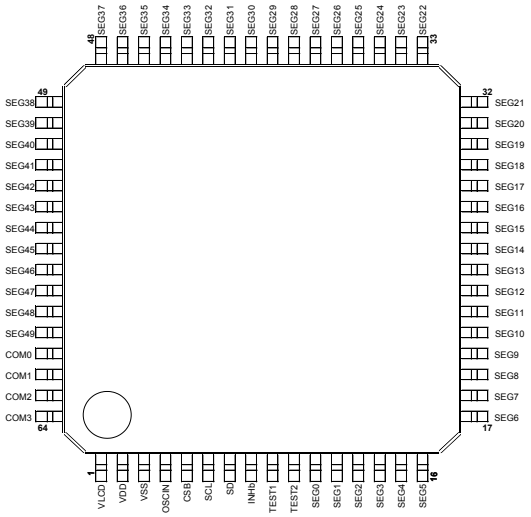


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Terminal	Terminal No.	I/O	Function	Handling when unused
INHb	8	I	Input terminal for turning off display H : turn on display L : turn off display	VDD
TEST1	9	I	Test input (ROHM use only) Must be connected to VSS	GND
TEST2	10	I	Test input (ROHM use only) Must be connected to VSS	GND
OSCIN	4	I	External clock input. External clock and Internal clock can be selected by command. Must be connected to VSS when internal oscillation circuit is used.	GND
SD	7	I	Serial data input	GND
SCL	6	I	Serial data transfer clock	GND
CSB	5	I	Chip select : “L” active	GND
VSS	3		GND	-
VDD	2		Power supply	-
VLCD	1		Power supply for LCD driving	-
SEG0 to 49	11 to 60	O	SEGMENT output for LCD driving	OPEN
COM0 to 3	61 to 64	O	COMMON output for LCD driving	OPEN

●**Absolute Maximum Ratings (VSS=0V)**

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 to +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 to +7.0	V	LCD drive voltage
Power dissipation	Pd	0.75	W	When operate at more than 25℃, subtract 7.5mW/°C (Package only)
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operational temperature range	Topr	-40 to +85	℃	
Storage temperature range	Tstg	-55 to +125	℃	

●**Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)**

Parameter	Symbol	Ratings			Unit	Remarks
		MIN	TYP	MAX		
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	2.5	-	5.5	V	LCD drive voltage

●**Electrical Characteristics**

DC Characteristics (VDD=2.5V to 5.5V, VLCD=2.5 to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter		Symbol	Limits			Unit	Conditions
			MIN	TYP	MAX		
“H” level input voltage		VIH	0.8VDD	-	VDD	V	SD,SCL,CSB
“L” level input voltage		VIL	VSS	-	0.2VDD	V	SD,SCL,CSB
“H” level input current		IIH	-	-	1	μA	SD,SCL,CSB
“L” level input current		IIL	-1	-	-	μA	SD,SCL,CSB
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10μA
	COM	RON	-	3.5	-	kΩ	
Standby current		Ist	-	-	5	μA	Display off, Oscillation off
Power consumption 1		IDD	-	5	15	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse
Power consumption 2		ILCD	-	10	20	μA	VDD=3.3V, VLCD=5V, Ta=25°C Power save mode1, FR=70Hz 1/3 bias, Frame inverse

Oscillation Characteristics
(VDD=2.5V to 5.5V, VLCD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency	fCLK	68	80	92	Hz	FR = 80Hz setting, VDD=3.3V

MPU I/F Characteristics (VDD=2.5V to 5.5V, VLCD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions
		MIN.	TYP.	MAX.		
Input rise time	tr	-	-	80	ns	
Input fall time	tf	-	-	80	ns	
SCL cycle time	tSCYC	400	-	-	ns	
“H” SCL pulse width	tSHW	100	-	-	ns	
“L” SCL pulse width	tSLW	100	-	-	ns	
SD setup time	tSDS	20	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
“H” CSB pulse time	tCHW	50	-	-	ns	

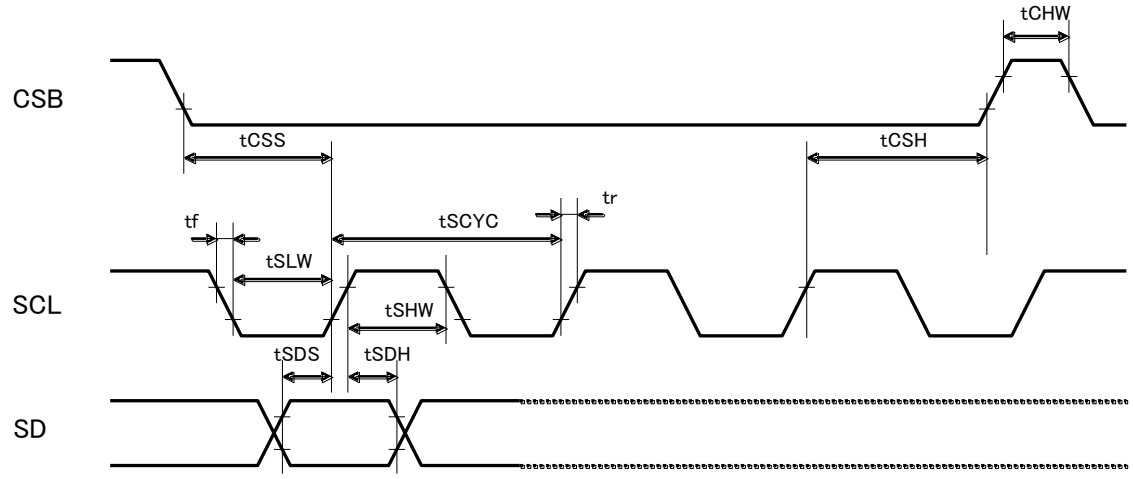


Figure 4. Interface Timing

●I/O equivalent circuit

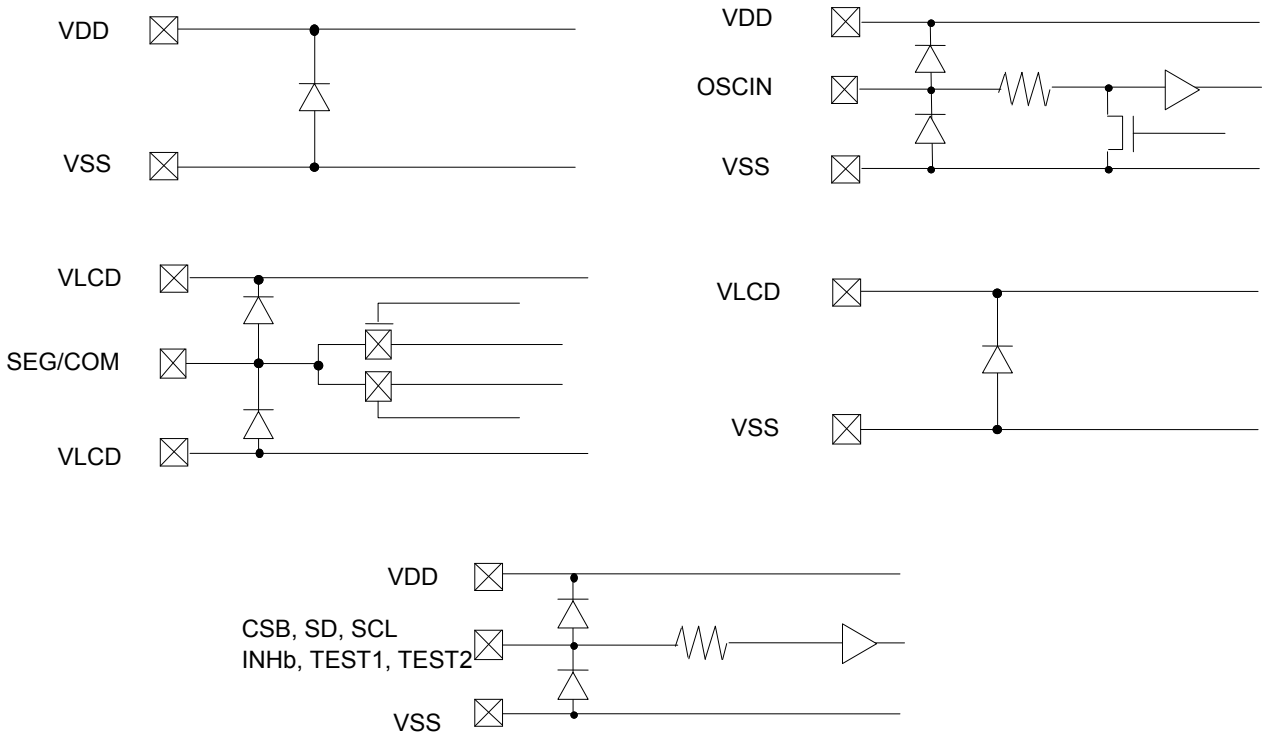
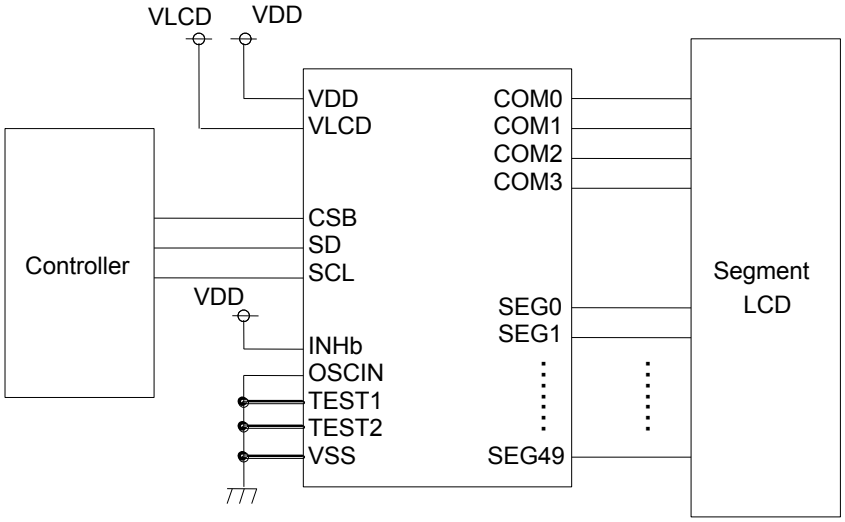
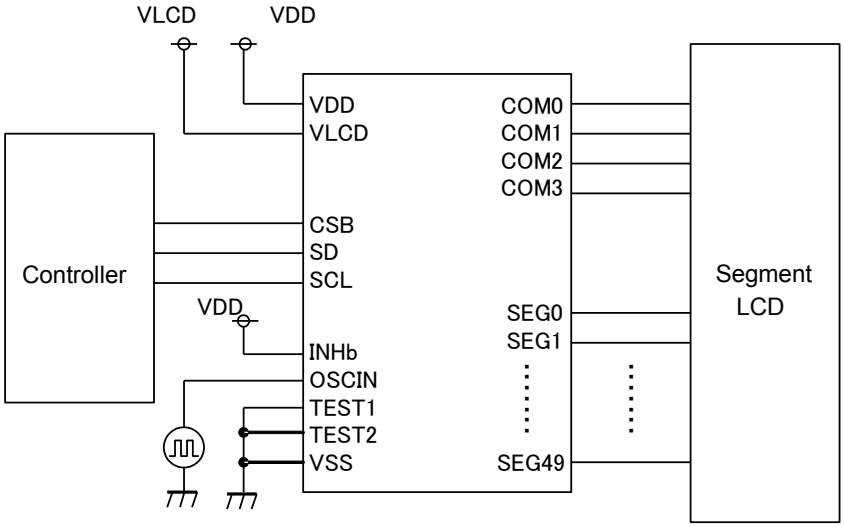


Figure 5. I/O equivalent circuit

●**Example of recommended circuit**



Internal oscillator circuit mode



External clock input mode

Figure 6. Example of recommended circuit

●Function Description

○Command and data transfer method

○SPI (3wire Serial Interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H", and CSB="L" makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by D6 – D0 during CSB ="L".
(Internal data is latched at the rising edge of SCL, then it is converted to 8bits parallel data at the rising edge of 8th CLK.)

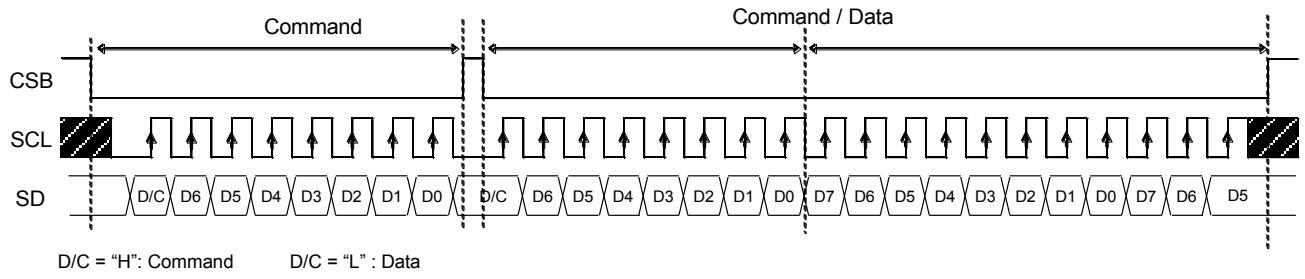


Figure 7. 3-SPI Command/Data Transfer format

○Command transfer method

After CSB="H"→"L", 1st byte is always a command input.
MSB of the command input data will be judged that the next byte data is a command or display data (This bit calls "command or data judgment bit").
When set "command or data judge bit"='1', next byte will be (continuously) command.
When set "command or data judge bit"='0', next byte data is display data.

1 Command	1 Command	1 Command	0 Command	Display Data	...

Once it becomes display data transfer condition, it will not be back to command input condition even if D/C=1.
So if you want to send command data again, please set CSB="L"→"H" (CSB "L"→"H" will cancel data transfer condition.)
Command transfer is done by 8bits unit, so if CSB="L"→"H" with less than 8bits data transfer, command will be cancelled.
It will be able to transfer command with CSB="L" again.

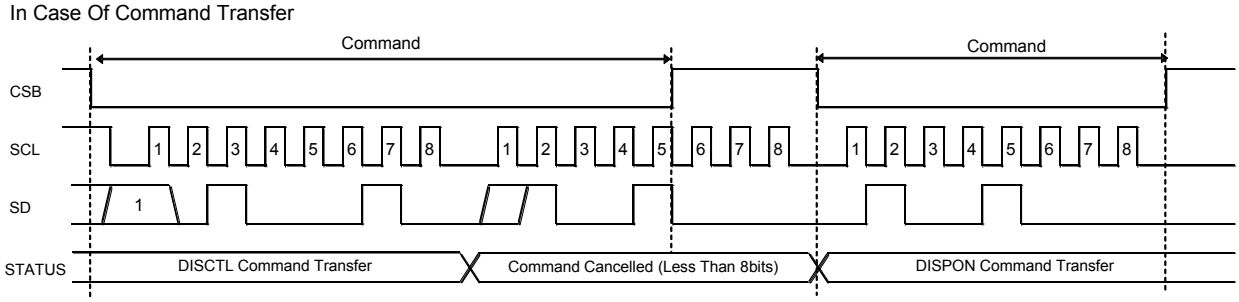
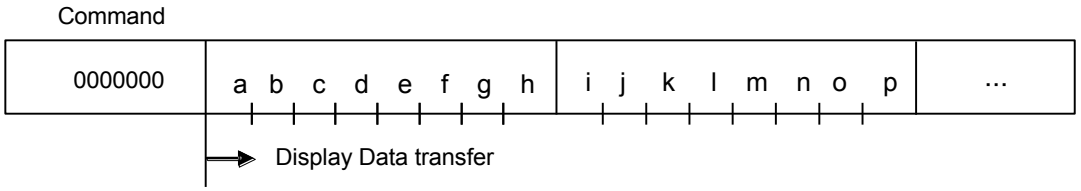


Figure 8. Command transfer format

○Write display data and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bit.

The relationship between data input and display data, DDRAM data and address are as follows;



8 bit data will be stored in DDRAM. The address to be written is the specified by ADSET command and the address is automatically incremented in every 4bit data.

Data can be continuously written in DDRAM by transmitting Data continuously.

(When RAM data is written successively after writing RAM data to 31h (SEG49), the address is returned to 00h (SEG0) by the auto-increment function

DDRAM address

BIT	00	01	02	03	04	05	06	・・・	2Fh	30h	31h	
0	a	e	i	m								COM0
1	b	f	j	n								COM1
2	c	g	k	o								COM2
3	d	h	l	p								COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6		SEG47	SEG48	SEG49	

As data transfer to DDRAM is done every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

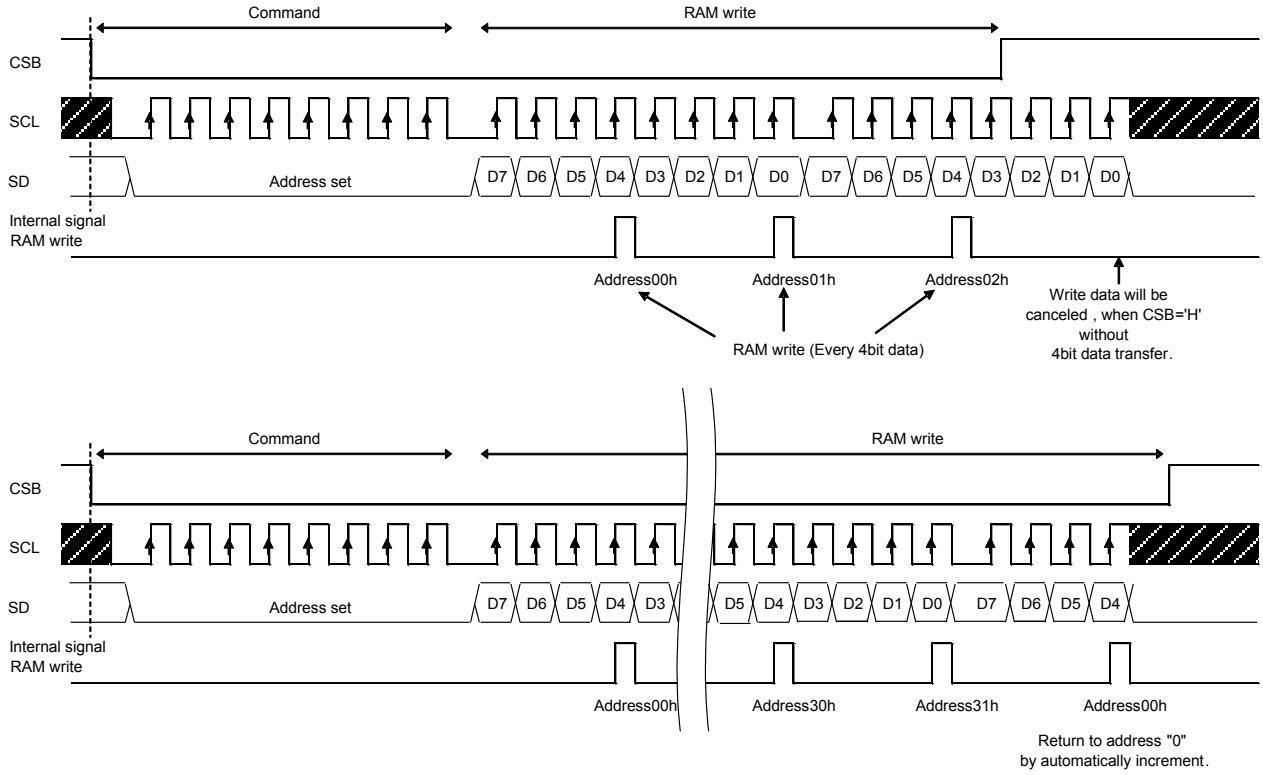


Figure 9. Data transfer format

○OSCILLATOR

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

*When using external clock mode, it has to input external clock from OSCIN terminal after DISCTL command setting.

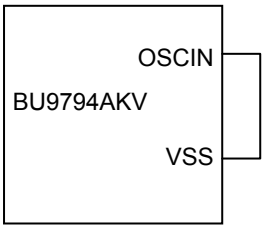


Figure 10. Internal oscillator circuit mode

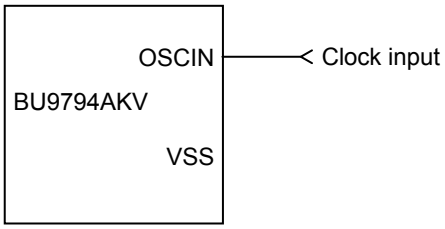


Figure 11. External clock input mode

○LCD Driver Bias Circuit

This device generates LCD driving voltage with on-chip Buffer AMP.
It can drive LCD at low power consumption.
*1/3 and 1/2Bias can set in DISCTL command.
*Line and frame inversion can set in MODESET command.
Refer to “LCD driving waveform” about each LCD driving waveform.

○Blink timing generator

This device has Blink function.
*This device will be Blink mode with BLKCTL command.
Blink frequency varies widely by characteristic of fCLK, when at internal oscillation circuit mode.
Refer to Oscillation Characteristics for more details on fCLK.

○Reset initialize condition

Initial condition after execute Software Reset is as follows.
・Display is OFF.
・DDRAM address is initialized (DDRAM Data is not initialized).
Refer to Command Description about initialize value of register.

●Command / Function List

Description List of Command / Function

No.	Command	Function
1	Mode Set (MODESET)	Set LCD drive mode
2	Address Set (ADSET)	Set LCD display mode 1
3	Display Control (DISCTL)	Set LCD display mode 2
4	Software Reset (SWRST)	Execute software reset
5	Blink Control (BLKCTL)	Set blink mode
6	All Pixel Control (APCTL)	Set pixel condition

●Detailed Command Description

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C: 0 : Next byte is RAM write data.
1 : Next byte is command.

○Mode Set (MODESET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	0	P3	P2	P1	P0

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF	0	○
Display ON	1	

Display OFF: Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1frame of data write. Display OFF mode will be finished by Display ON.
Display ON: SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

Set LCD drive waveform

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

*Refer to LCD driving waveform.

Set Power save mode

Setup	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

*Please use VLCD≥3.0V at High power mode.

(Reference current consumption data)

Setup	Current consumption
Power save mode 1	×0.5
Power save mode 2	×0.67
Normal mode	×1.0
High power mode	×1.8

*Above data is reference. It depends on Panel load.

○Address Set (ADSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	P5	P4	P3	P2	P1	P0

The address can be set from 00h to 31h.
Address beyond this range will be set at 00h.
At reset condition, the address is set to 00h.

○Display Control (DISCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	1	P3	P2	P1	P0

Set bias level

setup	P3	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

*Refer to LCD driving waveform.

Set oscillator mode

setup	P2	Reset initialize condition
Internal oscillation	0	○
External clock input	1	

Internal oscillation: Must be connected to VSS.
External clock input: Input external clock from OSCIN terminal

<Frame frequency Calculation at external clock mode>
DISCTL 80Hz setting: Frame frequency [Hz] = external clock [Hz] / 512
DISCTL 71Hz setting: Frame frequency [Hz] = external clock [Hz] / 576
DISCTL 64Hz setting: Frame frequency [Hz] = external clock [Hz] / 648
DISCTL 53Hz setting: Frame frequency [Hz] = external clock [Hz] / 768

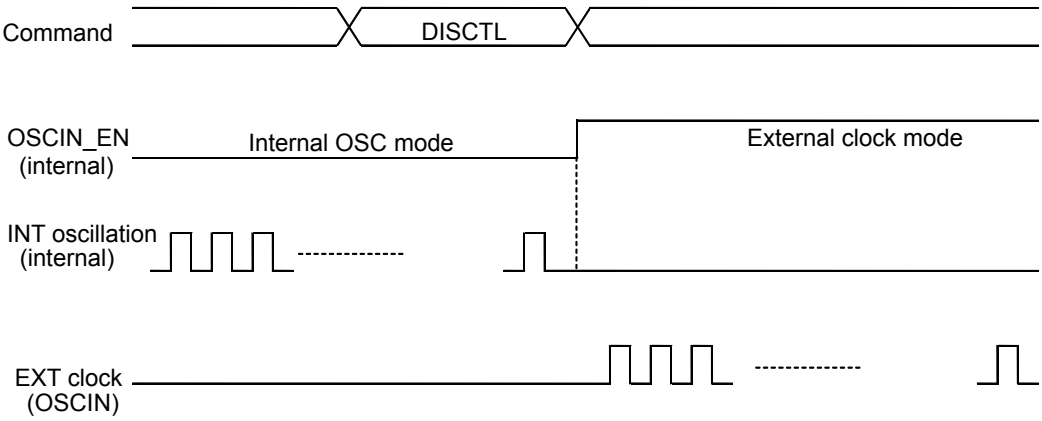


Figure 12. OSCMODE change timing

Set Frame frequency

Setup	P1	P0	Reset initialize condition
80Hz	0	0	○
71Hz	0	1	
64Hz	1	0	
53Hz	1	1	

(Note) The setting of the frame frequency, LCD waveform, and Power save mode will influence the following display image qualities. Please select most suitable value from current consumption and display image quality with LCD panel.

Mode	Flicker	Image quality, contrast
Frame frequency	○	-
LCD waveform	○	○
Power save mode	-	○

○Software Reset (SWRST)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	0	1	1

This command will set initial condition

○Blink Control (BLKCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

(Don't care)

Set blink mode

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

○All Pixel Control (APCTL)

MSB LSB

7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

All pixels ON: All pixels are ON regardless of DDRAM data
All pixels OFF: All pixels are OFF regardless of DDRAM data

(Note) This command is valid in Display on status. The data of DDRAM don't change by this command.
If set both P1 and P0 ="1", APOFF will be select.

●LCD driving waveform

(1/3bias)

Line inversion

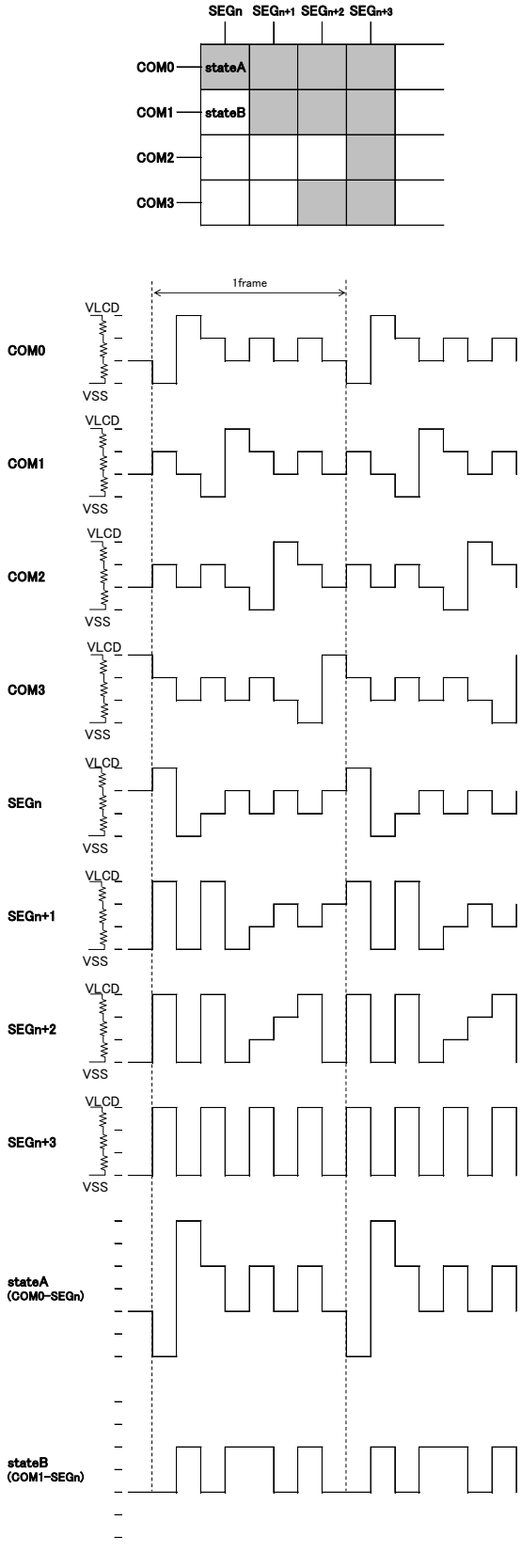


Figure 13.LCD waveform at line inversion (1/3bias)

Frame inversion

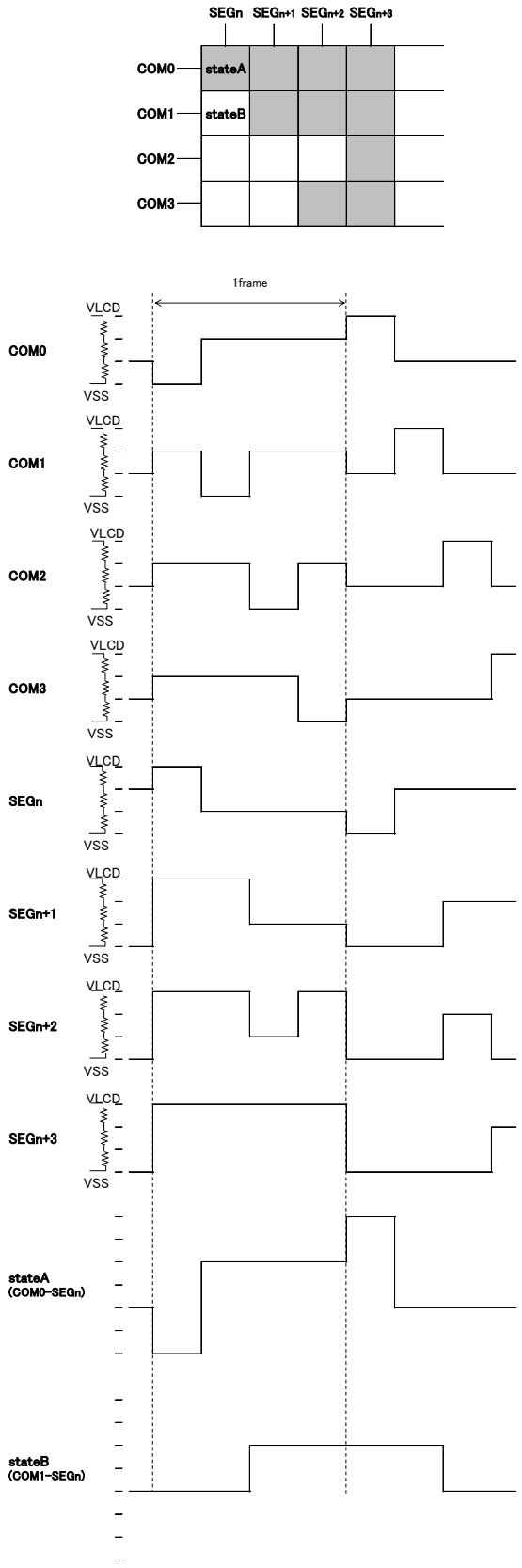


Figure 14.LCD waveform at frame inversion (1/3bias)

(1/2bias)

Line inversion

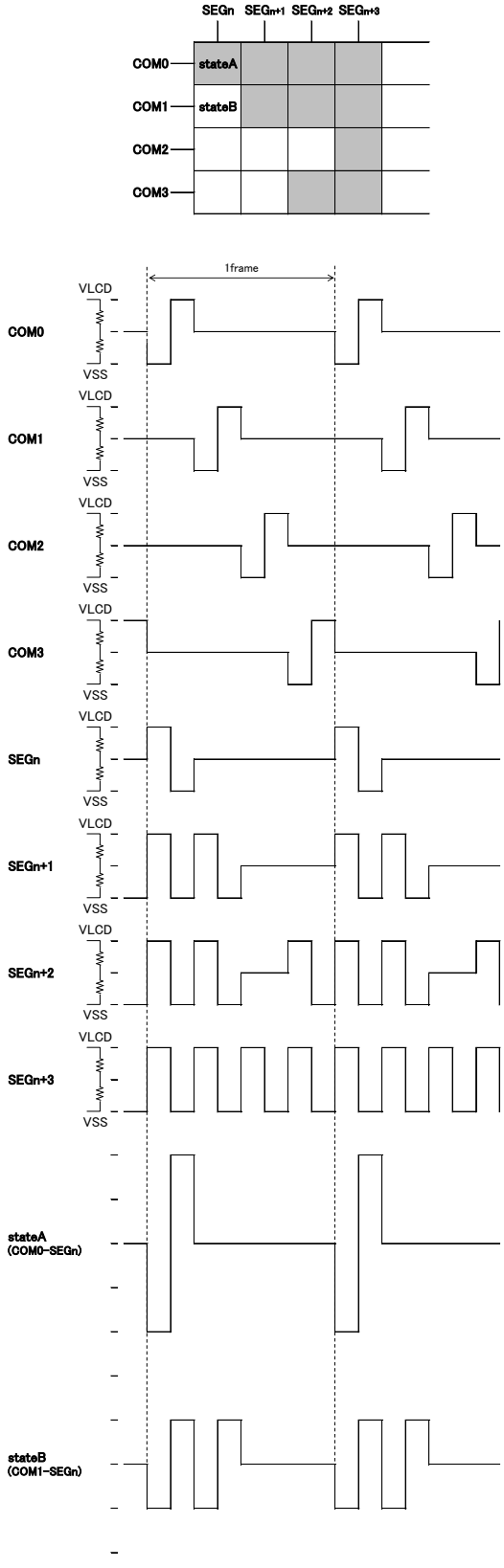


Figure 15.LCD waveform in line inversion (1/2bias)

Frame inversion

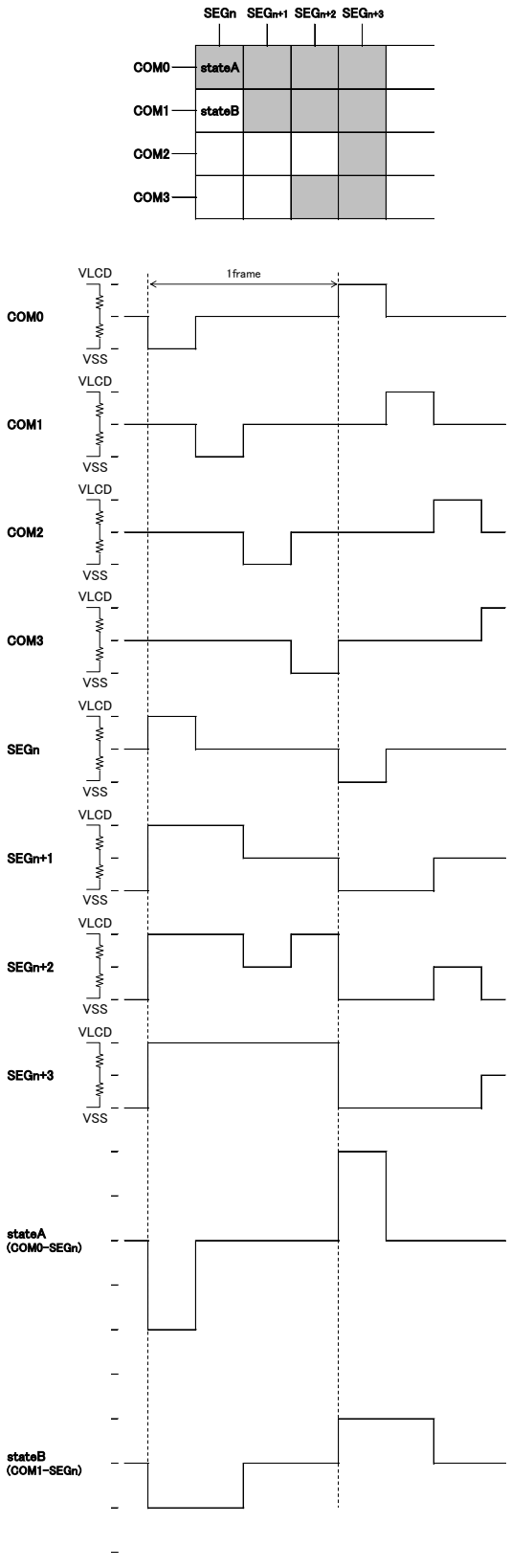


Figure 16. LCD waveform in frame inversion (1/2bias)

●**Example of display data**

If LCD layout pattern is like as Figure 17, Figure 18, and display pattern is like as Figure 19.
Display data will be shown as follows;

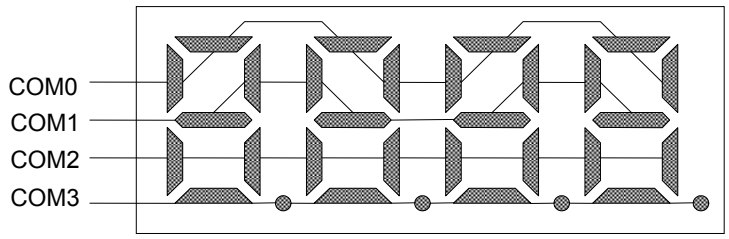


Figure 17. Example of COM line pattern

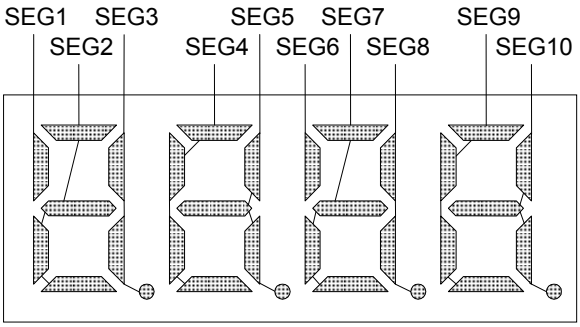


Figure 18. Example SEG line pattern

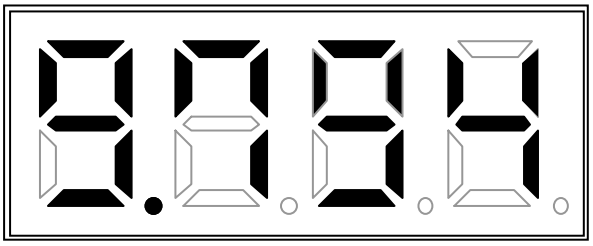


Figure 19. Example Display pattern

<DDRAM data mapping of BU97940AKV display pattern>

		SEG0	SEG1	SEG2		SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18	SEG19
COM0	D0	0	1	1		0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
COM1	D1	0	0	1		1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
COM2	D2	0	0	0		1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0
COM3	D3	0	0	1		1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Address		00h	01h	02h		03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h

●Initialize sequence

Please follow below sequence after Power-on to set BU9794AKV to initial condition.

Power on
↓
CSB ‘H’ … Initialize Interface
↓
CSB ‘L’ …Start interface data transfer
↓
Execute Software Reset by sending SWRST command.

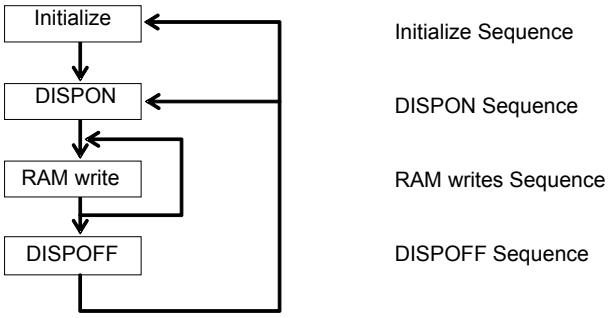
*Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

●Start sequence

○Start sequence example 1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0 to 5V (Tr=0.1ms)
	↓									
2	wait 100us									Initialize IC
	↓									
3	CSB ‘H’									Initialize I/F data
	↓									
4	CSB ‘L’									I/F Data transfer start
	↓									
5	SWRST	1	1	1	0	1	0	1	1	Software Reset
	↓									
6	BLKCTL	1	1	1	1	0	*	0	1	
	↓									
7	MODESET	1	1	0	0	0	1	1	0	
	↓									
8	DISCTL	1	1	0	1	0	0	0	1	
	↓									
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h to 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	address 30h to 31h
11	CSB ‘H’									I/F Data transfer stop
	↓									
12	CSB ‘L’									I/F Data transfer start
	↓									
13	MODESET	1	1	0	0	1	1	1	0	Display ON
	↓									
14	CSB ‘H’									I/F Data transfer stop

○Start sequence example 2



This LSI is initialized with Initialize Sequence and start to display with DISPON Sequence.
This LSI will update display data with RAM write Sequence.
and stop the display with DISPOFF sequence.
If you want to restart to display, this LSI will restart to display with DISPON Sequence.

Initialize sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Power on									
wait 100us									IC is initialized
CSB 'H'									I/F is initialized
CSB 'L'									
SWRST	1	1	1	0	1	0	1	1	Software Reset
MODESET	1	1	0	0	0	0	1	0	Display OFF
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
⋮									
CSB 'H'									

DISPON sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
DISCTL	1	1	0	1	0	0	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	1	0	0	Display ON
CSB 'H'									

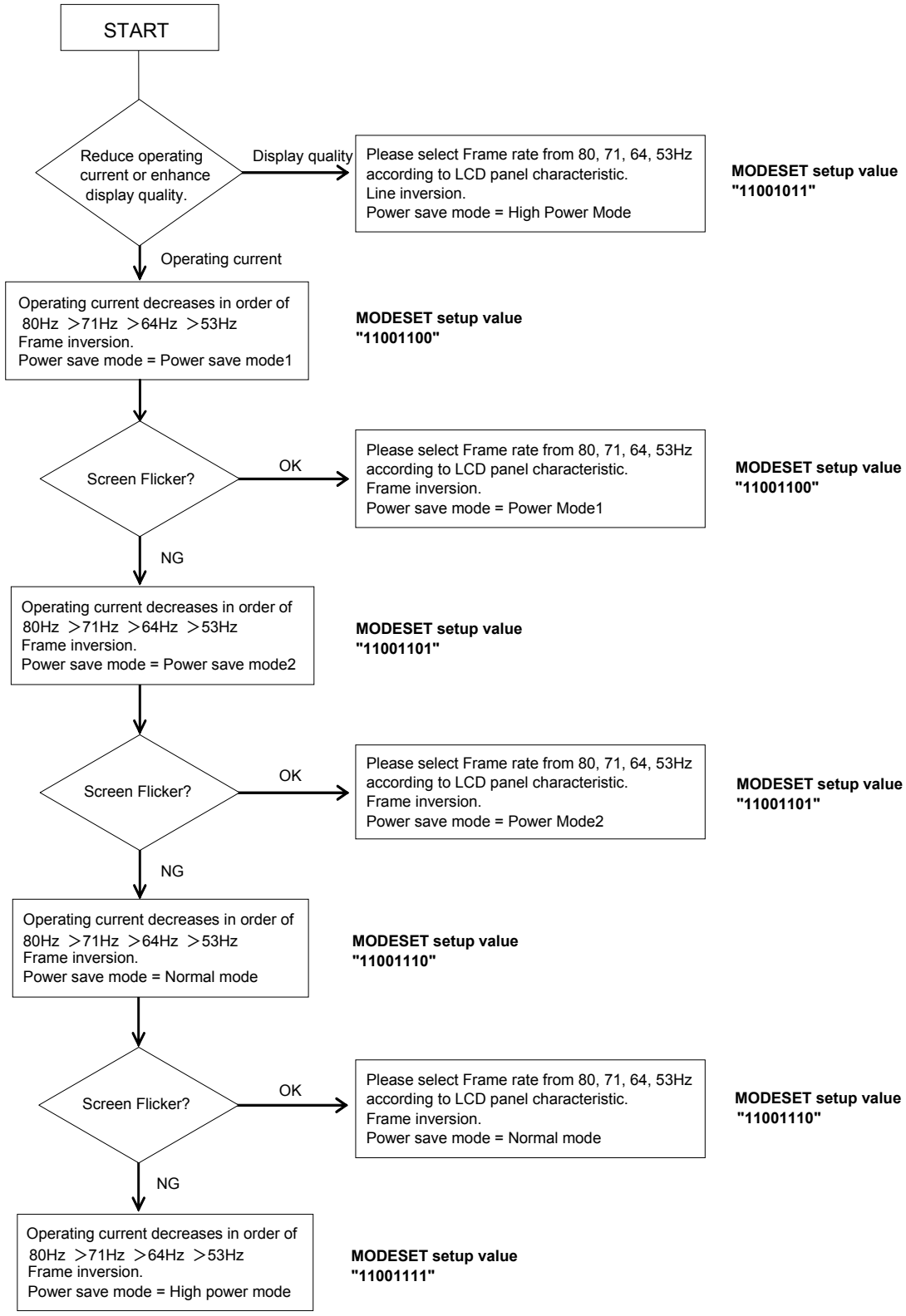
RAM write sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
DISCTL	1	1	0	1	0	0	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	1	0	0	Display ON
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
⋮									
CSB 'H'									

DISPOFF sequence

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
MODESET	1	1	0	0	0	1	0	0	Display OFF
CSB 'H'									

●**MODESET setup flow chart**



●**Cautions on Power ON/OFF**

○Power supply sequence

Please keep Power ON/OFF sequence as below waveform.
To prevent incorrect display, malfunction and abnormal current,
VDD must be turned on before VLCD In power up sequence.
VDD must be turned off after VLCD In power down sequence.
Please satisfies VLCD≥VDD, t1>0ns, t2>0ns

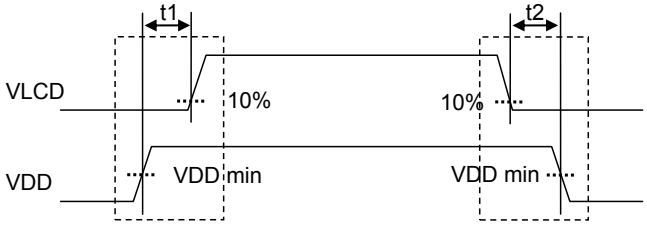
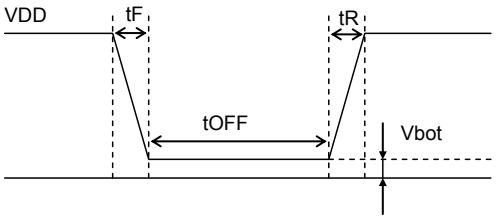


Figure 20. Power supply sequence

○Caution on P.O.R circuit use

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation



Recommended condition of tR, tF, tOFF, Vbot (Ta=25℃)

tR	tF	tOFF	Vbot
Less than 5ms	Less than 5ms	More than 20ms	Less than 0.3V

Figure 21. Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.
Command input is not accepted during power off. It has to take care that software reset is not perfect substitute to POR function.

(1) CSB “L”→ “H”

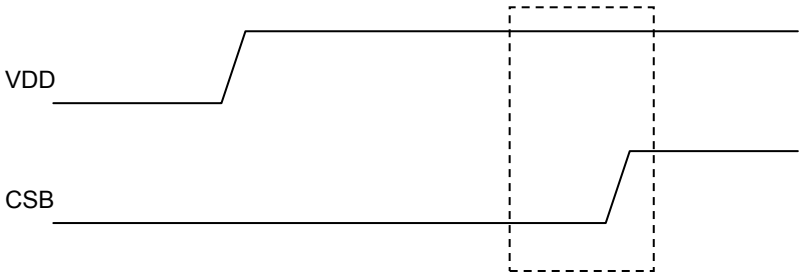


Figure 22. CSB timing

(2) CSB→ “L”, execute SWRST command.

●Operational Notes

(1) Absolute Maximum Ratings
Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(2) Recommended Operating conditions
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(4) Power Supply Lines
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(5) Ground Voltage
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(6) Short between Pins and Mounting Errors
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7) Operation under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8) Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(9) Regarding Input Pins of the IC
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the GND voltage should be avoided. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input terminals have voltages within the values specified in the electrical characteristics of this IC.

(10) GND Wiring Pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

(11) External Capacitor
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

(12) Unused Input Terminals
Input terminals of an IC are often connected to the gate of a CMOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or ground line.

(13) Rush current
When power is first supplied to the IC, rush current may flow instantaneously. It is possible that the charge current to the parasitic capacitance of internal photo diode or the internal logic may be unstable. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●**Ordering Information**

B U 9 7 9 4 A K V	-	E 2

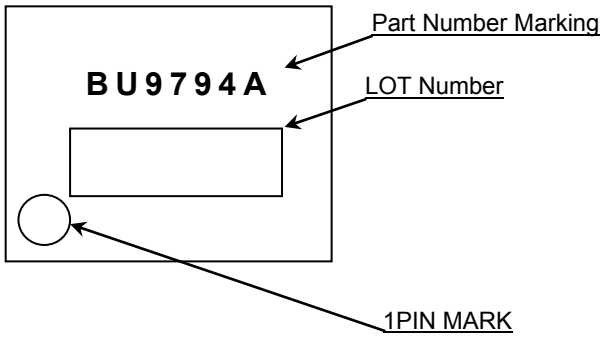
Part Number

Package
KV : VQFP64

Packaging and forming specification
E2: Embossed tape and reel
(VQFP64)

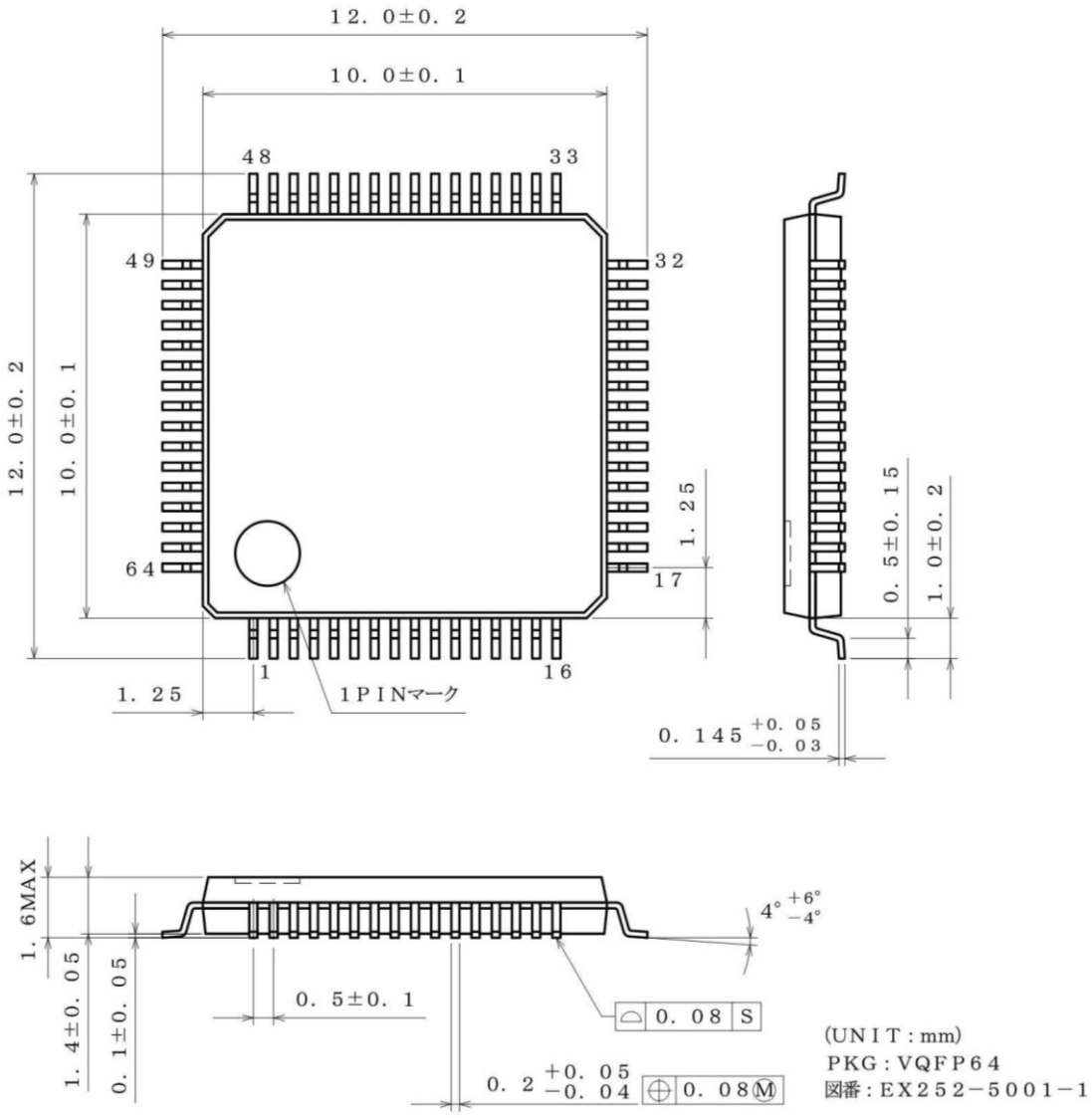
●**Marking Diagram**

VQFP64 (TOP VIEW)



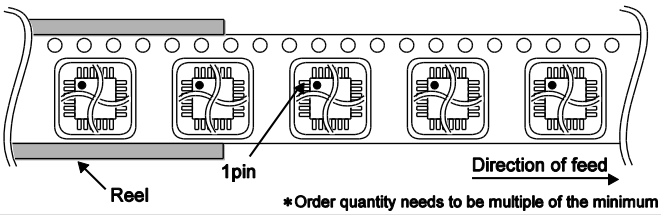
●**Physical Dimension, Tape and Reel Information**

Package Name	VQFP64



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

●**Revision History**

Date	Revision	Changes
14.Mar.2012	001	New Release
8.Jan.2013	002	Improved the statement in all pages. Deleted “Status of this document”. Changed format of Physical Dimension, Tape and Reel Information.
23.Jan.2015	003	Add the condition when power supply in page 18.
10.Apr.2015	004	Add Handling when unused of Pin Description in Page 2. Modified the figure of MODESET setup flow chart in page 17.

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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