A/D Converter Series

Successive Approximation A/D Converter 12 bit, 0.5 MSPS to 1 MSPS, 2.7 V to 5.25 V, 1-channel, SPI Interface

BU79100G-LA

General Description

This is the product guarantees long time support in industrial market.

The BU79100G-LA is a general purpose, 12 bit 1-channel successive approximation AD converter. The sampling rate of BU79100G-LA ranges from 0.5 MSPS to 1 MSPS.

Features

- Long Time Support Product for Industrial Applications
- Maximum 1 MSPS Sampling Rate
- Low Power Consumption
- Small SSOP6 Package Compatible with SOT23-6
- Serial Interface Compatible with SPI/QSPI/MICROWIRE
- Operational Supply Voltage Range: 2.7 V to 5.25 V
- Single-ended Input
- Output Code in Straight Binary Format

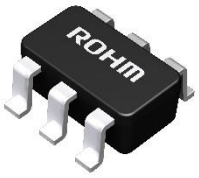
Applications

- Industrial Equipment
- Instrumentation and Control Systems
- Motor Control Systems
- Data Acquisition Systems

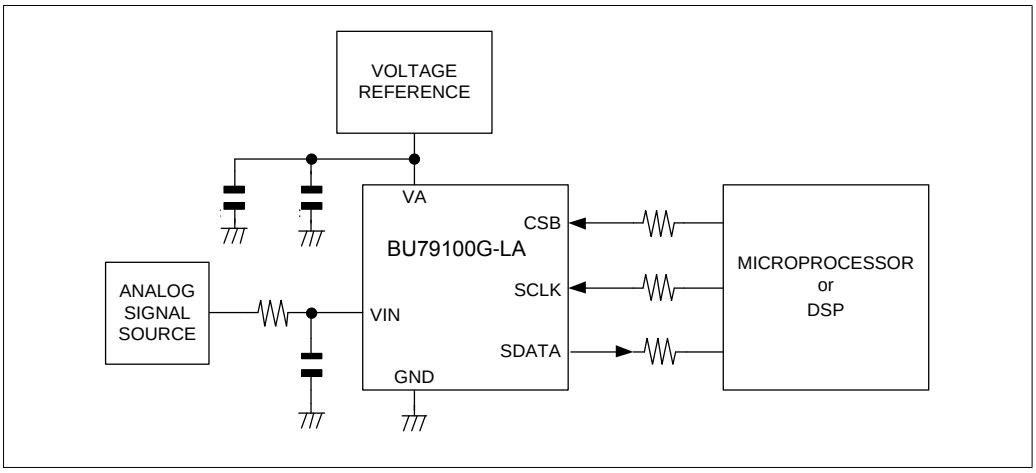
Key Specifications

- Supply Voltage Range: 2.70 V to 5.25 V
- Sampling Rate: 0.5 MSPS to 1.0 MSPS
- Power Consumption:
  (In 1MSPS Operation) 8 mW @V_A = 5 V (Typ)
  1.5 mW @V_A = 3 V (Typ)
- INL: -1.1 LSB to +1.0 LSB
- DNL: -1.0 LSB to +1.0 LSB
- SNR: 71.5 dB @ V_A = 3 V (Typ)
- SINAD: 71.0 dB @ V_A = 3 V (Typ)
- Operating Temperature Range: -40 °C to +85 °C

Package	W (Typ) x D (Typ) x H (Max)
SSOP6	2.9 mm x 2.8 mm x 1.25 mm



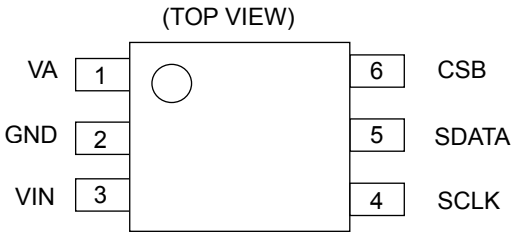
Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

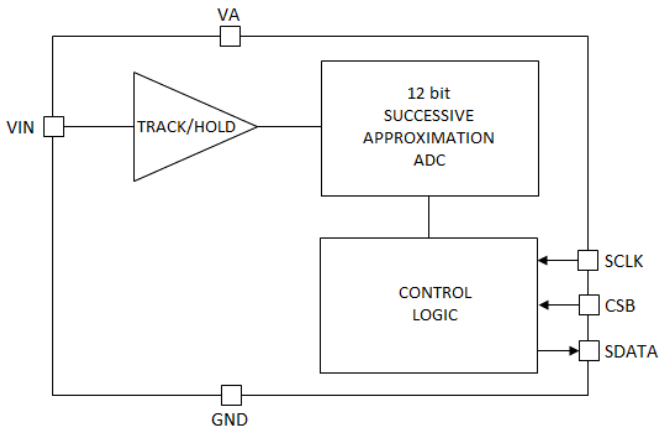
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Function
1	VA	Power supply pin. This voltage is the full scale of the analog input.
2	GND	Ground pin. This voltage level is the zero scale of the analog input.
3	VIN	Analog input pin. The voltage range must be between 0 V and V_A.
4	SCLK	Digital clock input pin.
5	SDATA	Digital data output pin.
6	CSB	Chip select pin. A/D conversion starts at the falling edge of this signal.

Block Diagram



Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_A	5.7	V
Analog Input Voltage	V_{IN}	-0.3 to V_A+0.3	V
Digital Input Voltage	V_{DIN}	-0.3 to +5.7	V
Maximum Junction Temperature	Tjmax	125	°C
Storage Temperature Range	Tstg	-55 to +125	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SSOP6				
Junction to Ambient	θ_{JA}	376.5	185.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	40	30	°C/W

(Note 1) Based on JESD51-2A (Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_A	2.70	-	5.25	V
Analog Input Voltage	V_{IN}	0	-	V_A	V
Digital Input Voltage	V_{DIN}	0	-	5.25	V
Operating Temperature	Topr	-40	+25	+85	°C
Clock Frequency	f_{SCLK}	10	-	20	MHz
Sampling Rate	f_S	0.5	-	1.0	MSPS

Electrical Characteristics

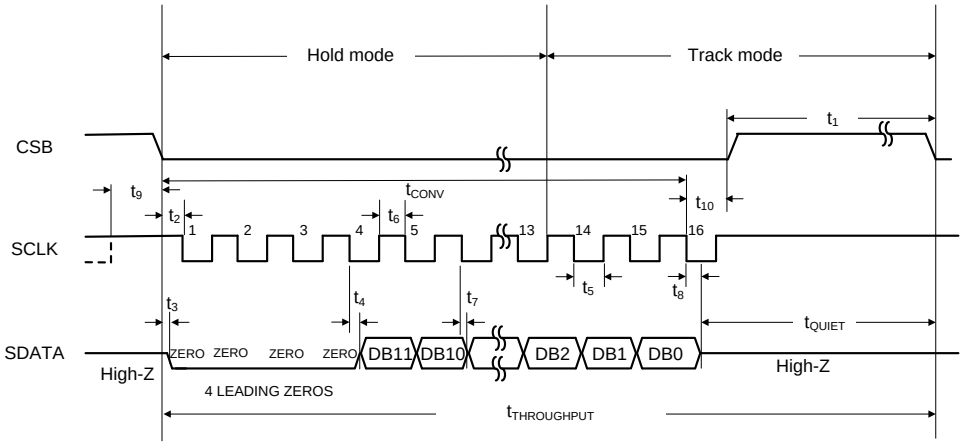
Unless otherwise specified, Ta = -40 °C to +85 °C (typical: Ta = 25 °C), V_A = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, f_S = 1 MSPS

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Statistic Converter Characteristics						
Resolution with No missing codes	R_{ES}	-	12	-	bit	V_A = 2.7 V to 3.6 V
Integral Non-linearity	I_{NL}	-1.1	-	+1.0	LSB	V_A = 2.7 V to 3.6 V, 25 °C
Differential Non-linearity	D_{NL}	-1.0	-	+1.0	LSB	V_A = 2.7 V to 3.6 V, 25 °C
Offset Error	O_E	-1.2	±0.2	+1.2	LSB	V_A = 2.7 V to 3.6 V, 25 °C
Gain Error	G_E	-1.2	±0.3	+1.2	LSB	V_A = 2.7 V to 3.6 V, 25 °C
Dynamic Converter Characteristics (f_{IN} = 100 kHz, V_{IN} = -0.02 dBFS)						
Signal to Noise and Distortion Ratio1	S_{INAD1}	70	71	-	dB	V_A = 2.7 V to 3.6 V, 25 °C
Signal to Noise and Distortion Ratio2	S_{INAD2}	68	70	-	dB	V_A = 4.75 V to 5.25 V, 25 °C
Signal to Noise Ratio1	S_{NR1}	70.8	71.5	-	dB	V_A = 2.7 V to 3.6 V, 25 °C
Signal to Noise Ratio2	S_{NR2}	68.8	71.0	-	dB	V_A = 4.75 V to 5.25 V, 25 °C
Total Harmonic Distortion	T_{HD}	-	-80	-	dB	V_A = 2.7 V to 3.6 V
Spurious-free Dynamic Range	S_{FDR}	-	82	-	dB	V_A = 2.7 V to 3.6 V
Effective Number of Bits1	E_{NOB1}	11.3	11.5	-	bit	V_A = 2.7 V to 3.6 V, 25 °C
Effective Number of Bits2	E_{NOB2}	11.0	11.3	-	bit	V_A = 4.75 V to 5.25 V, 25 °C
Inter-modulation Distortion1 (Second Order Term)	I_{MD1}	-	-78	-	dB	V_A = 5.25 V, 103.5 kHz, 113.5 kHz
Inter-modulation Distortion2 (Third Order term)	I_{MD2}	-	-76	-	dB	V_A = 5.25 V, 103.5 kHz, 113.5 kHz
Full Power Band Width1	f_{PBW1}	-	10.1	-	MHz	V_A = 5 V
Full Power Band Width2	f_{PBW2}	-	7.2	-	MHz	V_A = 3 V
Aperture Delay	t_{AD}	-	4.3	-	ns	V_A = 5 V
Aperture Jitter	t_{AJ}	-	30	-	ps	V_A = 5 V
Clock Frequency	f_{SCLK}	10	-	20	MHz	
Sampling Rate	f_S	500 k	-	1 M	SPS	
Track/Hold Acquisition Time	t_{ACQ}	-	-	350	ns	
Analog Input Characteristics						
Input Voltage Range	V_{IN}	0	-	V_A	V	
Input DC Leakage Current	I_{LEAK}	-1.0	±0.1	+1.0	µA	V_{IN} = 0 V or V_A
Input Capacitance1	C_{INA1}	-	28	-	pF	track mode, V_A = 5 V
Input Capacitance2	C_{INA2}	-	4	-	pF	hold mode, V_A = 5 V
Digital Input Characteristics						
High Input Voltage1	V_{IH1}	2.4	-	-	V	V_A = 5.25 V
High Input Voltage2	V_{IH2}	2.1	-	-	V	V_A = 3.6 V
Low Input Voltage1	V_{IL1}	-	-	0.8	V	V_A = 5 V
Low Input Voltage2	V_{IL2}	-	-	0.4	V	V_A = 3 V
Input Current	I_{IND}	-1.0	±0.1	+1.0	µA	V_{IND} = 0 V or V_A
Input Capacitance	C_{IND}	-	2.5	-	pF	
Digital Output Characteristics						
Output High Voltage1	V_{OH1}	V_A-0.20	V_A-0.03	-	V	I_{SOURCE} = 200 µA
Output High Voltage2	V_{OH2}	-	V_A-0.1	-	V	I_{SOURCE} = 1 mA
Output Low Voltage1	V_{OL1}	-	0.02	0.40	V	I_{SINK} = 200 µA
Output Low Voltage2	V_{OL2}	-	0.1	-	V	I_{SINK} = 1 mA
High-Z Leakage Current	I_{OZ}	-10.0	±0.1	+10.0	µA	V_{OZ} = 0 V or V_A
High-Z Output Capacitance	C_{OUT}	-	2	-	pF	
Current Consumption						
Operational Current Consumption1	I_{A1}	-	1.6	2.8	mA	V_A = 5.25 V, f_S = 1 MSPS
Operational Current Consumption2	I_{A2}	-	0.5	1.2	mA	V_A = 3.6 V, f_S = 1 MSPS

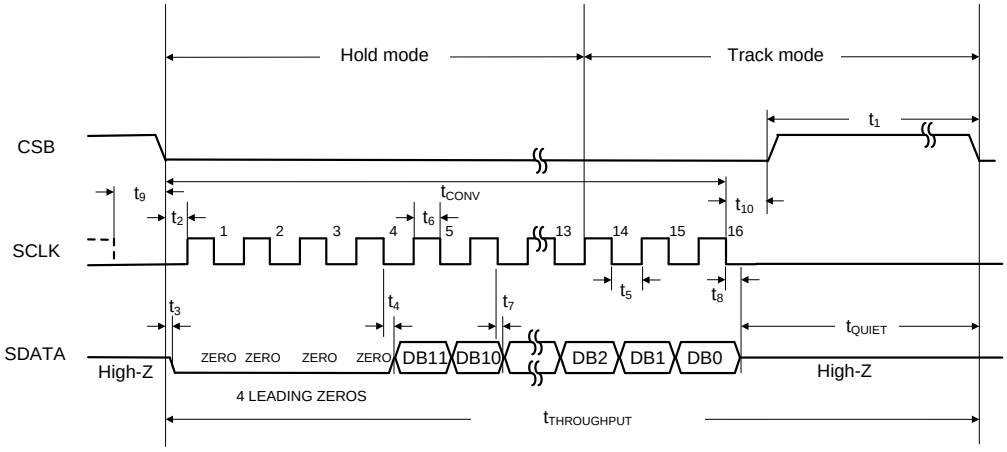
Timing Specifications

Unless otherwise specified, Ta = -40 °C to +85 °C (Typical: Ta = 25 °C), V_A = 2.7 V to 5.25 V, f_{SCLK} = 10 M to 20 MHz, C_L = 25 pF

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Conversion Time	t_{CONV}	-	16	-	SCLK	
CSB Pulse Width	t_1	10	-	-	ns	
CSB Setup Time	t_2	10	-	-	ns	
SDATA Enable Time	t_3	-	-	20	ns	
SDATA Access Time1	t_4	-	-	40	ns	V_A = 2.7 V to 3.6 V
SDATA Access Time2	t_4	-	-	20	ns	V_A = 4.75 V to 5.25 V
SCLK Low Pulse Width	t_5	0.4xt_{SCLK}	-	-	ns	
SCLK High Pulse Width	t_6	0.4xt_{SCLK}	-	-	ns	
SDATA Hold Time1	t_7	7	-	-	ns	V_A = 2.7 V to 3.6 V
SDATA Hold Time2	t_7	5	-	-	ns	V_A = 4.75 V to 5.25 V
SDATA Disable Time1	t_8	6	-	25	ns	V_A = 2.7 V to 3.6 V
SDATA Disable Time2	t_8	5	-	25	ns	V_A = 4.75 V to 5.25 V
CSB Hold Time	t_9	10	-	-	ns	
SCLK Setup Time	t_{10}	10	-	-	ns	
Quiet Time	t_{QUIET}	50	-	-	ns	
Power-Up Time	t_{POWUP}	-	1	-	µs	
Throughput Period	$t_{THROUGHPUT}$	1	-	20	µs	



(a) If SCLK is high at the falling edge of CSB



(b) If SCLK is low at the falling edge of CSB

Figure 1. Serial Interface Timing Chart

(Note 5) When the BU79100G-LA is used at the sampling frequency of 1 MSPS, it is recommended to hold SCLK high at the falling edge of CSB as shown in Figure 1(a). (See also "3. Serial Interface" on page 13.)

Term Definitions

ACQUISITION TIME:
At the 13th rising edge of SCLK, the mode is changed from Hold mode to Track mode and the sampling capacitor starts to be charged. It is the time when the voltage of the sampling capacitor equals input voltage from the charge start.

APERTURE DELAY:
It is defined as the time when the input voltage is held since a sampling capacitor was separated with outside by a falling edge of CSB.

APERTURE JITTER:
The variation in the aperture delays in sampling operations. Aperture jitter gets to affect output noise.

INTEGRAL NON-LINEARLITY (INL):
It is a measure of the deviation of each individual code from a line drawn from zero scale (0.5 LSB below the first code transition) through full scale (0.5 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

DIFFERENTIAL NON-LINEARLITY (DNL):
It is the measure of the maximum deviation from the ideal step size of 1 LSB.

OFFSET ERROR (OE):
It is the deviation of the first code transition “(000…000) to (000…001)” from the ideal of 0.5 LSB.

FULL SCALE ERROR (FSE):
It is the deviation of the last code transition “(111…110) to (111…111)” from the ideal of “V_A–1.5 LSB”.

GAIN ERROR (GE):
It is defined as full scale error minus offset error.

TOTAL HARMONIC DISTORTION (THD):
It is the ratio, expressed in dB or dBc, of the RMS total of the first five harmonic components at the output to the RMS level of the input signal frequency as seen at the output. THD is calculated as

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

where A_{f1} is the RMS power of the input frequency at the output and A_{f2} through A_{f6} are the RMS power in the first 5 harmonic frequencies.

SIGNAL TO NOISE AND DISTORTION RATIO (SINAD):
It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, including harmonics but excluding DC component.

EFFECTIVE NUMBER OF BITS (ENOB):
It is another method of specifying Signal to Noise and Distortion Ratio. ENOB is defined as “(SINAD–1.76) / 6.02” and says that the converter is equivalent to a perfect A/D converter of this number of bits.

SIGNAL TO NOISE RATIO (SNR):
It is the ratio, expressed in dB, of the RMS value of the input signal to the RMS value of all other spectral components below half the sampling frequency, not including harmonics and DC component.

SPURIOUS FREE DYNAMIC RANGE (SFDR):
It is the difference, expressed in dB, between the RMS value of the input signal to the RMS value of the peak spurious spectral component, where a peak spurious spectral component is any spurious signal present in the output spectrum that is not present at the input.

CONVERSION TIME:
It is the required time for the A/D converter to convert the input signal to the digital code.

THROUGHPUT PERIOD:
It is the period that should be used as an interval time between any adjacent conversions.

Typical Performance Curves

(Reference Data)

Unless otherwise noted, Ta = 25 °C.

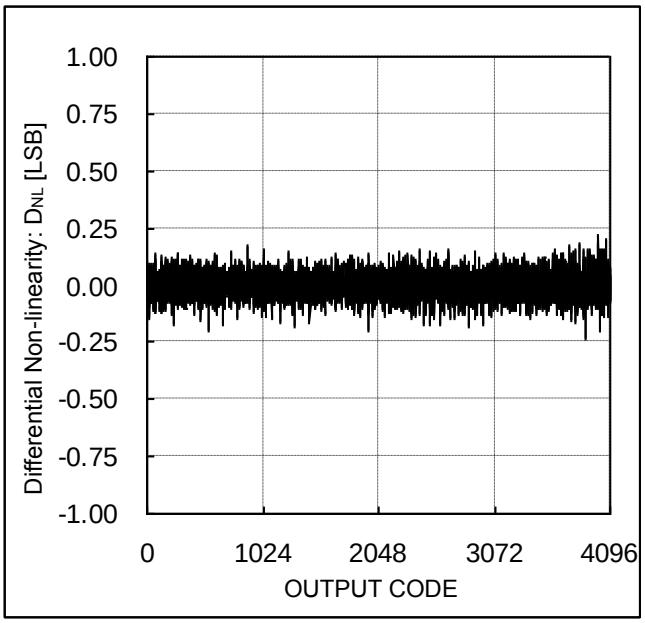


Figure 2. Differential Non-linearity vs OUTPUT CODE
(V_A = 3 V, f_{SCLK} = 10 MHz, f_S = 500 kSPS)

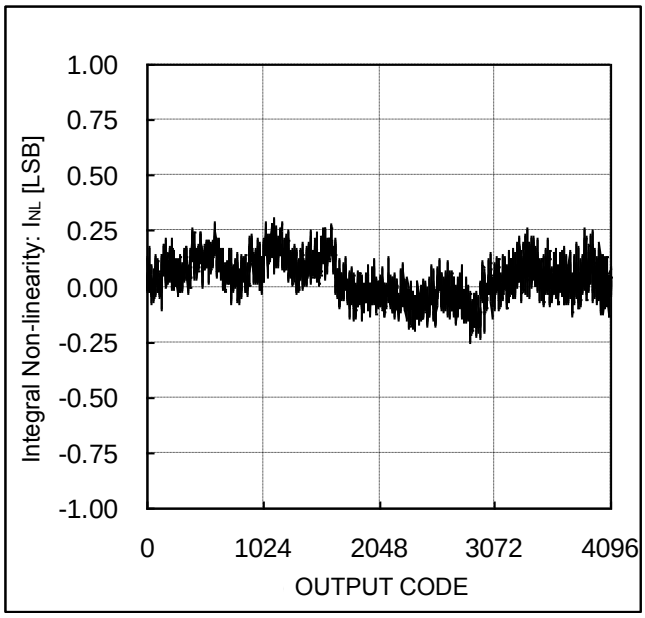


Figure 3. Integral Non-linearity vs OUTPUT CODE
(V_A = 3 V, f_{SCLK} = 10 MHz, f_S = 500 kSPS)

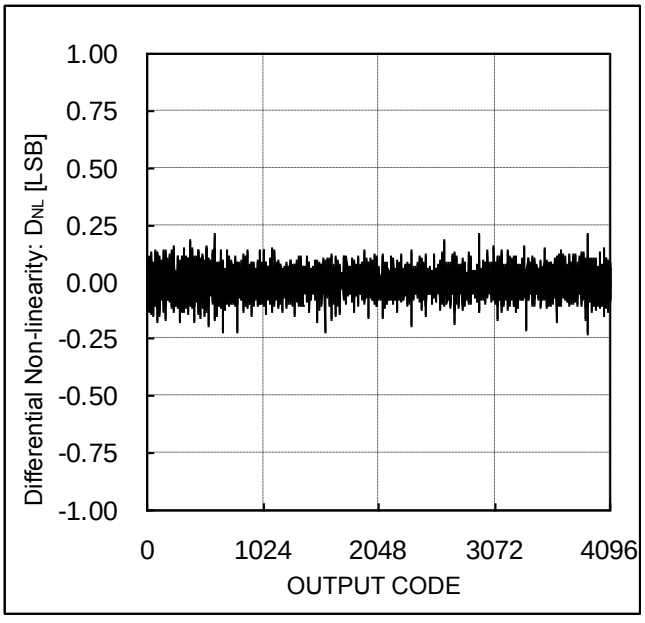


Figure 4. Differential Non-linearity vs OUTPUT CODE
(V_A = 3 V, f_{SCLK} = 20 MHz, f_S = 1 MSPS)

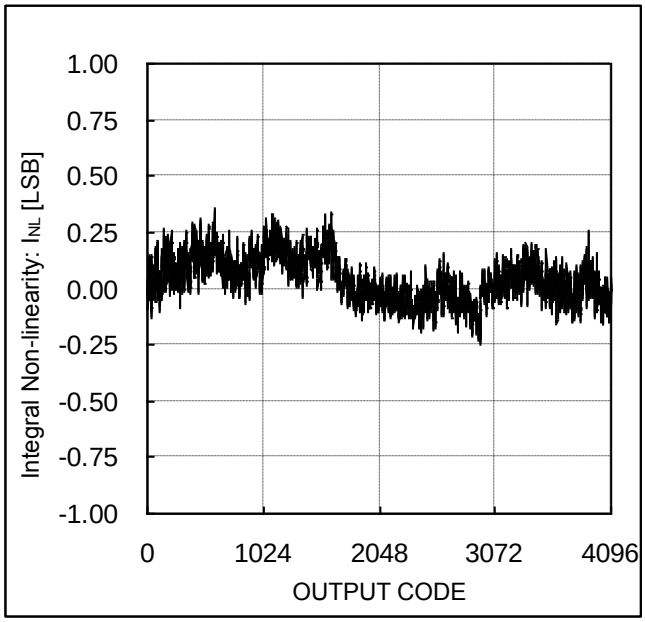


Figure 5. Integral Non-linearity vs OUTPUT CODE
(V_A = 3 V, f_{SCLK} = 20 MHz, f_S = 1 MSPS)

Typical Performance Curves – continued

(Reference Data)

Unless otherwise noted, Ta = 25 °C, f_{IN} = 100 kHz.

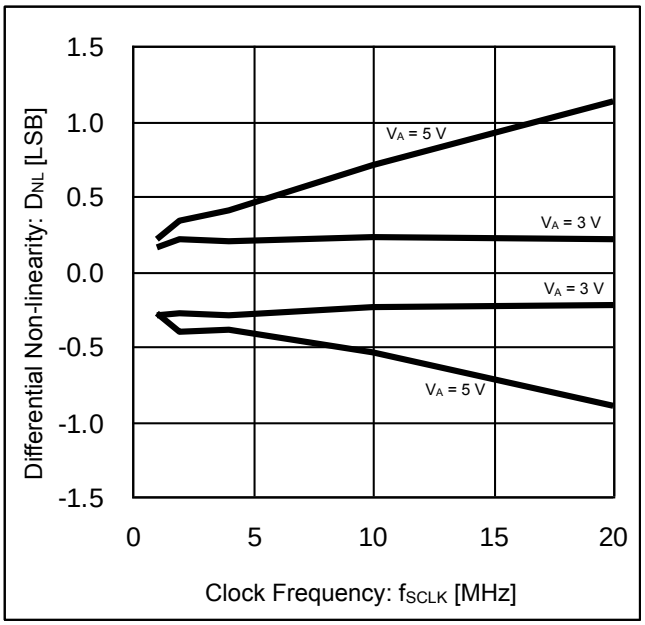


Figure 6. Differential Non-linearity vs Clock Frequency

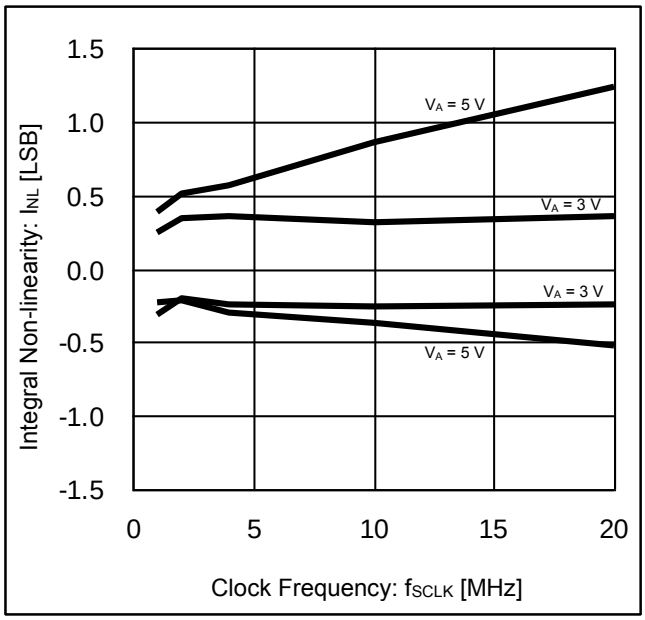


Figure 7. Integral Non-linearity vs Clock Frequency

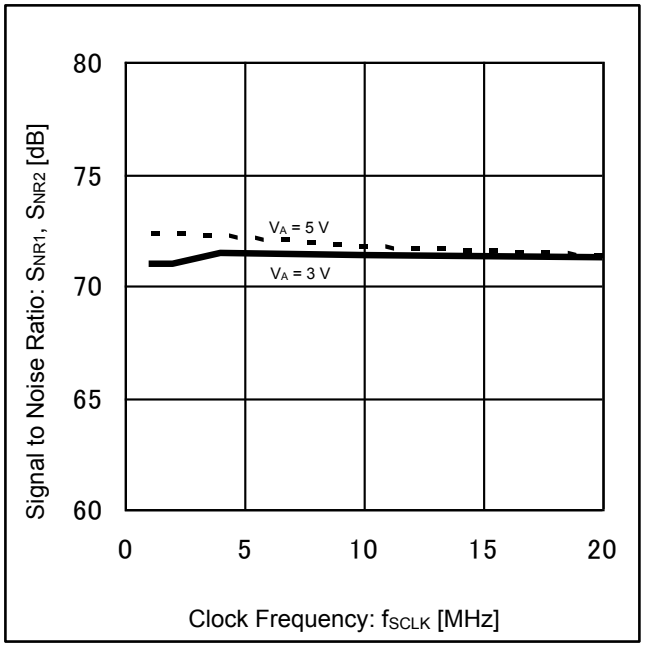


Figure 8. Signal to Noise Ratio vs Clock Frequency

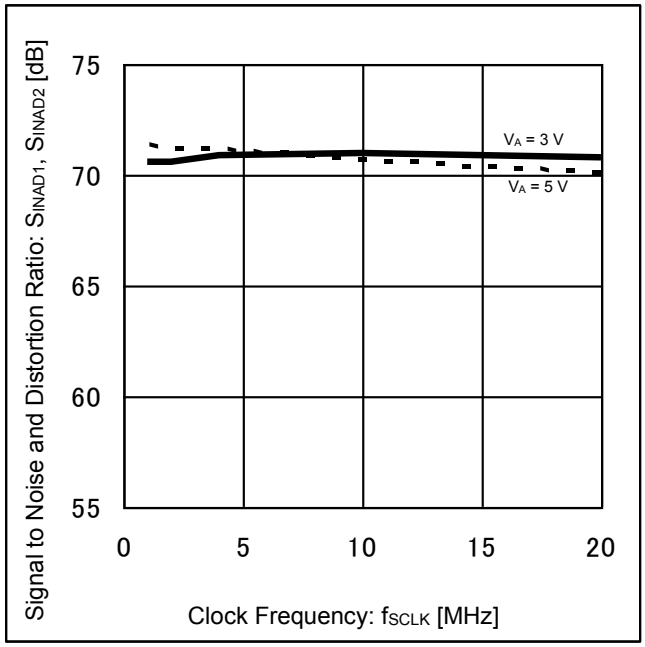


Figure 9. Signal to Noise and Distortion Ratio vs Clock Frequency

Typical Performance Curves – continued

(Reference Data)

Unless otherwise noted, Ta = 25 °C, f_{IN} = 100 kHz.

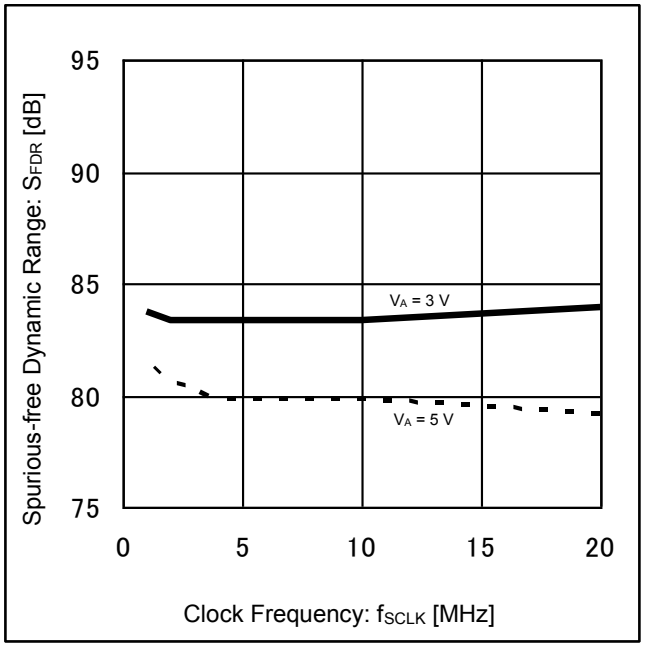


Figure 10. Spurious-free Dynamic Range vs Clock Frequency

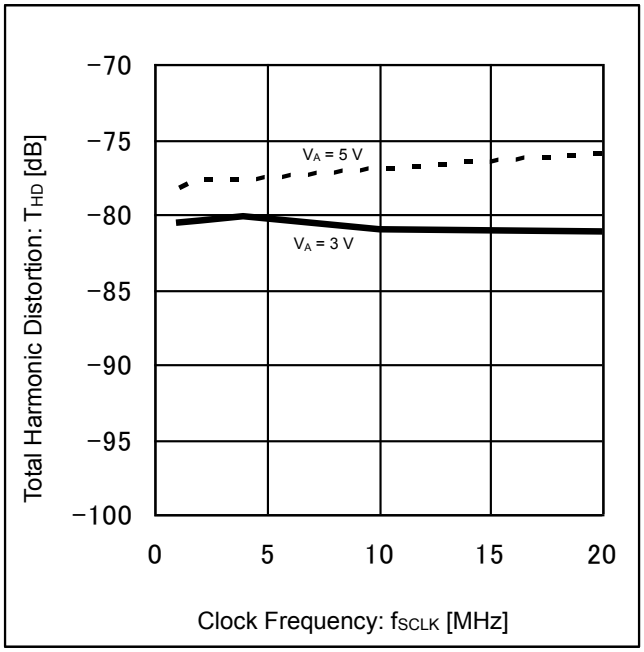


Figure 11. Total Harmonic Distortion vs Clock Frequency

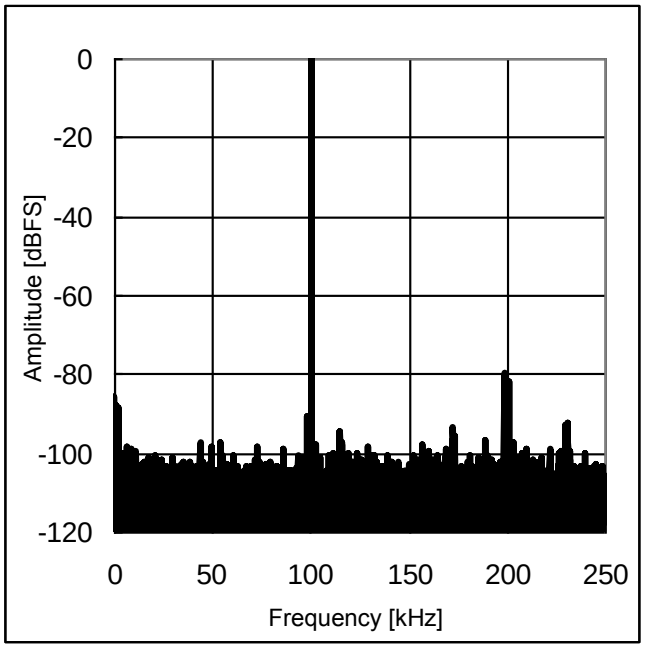


Figure 12. Amplitude vs Frequency
(V_A = 5 V, f_{SCLK} = 10 MHz, f_S = 500 kSPS)

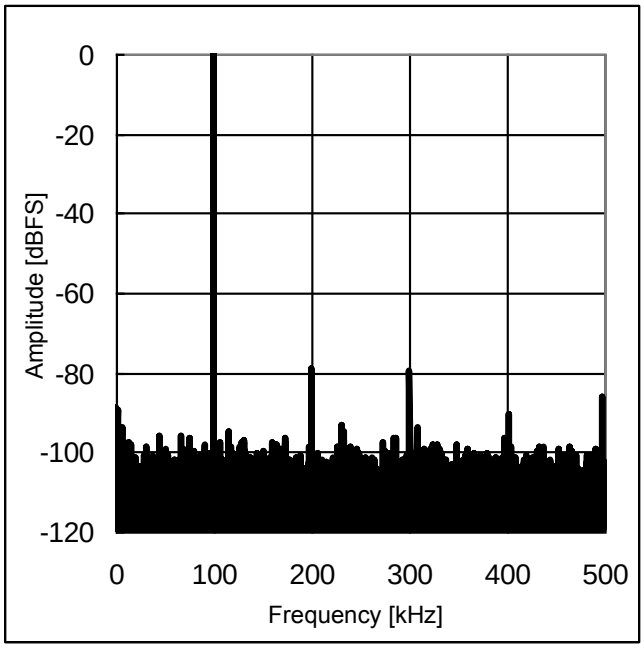


Figure 13. Amplitude vs Frequency
(V_A = 5 V, f_{SCLK} = 20 MHz, f_S = 1 MSPS)

Description of Functions

1. Overview of A/D Conversion Process

BU79100G-LA is a successive-approximation A/D converter designed with a charge-redistribution D/A converter. Simplified schematics of the A/D converter are shown in Figure 14 and Figure 15.

Figure 14 shows the A/D converter in Track mode: the switch SW1 is in the position A, SW2 is closed and balances the comparator. Then, the sampling capacitor is charged with the analog input voltage V_{IN}.

Figure 15 shows the A/D converter in Hold mode. When a conversion starts, the A/D converter goes into Hold mode: SW2 becomes open, SW1 connects the sampling capacitor to ground through the pin B and the comparator loses its balance. The control logic controls the input voltage of the comparator via the sampling capacitors of the charge-redistribution D/A converter to get the comparator back into a balanced state. A/D conversion finishes when the comparator balances again. The control logic also generates the output code of the A/D converter.

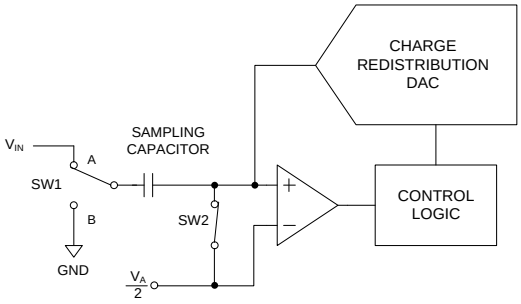


Figure 14. Track mode

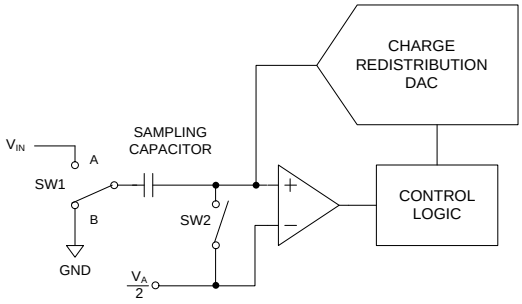


Figure 15. Hold mode

2. Ideal Transfer Characteristics

Figure 16 shows the ideal transfer characteristics of BU79100G-LA. Code transitions occur midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB, and so on. The LSB size for the BU79100G-LA is V_A / 4096. The output code format of the A/D converter is straight binary.

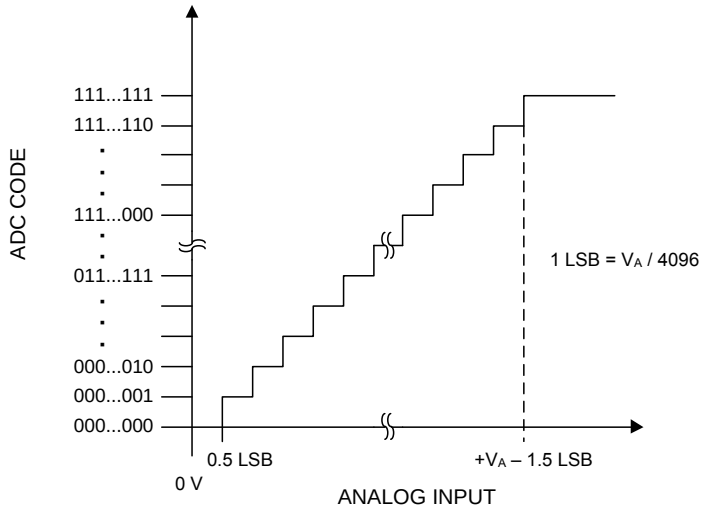


Figure 16. Ideal Transfer Characteristics

Description of Functions – continued

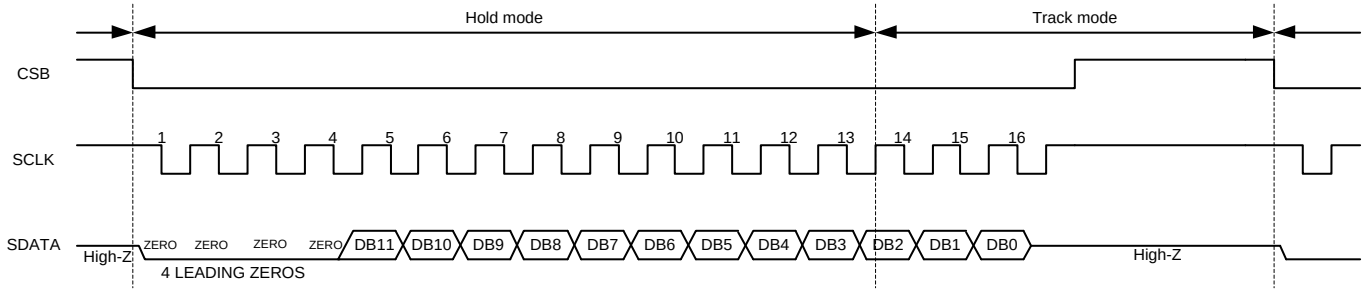
3. Serial Interface

The serial interface timing is shown in Figure 17. When CSB goes low, both a conversion process and data transfer are started. At the falling edge of CSB, SDATA changes its state from High-Z to Low, the converter moves from Track mode to Hold mode. A tracked input signal is sampled and held for conversion at this point. The converter returns from Hold mode back to Track mode at the rising edge of SCLK subsequent to the 13th falling edge of it. SDATA goes back to High-Z at the 16th falling edge of SCLK or at the rising edge of CSB. After a conversion, the quiet time t_{QUIET} must be satisfied before the next conversion triggered by the falling edge of CSB.

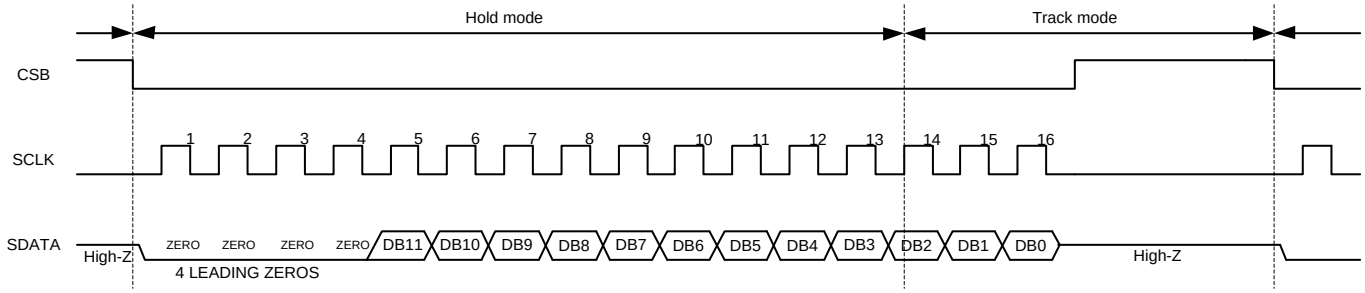
Sixteen SCLK cycles are needed to read a complete data of the A/D conversion from BU79100G-LA. First, four leading zeros come out from SDATA. Then, the 12 bit data comes out bit by bit, starting from the MSB. The first zero is clocked out at the falling edge of CSB. The remaining leading 3 zeros and data bits are clocked out to SDATA at the falling edge of SCLK; the host IC, the receiver of the A/D conversion data, is intended to receive the data at the subsequent falling edge of SCLK.

To perform A/D conversion properly, the BU79100G-LA needs at least 16 SCLK cycles while CSB is low. If an A/D conversion is interrupted in the middle of the conversion with CSB going to high before the 16th SCLK falling edge, the following A/D conversion may not be performed normally. Therefore, it is necessary that equal to or more than 16 falling edges of SCLK exist while CSB is low.

In addition, SCLK should be held either high or low at the falling edge of CSB. If SCLK is low at the falling edge of CSB, as shown in Figure 17(b), a Hold mode time length is about a half clock period longer than one if SCLK is high as shown in Figure 17(a). Therefore, when the BU79100G-LA is used at the sampling frequency of 1 MSPS, it is recommended to hold SCLK high at the falling edge of CSB, as shown in Figure 17(a), in order to ensure sufficient Track mode time for the maximum acquisition time.



(a) If SCLK is high at the falling edge of CSB



(b) If SCLK is low at the falling edge of CSB

Figure 17. Serial Interface Timing

Description of Functions – continued

4. Dummy Conversion
Dummy conversions are necessary in the following cases.

(1) A/D conversion after power-up
The first A/D conversion data after applying power to the BU79100G-LA is invalid. Therefore, a dummy conversion is necessary after power-up. In addition, the power-up time is satisfied with a cycle of the dummy conversion.

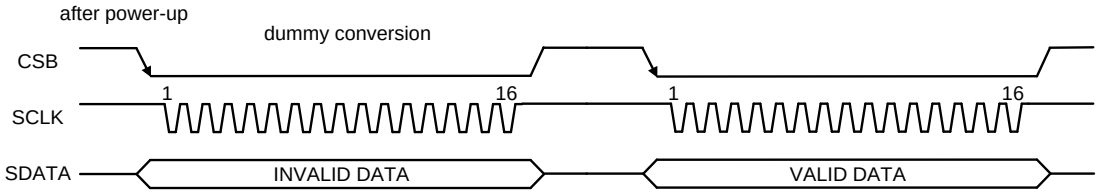


Figure 18. A/D conversion after power-up

(2) A/D conversion after a stop period more than the maximum throughput time
The BU79100G-LA may stop performing A/D conversion between some A/D conversion cycles. If the maximum limit of the throughput period of 20 µs is violated, the first A/D conversion data after the resumption is not valid similar to the case after power-up. Therefore, a dummy conversion cycle is necessary.

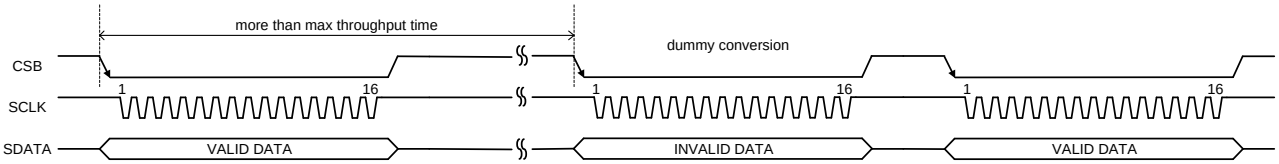


Figure 19. A/D conversion after a long suspension

Application Example

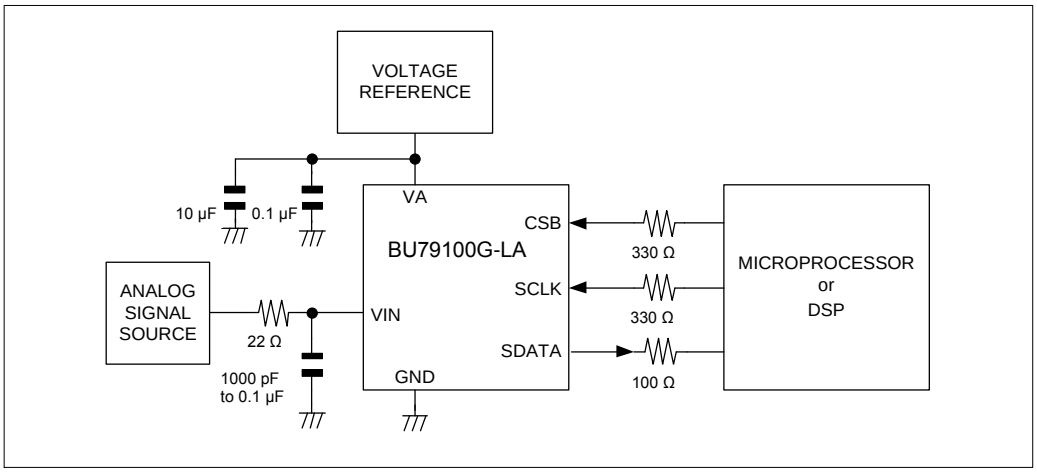


Figure 20. Application Circuit

As shown in Figure 20, a power supply pin connects voltage source and put two bypass capacitors for the high frequency and low frequency noise between VA and GND to make the maximum use of the A/D converter's capability. Ceramic capacitors of 0.1 µF and 1 µF to 10 µF are to be used as bypass capacitor for BU79100G-LA. Especially, the capacitor of 0.1 µF should be placed as close to the VA pin of BU79100G-LA as possible.
Because the voltages of VA and GND are used as the reference voltages for the A/D converter, the deviation of the supply voltage directly affects the full scale and has much influence on its characteristics. Therefore, the fully stable supply voltage should be connected to VA.

The output impedance of the analog input signal source should be small enough. Charge in the sampling capacitor is swept out to the VIN pin at the transition from Hold mode to Track mode because of the difference of the voltage between the input signal voltage and the sampling capacitor voltage. This charge could cause undesirable voltage deviation. If influence of the deviation remains at the transition from Track mode to Hold mode, it could cause the conversion error.
If a buffer amplifier is used to get low output impedance, high-speed response is required of the buffer amplifier. A decoupling capacitor and a resister on the VIN analog input could support the amplifier to reduce the influence of the charge.

The voltage fluctuation on the supply and ground pins is caused by the charge and discharge of the digital input and output pins through the digital signals. This fluctuation can be reduced by inserting resisters serially to the digital input and output pins. The resistance values must be small enough not to cause critical delay errors. It is more effective to place these resisters as close to the digital pins as possible.

I/O Equivalence Circuit

(1) Analog Input Pin

The equivalent analog input circuit is shown in Figure 21. The diodes, D_1 and D_2, are placed for ESD protection. If the analog input voltage is more than "V_A+0.3 V", or less than "GND–0.3 V", these diodes are turned on and forward current is generated. This current might cause malfunction or irreversible damage to BU79100G-LA. The capacitance value of the C_1 in Figure 21 is typically 4 pF, derived from the package parasitic capacitance. The R_1 is the resistance of the track/hold switch, typically 500 Ω. The C_2 is the sampling capacitance of BU79100G-LA, and the capacitance value is typically 24 pF.

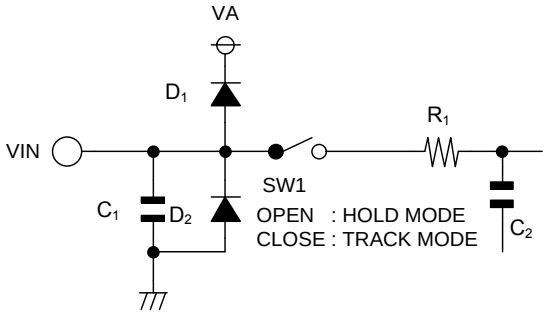


Figure 21. Analog Input Equivalent Circuit

(2) Digital Input and Output Pins

The equivalent digital input circuit is shown in Figure 22. Digital input pins, CSB and SCLK, don't have any diodes to VA. Thus, the maximum rating of "V_A+0.3 V" is not applied to these digital input pins. Digital input voltage range is 5.25 V in ground reference regardless of the supply voltage V_A. This enables BU79100G-LA to be interfaced with a wide range of logic levels, independent of the supply voltage.

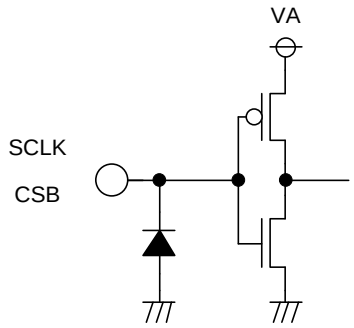


Figure 22. Equivalent Digital Input Circuit

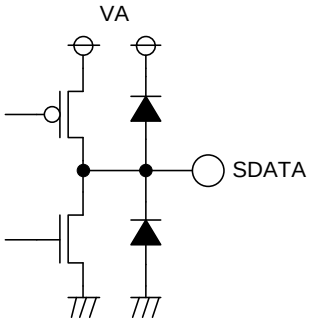


Figure 23. Equivalent Digital Output Circuit

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

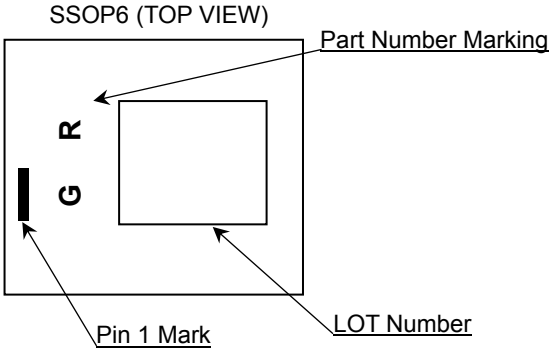
Ordering Information

B U 7 9 1 0 0 G - L A T R

Package
G: SSOP6

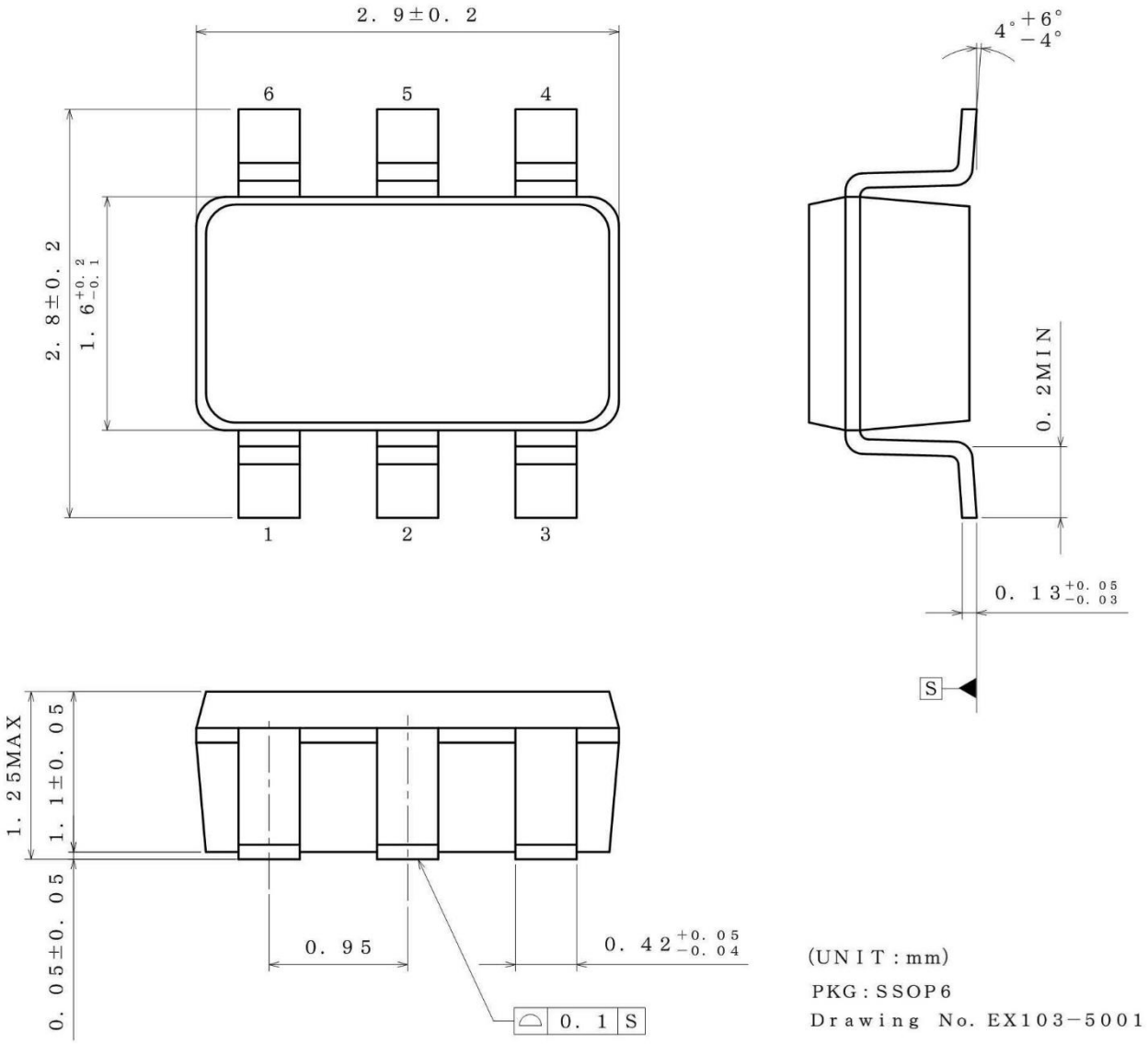
Product Class
LA: for Industrial Applications
Packaging and forming specification
TR: Embossed tape and reel

Marking Diagram



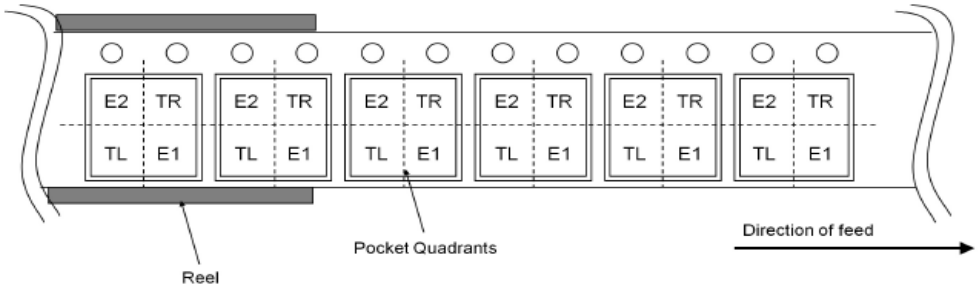
Physical Dimension and Packing Information

Package Name	SSOP6



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
05.Feb.2021	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

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