Datasheet

600V High Voltage 3 Phase Bridge Driver Integrated Bootstrap Diode

BS2132F

General Description

The BS2132F is a monolithic bridge driver IC, which can drive external Nch-FET and IGBT driver in 3 phase systems with bootstrap operations. 600V high voltage bootstrap diode is integrated between the VCC pin and the VB pins.
The logic inputs can be used 3.3V and 5.0V.
As a protection function, the device includes an Undervoltage Lockout (UVLO) circuit between VCC-COM and between VB-VS and an Over Current Protection (OCP) circuit.
In addition, the /FAULT pin outputs a protection detecting signal, and the RCIN pin can determine the OCP holding time by external resistance and capacitance.

Features

- High-Side Floating Supply Offset Voltage Range to 600V
- Gate Drive Supply Range from 11.5V to 20V
- Integrated 600V High Voltage Bootstrap Diode between the VCC pin and the VB pin
- Built-in Undervoltage Lockout (UVLO) for Both Channels
- Built-in High Precision (0.46V±5%) Over Current Protection (OCP) Circuit
- Built-in the Enable Pin (EN) which Enable I/O Functionality
- Built-in the /FAULT pin which is Protection Detecting Signals (OCP and UVLO) output pin
- RCIN Pin can determine the OCP holding time by External Resistance and Capacitance
- 3.3V and 5.0V Input Logic Compatible
- Output in Phase with Input

Applications

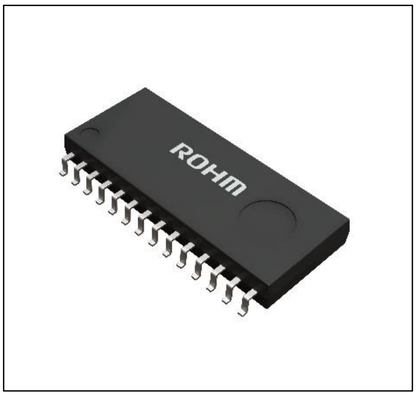
- MOSFET and IGBT Driver Applications

Key Specifications

■High-Side Floating Supply Offset Voltage:	600V
■Input Voltage Range:	11.5V to 20V
■Output Current I_{O+}/I_{O-}:	200mA/350mA(Typ)
■Bootstrap Diode Current Limit Resistance:	28Ω(Typ)
■OCP Detect Voltage:	0.46V(Typ)
■OCP Blanking Time:	150ns(Typ)
■Turn-on/Turn-off Time:	630ns/580ns(Typ)
■Offset Supply Leakage Current:	50µA(Max)
■Operating Temperature Range:	-40°C to +125°C

Package

Package	W(Typ) x D(Typ) x H(Max)
SOP28	18.50mm x 9.90mm x 2.41mm



Typical Application Circuit

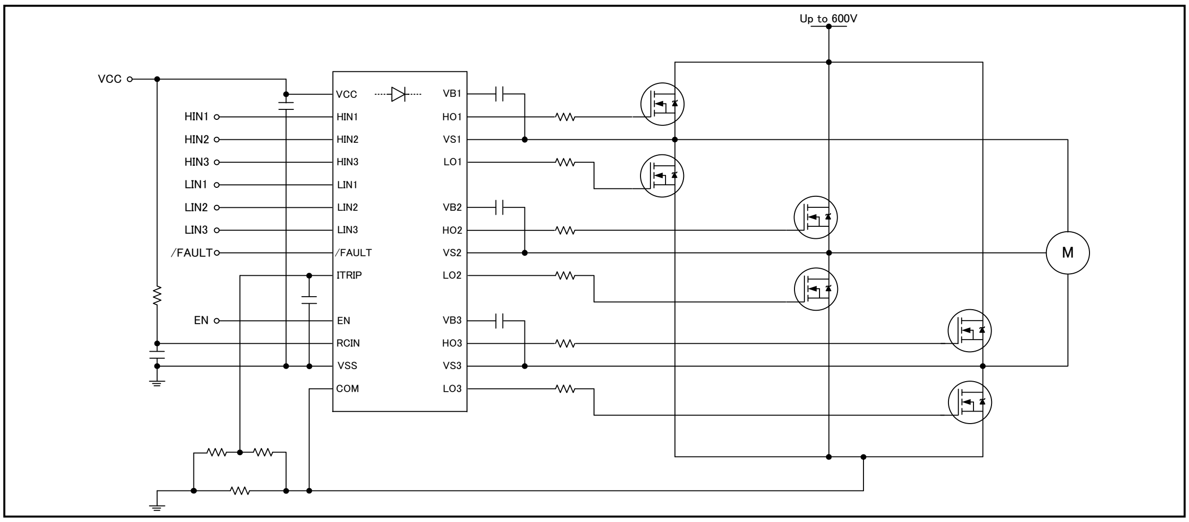


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

(TOP VIEW)

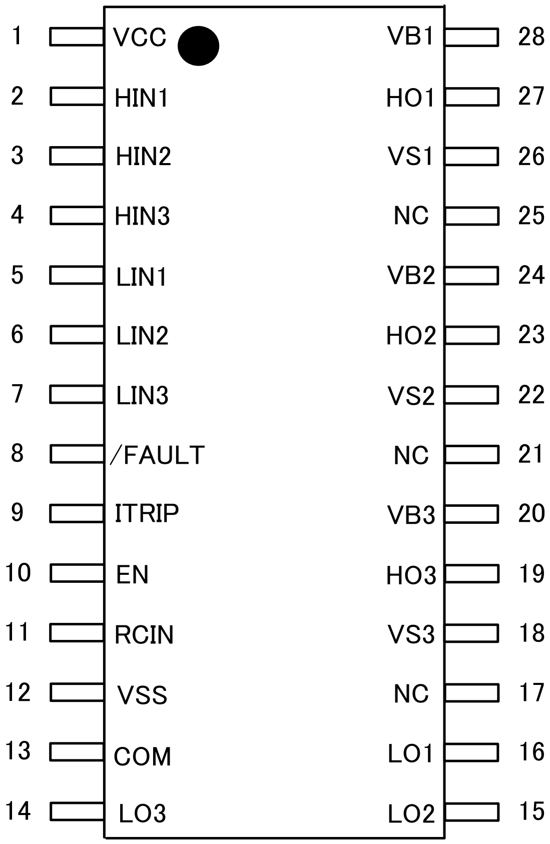


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	VCC	Low-side supply voltage
2	HIN1	Logic input for high-side gate driver output (HO1), in phase
3	HIN2	Logic input for high-side gate driver output (HO2), in phase
4	HIN3	Logic input for high-side gate driver output (HO3), in phase
5	LIN1	Logic input for low-side gate driver output (LO1), in phase
6	LIN2	Logic input for low-side gate driver output (LO2), in phase
7	LIN3	Logic input for low-side gate driver output (LO3), in phase
8	/FAULT	OCP or low-side UVLO(VCC-COM) detect signal output (negative logic, open-drain output)
9	ITRIP	Analog input for over current shutdown, activates /FAULT and RCIN to VSS
10	EN	Logic input to enable I/O functionality (positive logic)
11	RCIN	External RC-network to define /FAULT clear delay after the /FAULT signal
12	VSS	Logic ground
13	COM	Power ground
14	LO3	Low-side gate drive output
15	LO2	Low-side gate drive output
16	LO1	Low-side gate drive output
17	NC	Non-Connection
18	VS3	High-side negative power supply
19	HO3	High-side gate drive output
20	VB3	High-side positive power supply
21	NC	Non-Connection
22	VS2	High-side negative power supply
23	HO2	High-side gate drive output
24	VB2	High-side positive power supply
25	NC	Non-Connection
26	VS1	High-side negative power supply
27	HO1	High-side gate drive output
28	VB1	High-side positive power supply

Block Diagram

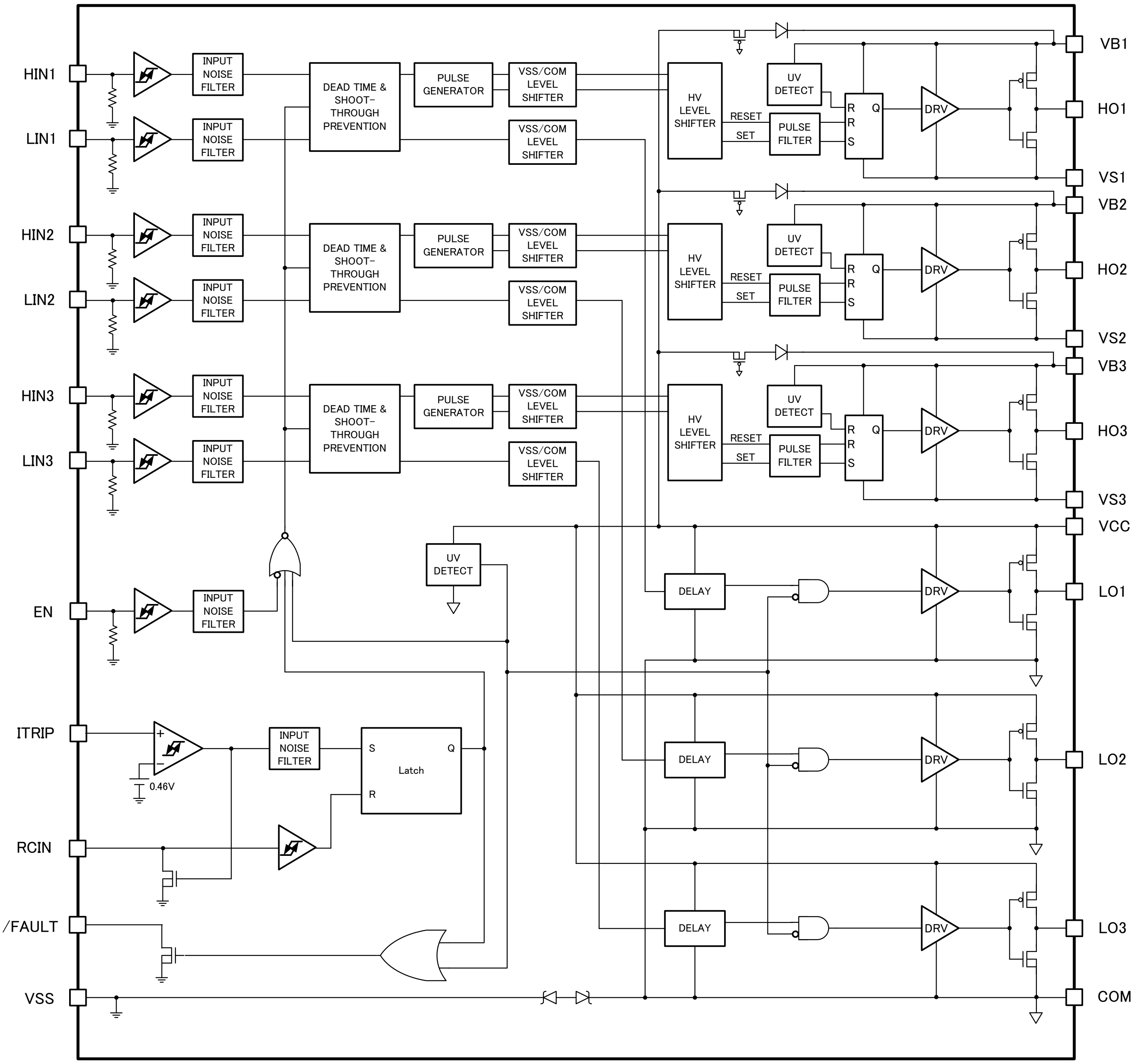


Figure 3. Functional Block Diagram

Absolute Maximum Ratings

(Unless otherwise specified Ta=25°C, All voltages are absolute voltages referenced to VSS. V_{SS}=0V)

Parameter	Symbol	Rating	Unit
High-side Offset Voltage	V_S	V_B - 25 to V_B + 0.3	V
High-side Floating Supply Voltage	V_B	V_{COM} - 0.3 to V_{COM} + 625	V
High-side Floating Output Voltage HOx*(Note 1)*	V_{HO}	V_S - 0.3 to V_B + 0.3	V
Low-side and Logic Fixed Supply Voltage (VCC vs VSS)	V_{CC}	- 0.3 to + 25	V
Low-side and Logic Fixed Supply Voltage (VCC vs COM)	V_{CCCOM}	- 0.3 to + 25	V
Low-side Output Voltage LOx (LOx vs COM) *(Note 1)*	V_{LO}	- 0.3 to V_{CCCOM} + 0.3	V
Logic Input Voltage HINx, LINx*(Note 1)*, EN	V_{IN}	- 0.3 to V_{CC} + 0.3	V
/FAULT Output Voltage	V_{FLT}	- 0.3 to V_{CC} + 0.3	V
RCIN Input Voltage	V_{RCIN}	- 0.3 to V_{CC} + 0.3	V
ITRIP Input Voltage	V_{ITRIP}	- 0.3 to V_{CC} + 0.3	V
Power Ground	V_{COM}	- 5.5 to + 5.5	V
Allowable Offset Voltage Slew Rate	dV_S/dt	50	V/ns
Storage Temperature Range	Tstg	- 55 to + 150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 1) x=1, 2, 3.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
SOP28				
Junction to Ambient	θ_{JA}	136.9	88.6	°C/W
Junction to Top Characterization Parameter*(Note 3)*	Ψ_{JT}	19	15	°C/W

(Note 2) Based on JESD51-2A(Still-Air)

(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 4) Using a PCB board based on JESD51-3.

(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Ratings

(Unless otherwise specified All voltages are absolute voltages referenced to VSS. V_{SS}=0V)

Parameter	Symbol	Min	Typ	Max	Unit
High-side Floating Supply Offset Voltage (VSx vs COM) *(Note 6)*	V_S	-	-	600	V
High-side Floating Supply Voltage (VBx vs VSx) *(Note 6)*	V_{BS}	11.5	15	20	V
High-side Floating Output Voltage (HOx vs VSx) *(Note 6)*	V_{HO}	0	15	V_{BS}	V
Low-side Supply Voltage (VCC vs VSS)	V_{CC}	11.5	15	20	V
Low-side Supply Voltage (VCC vs COM)	V_{CCCOM}	11.5	15	20	V
Low-side Output Voltage LOx (LOx vs COM) *(Note 6)*	V_{LO}	0	-	V_{CCCOM}	V
Logic Input Voltage HINx, LINx*(Note 6)*, EN	V_{IN}	0	-	V_{CC}	V
/FAULT Output Voltage	V_{FLT}	0	-	V_{CC}	V
RCIN Input Voltage	V_{RCIN}	0	-	V_{CC}	V
ITRIP Input Voltage	V_{ITRIP}	0	-	V_{CC}	V
Power Ground	V_{COM}	-2.5	-	+2.5	V
Operating Temperature	Topr	-40	-	+125	°C

(Note 6) x=1, 2, 3.

Static Logic Function Table

VCC	**VB-VS**	**RCIN**	**ITRIP**	**EN**	**/FAULT**	**HO1, HO2, HO3**	**LO1, LO2, LO3**
$<V_{CCUV-}$	X*(Note 7)*	X*(Note 7)*	X*(Note 7)*	X*(Note 7)*	0V	0V	0V
15V	$<V_{BSUV-}$	X*(Note 7)*	0V	5V	High-Z	0V	LIN1, LIN2, LIN3
15V	15V	X*(Note 7)*	$>V_{IT\_TH+}$	5V	0V	0V	0V
15V	15V	$<V_{RCIN+}$	0V	5V	0V*(Note 8)*	0V*(Note 8)*	0V*(Note 8)*
15V	15V	$>V_{RCIN+}$	0V	5V	High-Z	HIN1, HIN2, HIN3	LIN1, LIN2, LIN3
15V	15V	$>V_{RCIN+}$	0V	0V	High-Z	0V	0V

(Note 7) X is not depend on the value.
(Note 8) State after the OCP. Because the latch circuit is not reset, the OCP state is maintained.

DC Operation Electrical Characteristics

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
V_{CC} and V_{BS} Supply Undervoltage Positive Going Threshold	V_{CCUV+} V_{BSUV+}	9.6	10.4	11.2	V	
V_{CC} and V_{BS} Supply Undervoltage Negative Going Threshold	V_{CCUV-} V_{BSUV-}	8.6	9.4	10.2		
V_{CC} Supply Undervoltage Lockout Hysteresis	V_{CCUVH} V_{BSUVH}	-	1.0	-		
Offset Supply Leakage Current	I_{LK}	-	-	50	µA	V_B = V_S = 600V
Quiescent V_{BS} Supply Current	I_{QBS}	-	60	120		V_{IN} = 0V or 5V
Quiescent V_{CC} Supply Current	I_{QCC}	-	0.7	1.3	mA	V_{IN} = 0V or 5V
Logic “1” Input Voltage	V_{IH}	2.6	-	-	V	
Logic “0” Input Voltage	V_{IL}	-	-	0.8		
EN Positive Going Threshold	V_{EN+}	-	-	2.6		
EN Negative Going Threshold	V_{EN-}	0.8	-	-		
RCIN Positive Going Threshold	V_{RCIN+}	-	8	-	V	
RCIN Hysteresis	V_{RCIN_HYS}	-	3	-		
ITRIP Positive Going Threshold	V_{IT_TH+}	0.437	0.46	0.483	V	
ITRIP Hysteresis	V_{IT_HYS}	-	0.07	-		
High Level Output Voltage, V_{CC} (V_{BS}) - V_{LO} (V_{HO})	V_{OH}	-	-	1.4	V	I_O = 20mA
Low Level Output Voltage, V_{LO} (V_{HO})	V_{OL}	-	-	0.6		
Logic “1” Input Bias Current	I_{IN+}	-	100	150	µA	V_{IN} = 3.3V
Logic “0” Input Bias Current	I_{IN-}	-	-	1.0		V_{IN} = 0V
ITRIP Input Bias Current	I_{ITRIP}	-	1	2		V_{ITRIP} = 0V or 3.3V
Output High Short Circuit Pulsed Current	I_{O+}	120	200	-	mA	V_O = 0V Pulse Width ≤ 10µs
Output Low Short Circuit Pulsed Current	I_{O-}	250	350	-		V_O = 15V Pulse Width ≤ 10µs
RCIN Input Bias Current	I_{RCIN}	-	-	1	µA	
RCIN Low ON Resistance	R_{ON_RCIN}	-	50	100	Ω	V_{RCIN} = 0.5V
/FAULT Low ON Resistance	R_{ON_FLT}	-	50	100		V_{FLT} = 0.5V
Bootstrap Diode Resistance	R_{BOOT}	16	28	40		I_{F1} = 10mA, I_{F2} = 20mA
Bootstrap Diode Forward Voltage	V_{FBOOT}	0.4	0.7	1.0	V	I_F = 0.5mA, V_{FBOOT} = VCC - VB
Bootstrap Diode Leakage Current	I_{LKBOOT}	-	-	50	µA	V_B = V_S = 600V, V_{CC} = V_{SS}

AC Operation Electrical Characteristics

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Turn-on Propagation Delay	t_{ON}	480	630	780	ns	V_S = 0V, V_{IN} = 0V to 5V
Turn-off Propagation Delay	t_{OFF}	430	580	730		V_S = 0V or 600V, V_{IN} = 5V to 0V
Turn-on Rise Time	t_R	-	125	190		V_{IN} = 0V to 5V
Turn-off Fall Time	t_F	-	50	75		V_{IN} = 5V to 0V
EN Low to Output Shutdown Propagation Delay	t_{EN}	430	580	730		V_{IN} = 5V, V_{EN} = 5V to 0V
ITRIP to Output Shutdown Propagation Delay	t_{ITRIP}	500	750	1000		V_{ITRIP} = 5V
ITRIP Blanking Time	t_{BL}	100	150	-		V_{ITRIP} = 5V
ITRIP to /FAULT Propagation Delay	t_{FLT}	400	600	800		V_{ITRIP} = 5V
Input Filter Time (HINx, LINx)*(Note 9)*	t_{FILIN}	100	200	-		V_{IN} = 0V to 5V, 5V to 0V
Enable Input Filter Time	t_{FLTEN}	100	200	-		V_{EN} = 0V to 5V, 5V to 0V
Dead Time	t_{DT}	200	300	450		V_{IN} = 0V to 5V, 5V to 0V
Delay Matching, High-side & Low-side Turn-on/off	t_{MT}	-	-	150		
/FAULT Clear Time	t_{FLTCLR}	1.3	1.65	2.0	ms	RCIN : R = 2MΩ, C = 1nF

(Note 9) x=1, 2, 3.

Typical Performance Curves

(Unless otherwise specified Ta=25°C, $V_{CC}=V_{BS}=15V$, $V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}$, $C_L=1000pF$)

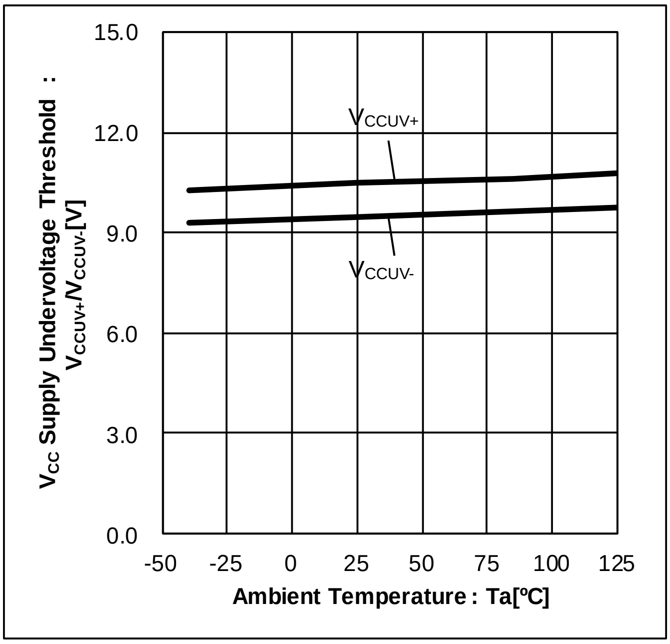


Figure 4. V_{CC} Supply Undervoltage Threshold vs Ambient Temperature

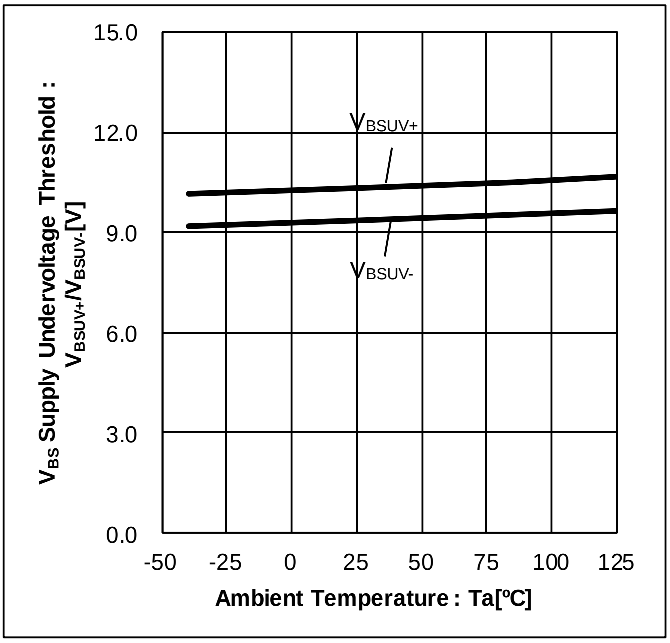


Figure 5. V_{BS} Supply Undervoltage Threshold vs Ambient Temperature

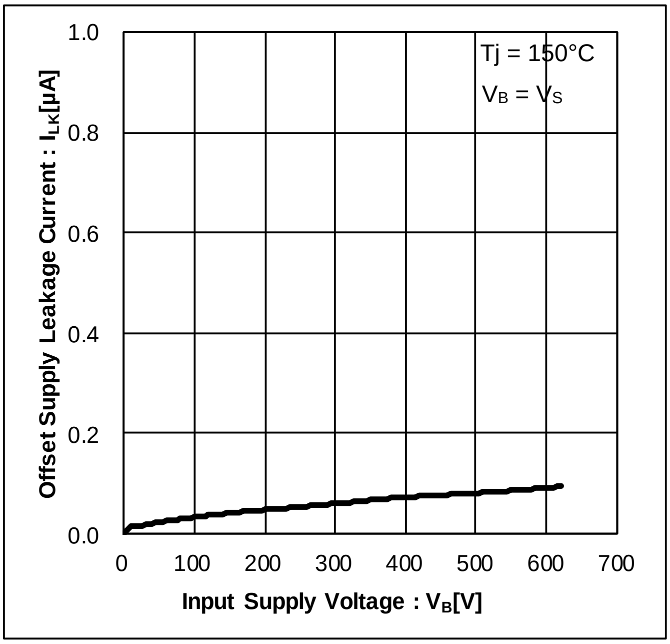


Figure 6. Offset Supply Leakage Current vs Input Supply Voltage V_B

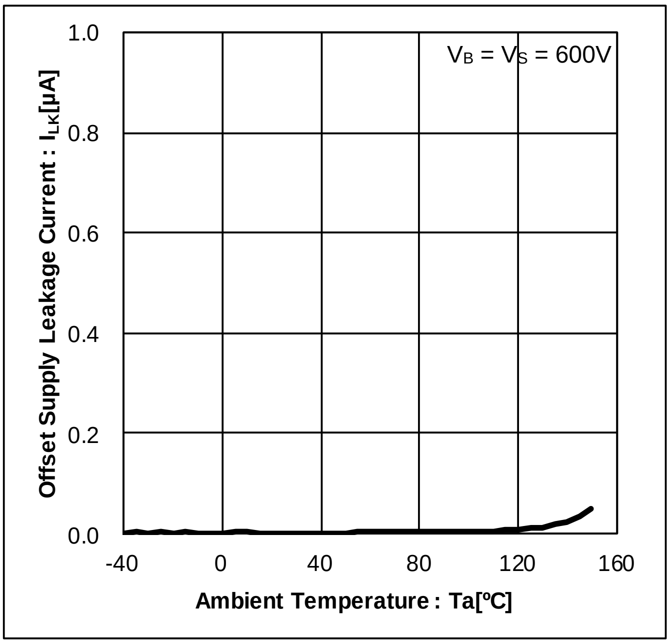


Figure 7. Offset Supply Leakage Current vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

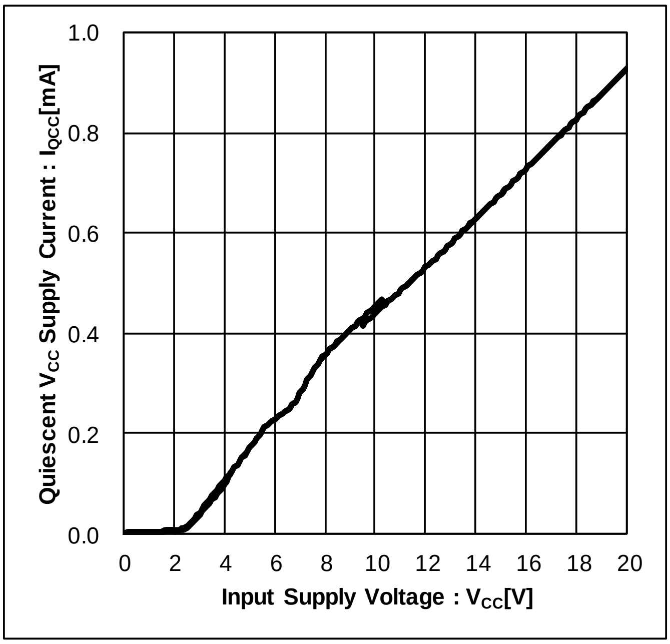


Figure 8. Quiescent V_{CC} Supply Current vs Input Supply Voltage V_{CC}

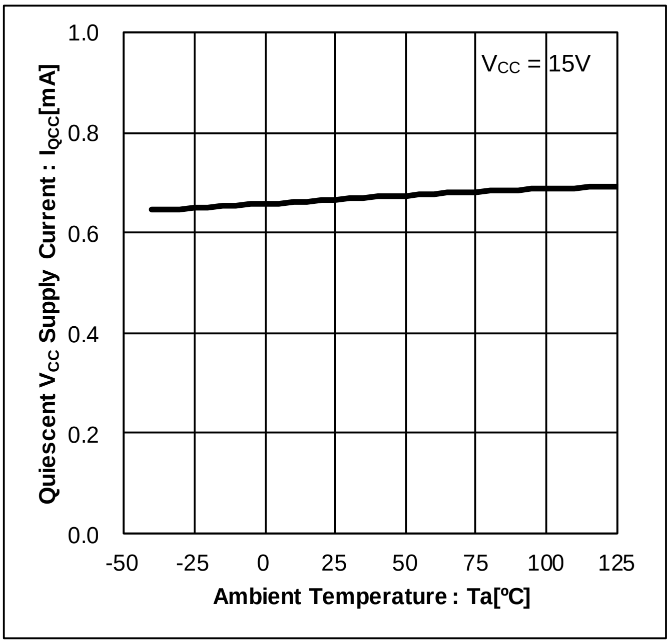


Figure 9. Quiescent V_{CC} Supply Current vs Ambient Temperature

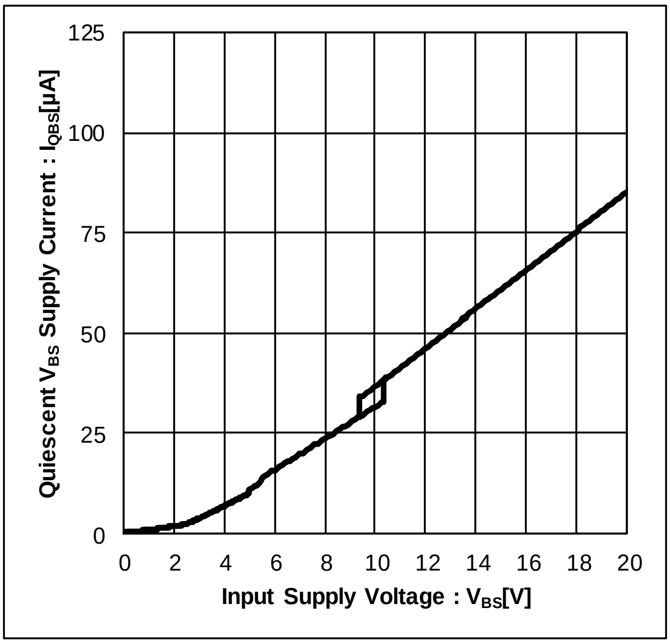


Figure 10. Quiescent V_{BS} Supply Current vs Input Supply Voltage V_{BS}

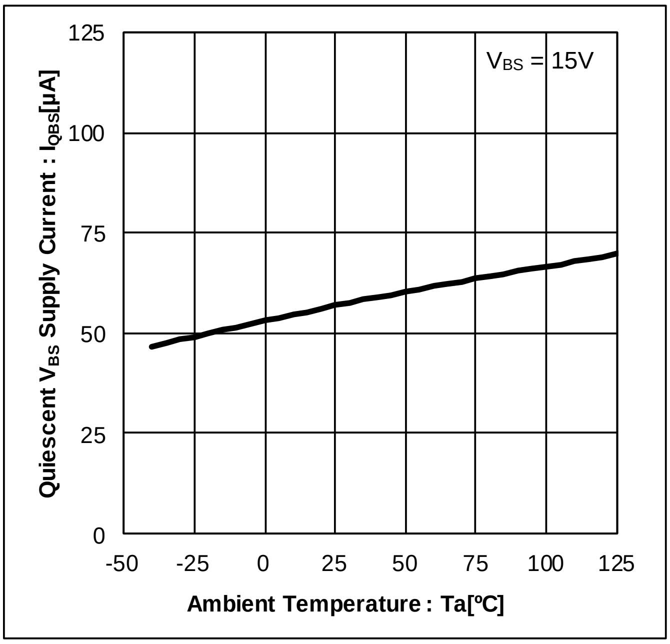


Figure 11. Quiescent V_{BS} Supply Current vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, $V_{CC}=V_{BS}=15V$, $V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}$, $C_L=1000pF$)

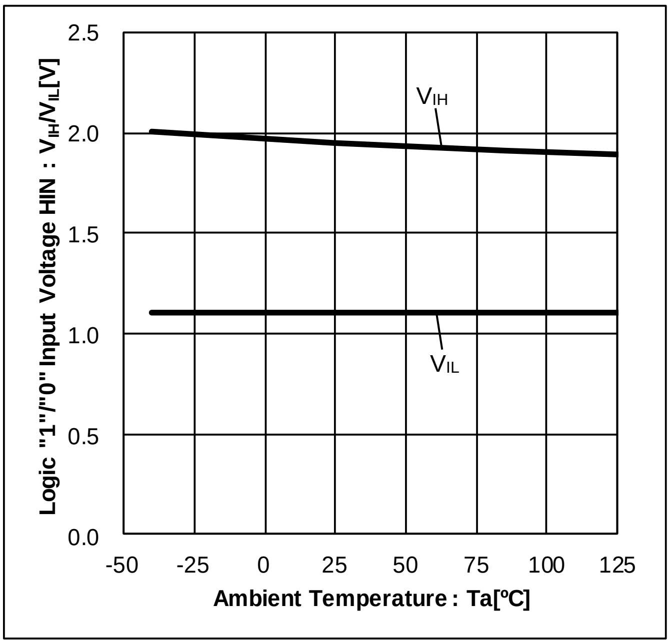


Figure 12. Logic “1”/”0” Input Voltage HIN vs Ambient Temperature

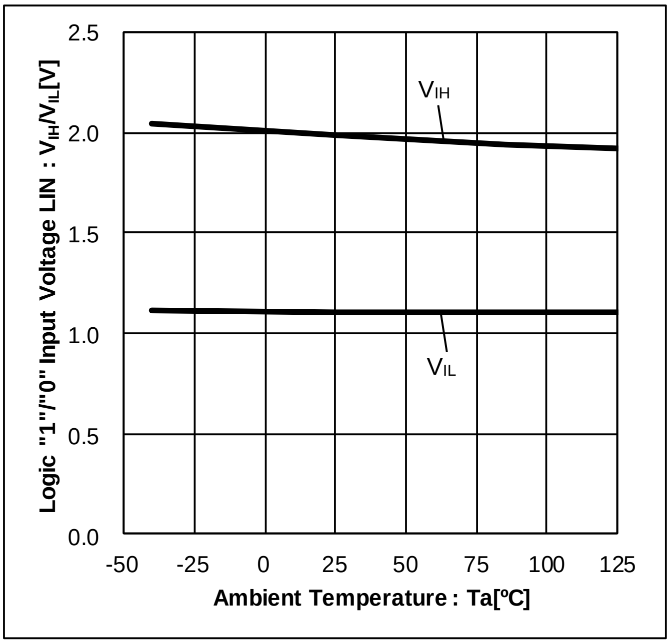


Figure 13. Logic “1”/”0” Input Voltage LIN vs Ambient Temperature

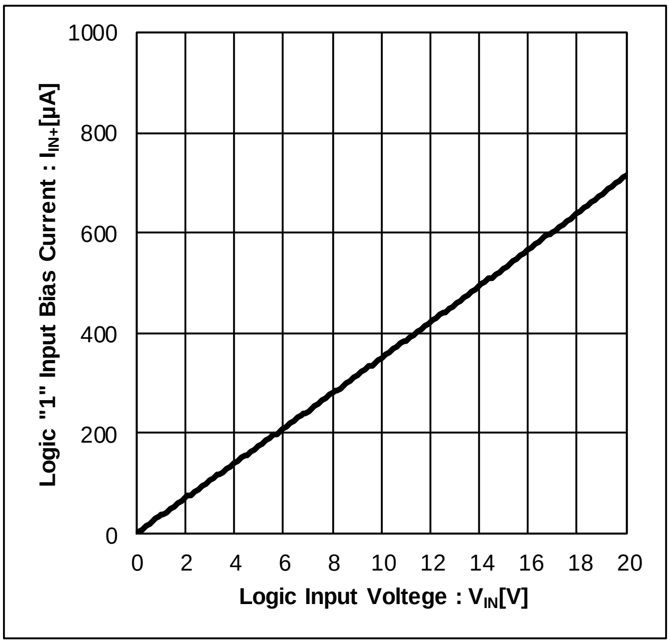


Figure 14. Logic “1” Input Bias Current vs Logic Input Voltage V_{IN}

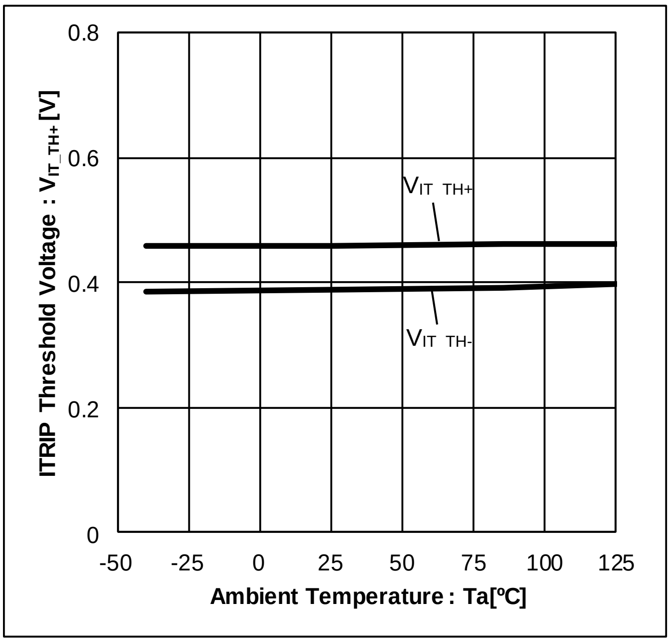


Figure 15. ITRIP Threshold Voltage vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

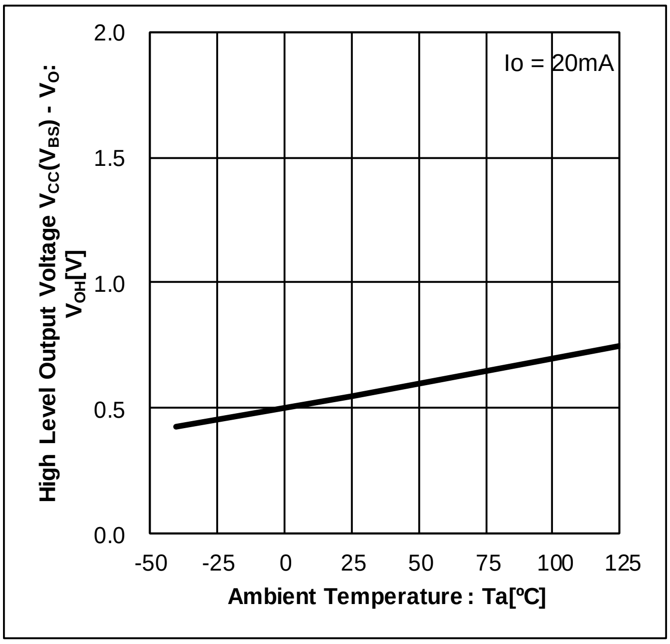


Figure 16. High Level Output Voltage vs Ambient Temperature

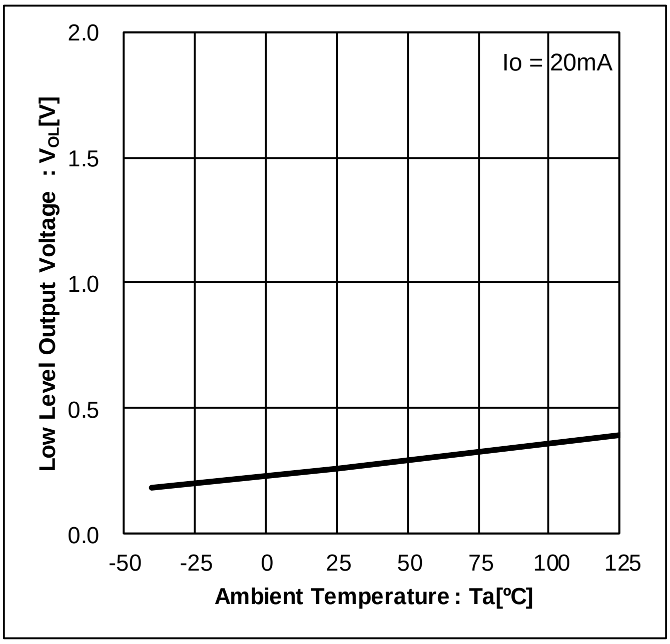


Figure 17. Low Level Output Voltage vs Ambient Temperature

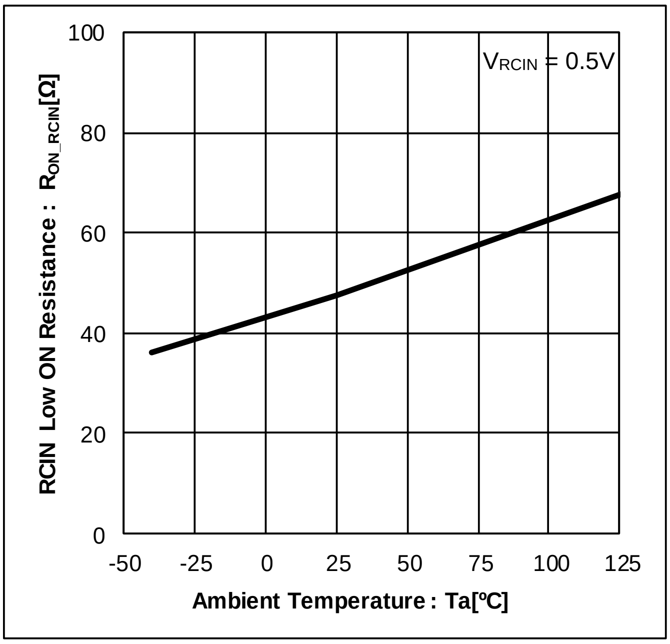


Figure 18. RCIN Low ON Resistance vs Ambient Temperature

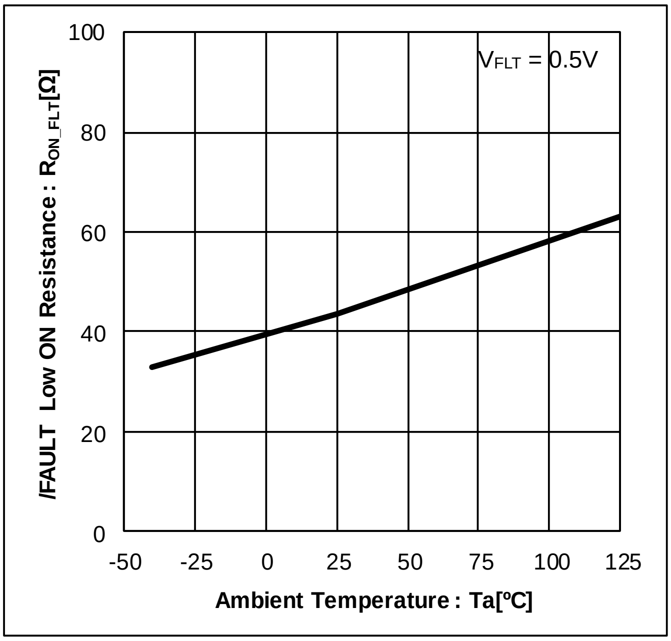


Figure 19. /FAULT Low ON Resistance vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, $V_{CC}=V_{BS}$=15V, $V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}$, C_L=1000pF)

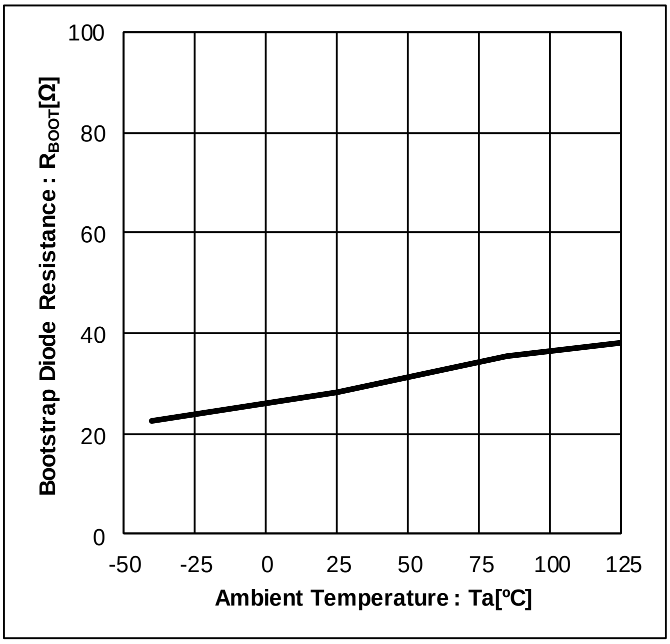


Figure 20. Bootstrap Diode Resistance vs Ambient Temperature

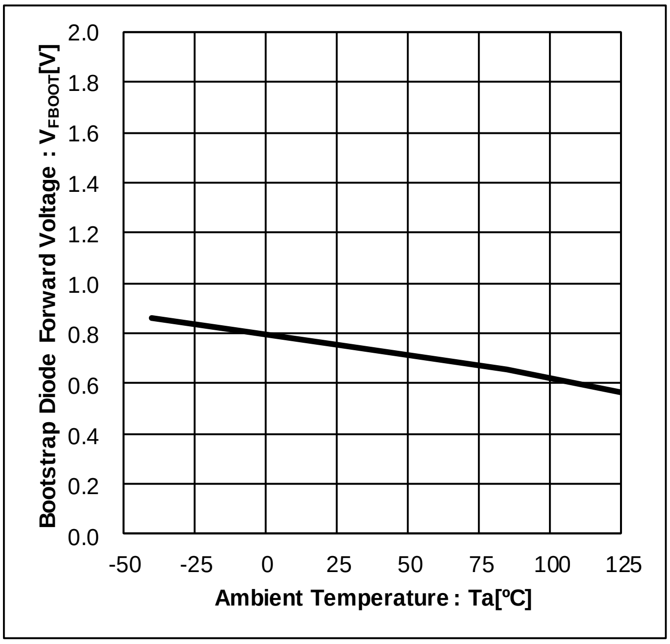


Figure 21. Bootstrap Diode Forward voltage vs Ambient Temperature

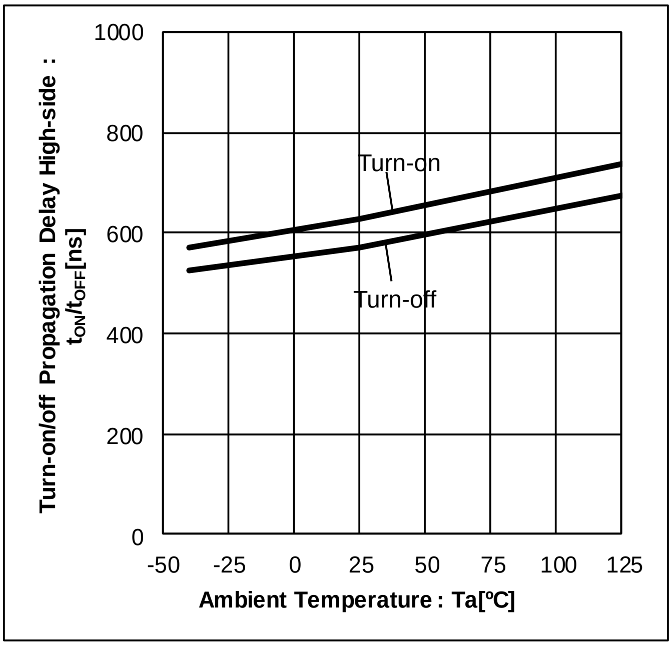


Figure 22. Turn-on/off Propagation Delay High-side vs Ambient Temperature

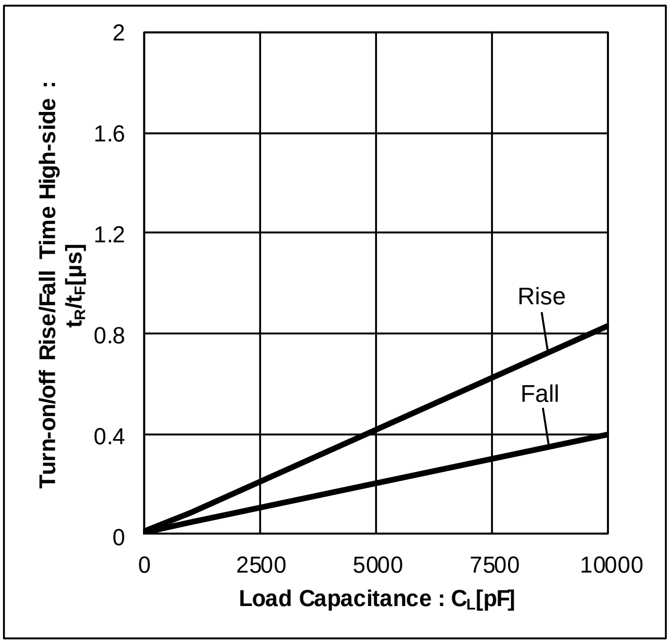


Figure 23. Turn-on/off Rise/Fall Time High-side vs Load Capacitance

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

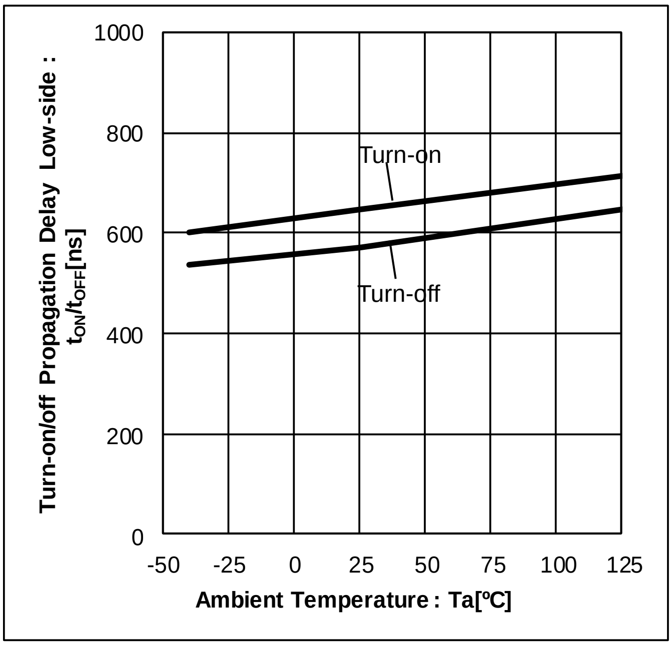


Figure 24. Turn-on/off Propagation Delay Low-side vs Ambient Temperature

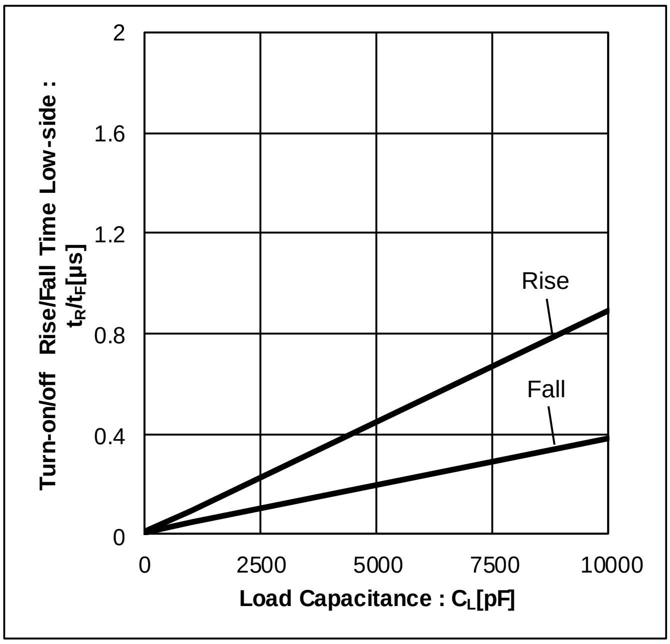


Figure 25. Turn-on/off Rise/Fall Time Low-side vs Load Capacitance

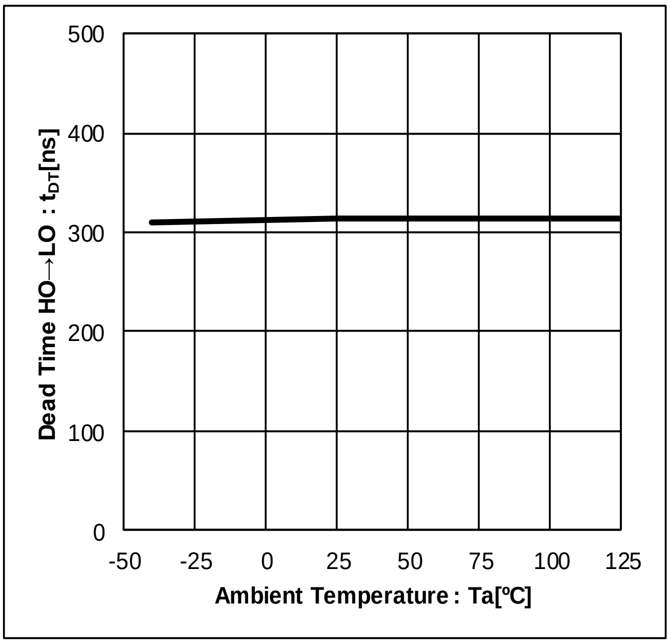


Figure 26. Dead Time HO→LO vs Ambient Temperature

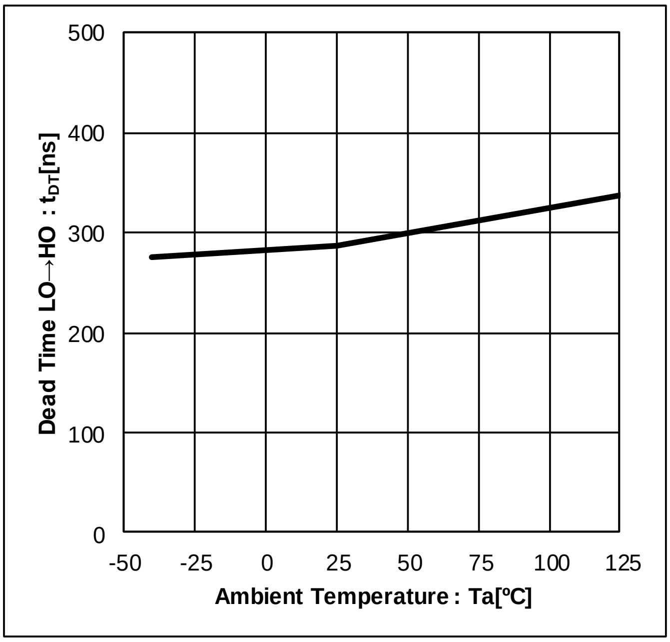


Figure 27. Dead Time LO→HO vs Ambient Temperature

Typical Performance Curves – continued

(Unless otherwise specified Ta=25°C, V_{CC}=V_{BS}=15V, V_{SS}=V_{COM}=V_{S1}=V_{S2}=V_{S3}, C_L=1000pF)

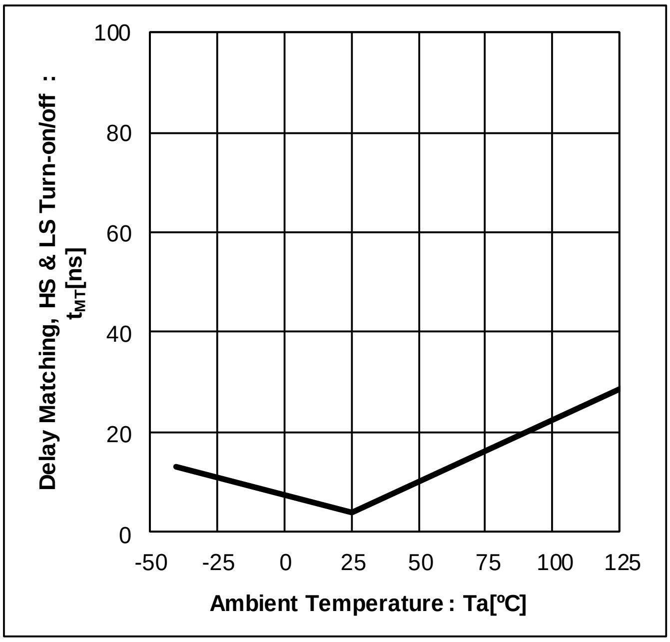


Figure 28. Delay Matching, HS & LS Turn-on/off vs Ambient Temperature

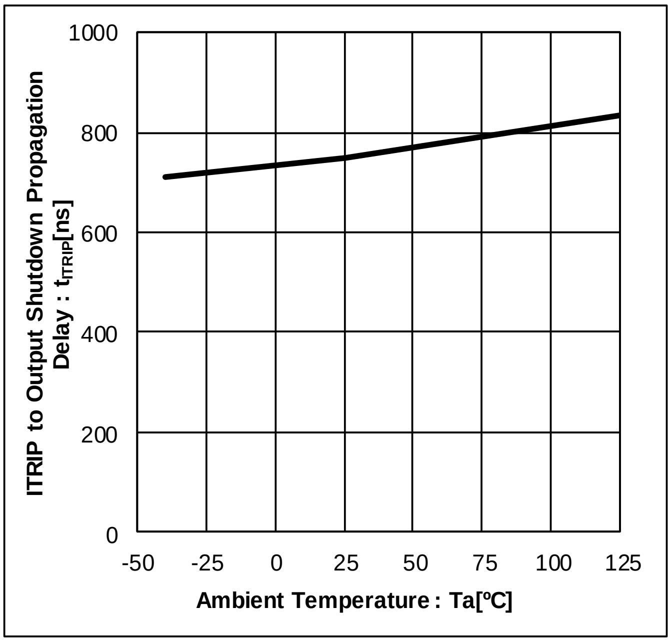


Figure 29. ITRIP to Output Shutdown Propagation Delay vs Ambient Temperature

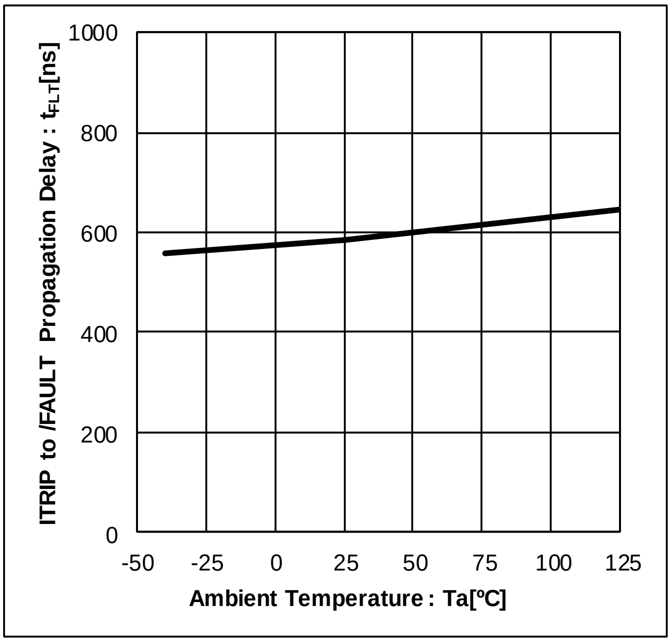


Figure 30. ITRIP to /FAULT Propagation Delay vs Ambient Temperature

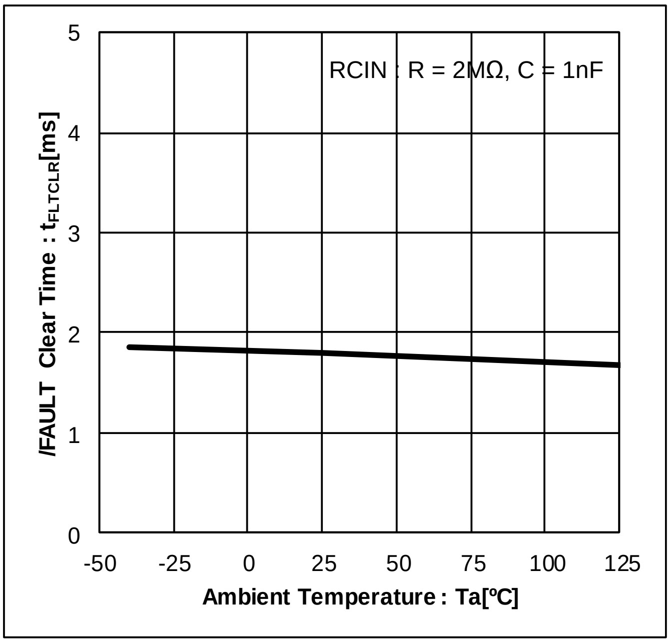
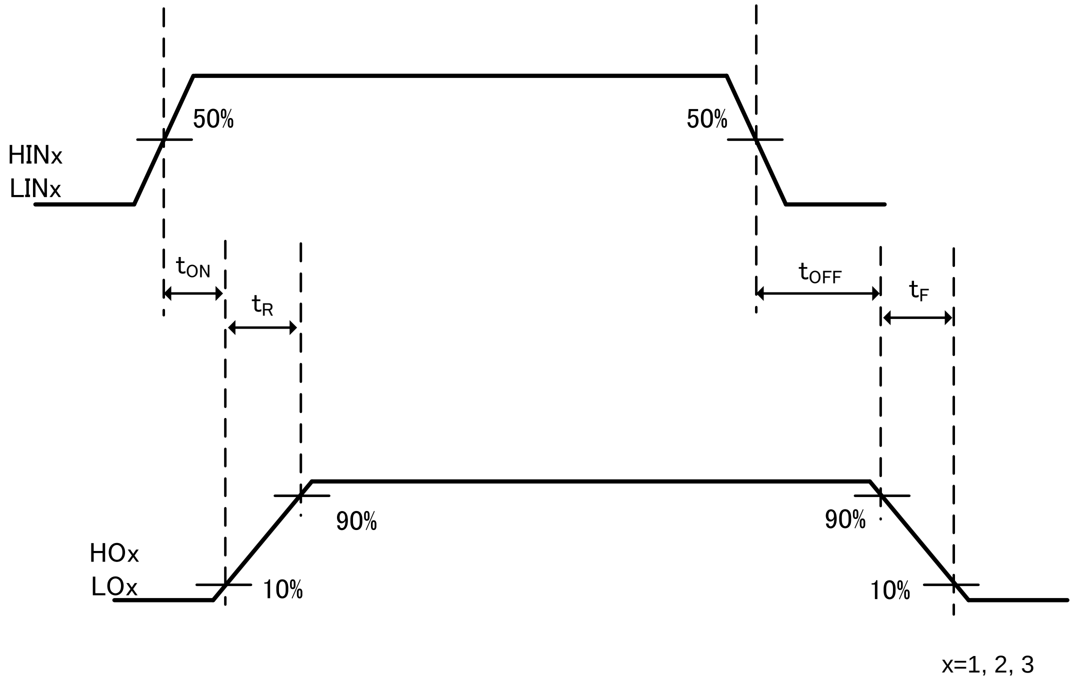
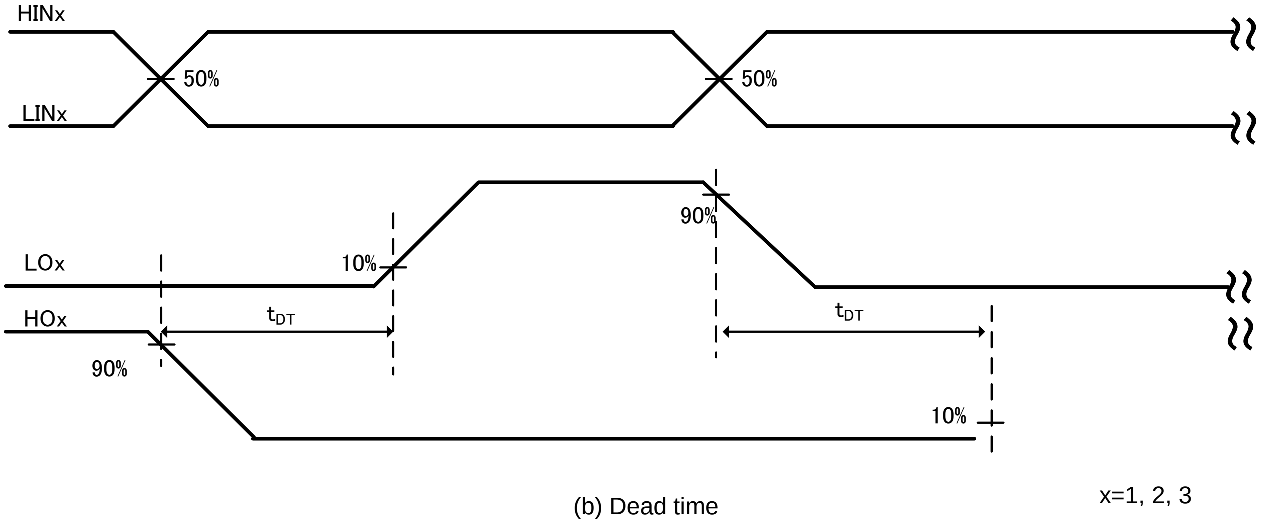


Figure 31. /FAULT Clear Time vs Ambient Temperature

Timing Chart



(a) Propagation Delay



(b) Dead time

Figure 32. Timing Chart

Timing Chart – continued

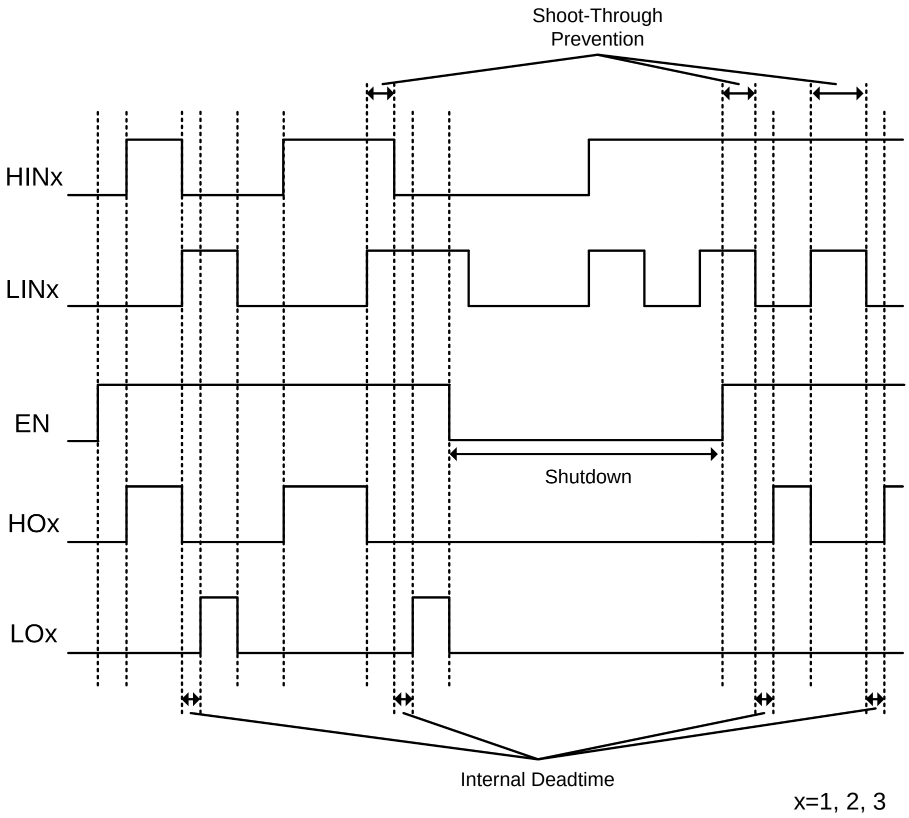


Figure 33. Input-Output Logic

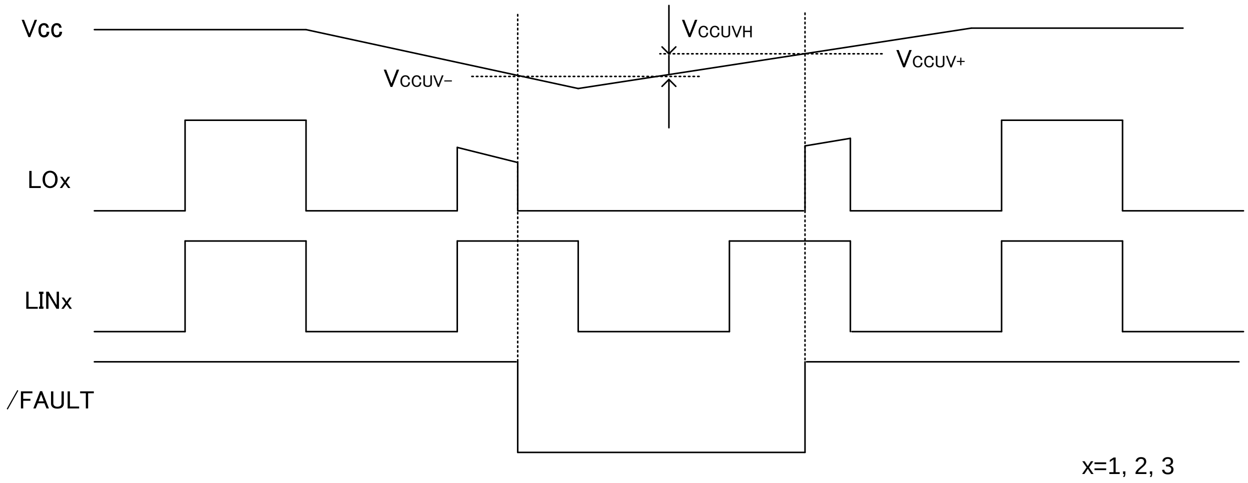


Figure 34. UVLO of VCC Timing Chart

Over Current Protection

As soon as the ITRIP voltage is exceeded the threshold voltage V_{IT_TH+}=0.46V (Typ), the RCIN pin changes from “H” to ”L” by discharge SW being turned on, and the /FAULT pin changes from “High-Z” to “L”.
ITRIP blanking time t_{BL}=150ns (Typ) prevents the driver to detect false over-current protection events which caused by noise. However, it is recommended to add a ceramic capacitor near the ITRIP pin.
The RCIN voltage increases by time constant of external resistance and capacitance. As soon as the RCIN voltage is exceeded V_{RCIN+}=8V (Typ), the /FAULT pin changes from “L” to “High-Z”.
Also, the RCIN voltage operates in the voltage V_{RCIN+} or less. However, it is not returned with stopping when the ITRIP voltage goes over threshold voltage V_{IT_TH+} once. The RCIN voltage to recommend at the normal operation is V_{RCIN+} or more.

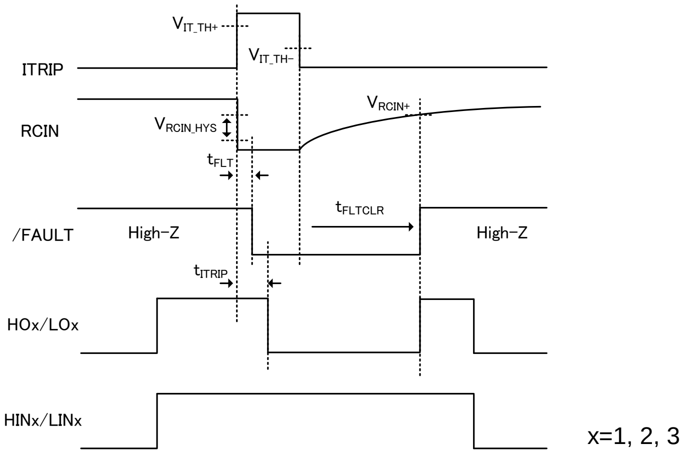


Figure 35. OCP Detection Timing Chart

The over current detection value is determined by R_1, R_2, and R_S, which are connected to the ITRIP pin as Figure 36.
It is determined by the following equation.

$$I_{OCP} = \frac{R_1 + R_2}{R_2} \times \frac{V_{IT\_TH+}}{R_S}$$

where:

I_{OCP} is over current detection value.

V_{IT_TH+} is OCP threshold voltage 0.46V(Typ).

R_S is shunt resistor.

It is determined the reset time when the /FAULT pin changes from “L” to “High-Z” after over current protection was removed by the following equation.

$$t_{FLTCLR} = -(R_{RCIN} \times C_{RCIN}) \times \ln\left(1 - \frac{V_{RCIN+}}{V_{CC}}\right)$$

where:

V_{RCIN+} is RCIN threshold voltage 8V(Typ).

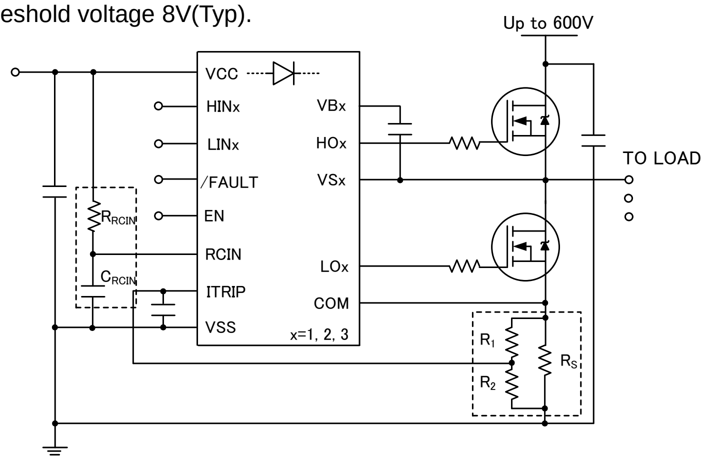


Figure 36. OCP Detection Schematic

Application Components Selection Method

(1) Gate Resistor

The gate resistor $R_{G(on/off)}$ is selected to the switching speed of the power device. The switching time (t_{SW}) is defined as the time spent to reach the end of the plateau voltage, so the turn-on gate resistor $R_{G(on)}$ can be calculated using the following formulas.

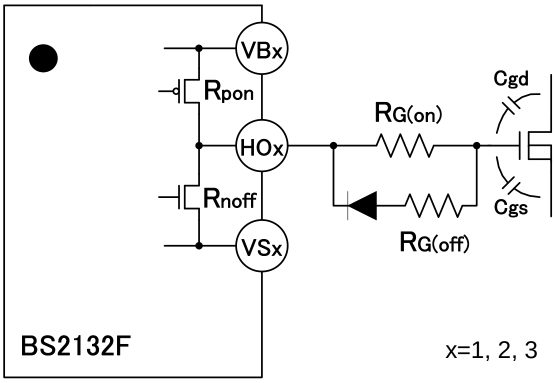


Figure 37. Gate Driver Equivalent Circuit

$$I_g = \frac{Q_{gs} + Q_{gd}}{t_{SW}} \tag{1}$$

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{I_g} \tag{2}$$

$$t_{sw} = \frac{Q_{gs} + Q_{gd}}{I_g} = \frac{(Q_{gs} + Q_{gd})(R_{pon} + R_{G(on)})}{(V_{BS} - V_{gs(th)})} \tag{3}$$

Where:

I_g is the gate current of the power device.

Q_{gs} is the charge between gate and source of the power device.

Q_{gd} is the charge between gate and drain of the power device.

$V_{gs(th)}$ is the threshold voltage of the power device.

The turn-on gate resistance can be changed to control output slew rate (dVs/dt). The slew rate of the power device is determined by the following equation.

$$\frac{dVs}{dt} = \frac{I_g}{C_{rss}} \tag{4}$$

where:

C_{rss} is the feedback capacitance.

The gate resistance is determined as follows by substituting equation (4) into equation (2).

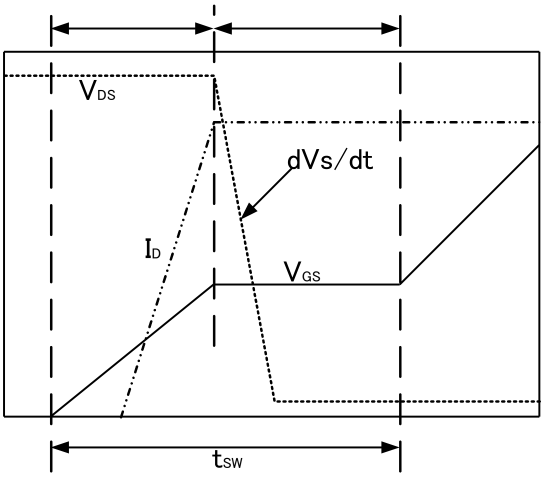


Figure 38. Gate Charge Transfer Characteristics

$$R_{TOTAL(on)} = R_{pon} + R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{C_{rss} \cdot \frac{dVs}{dt}} \tag{5}$$

$$R_{G(on)} = \frac{V_{BS} - V_{gs(th)}}{C_{rss} \cdot \frac{dVs}{dt}} - R_{pon} \tag{6}$$

When other power devices are turned on, current flows in the power device which is off through C_{gd}. At this point, the gate resistance ($R_{G(off)}$) should be set so that the gate voltage does not exceed the threshold of the power device and turn on the power device itself.

$$V_{gs(th)} \geq (R_{noff} + R_{G(off)}) \cdot I_g = (R_{noff} + R_{G(off)}) \cdot C_{gd} \frac{dVs}{dt} \tag{7}$$

$$R_{G(off)} \leq \frac{V_{gs(th)}}{C_{gd} \frac{dVs}{dt}} - R_{noff} \tag{8}$$

Application Components Selection Method – continued

(2) Bootstrap Capacitor C_{BS}

To reduce ripple voltage, ceramic capacitors with low ESR value are recommended for use in the bootstrap circuit. The bootstrap capacitor is determined by the voltage drop level and the total amount of the charge supplied. The maximum voltage drop to be able to turn on the power device of the high-side is determined by following formula.

$$\Delta V_{BS} \leq V_{CC} - VF - V_{GSMIN} - V_{OL} - V_{RS} \tag{9}$$

where:

V_{CC} is the gate driver supply voltage.

VF is the bootstrap diode forward voltage drop.

V_{GSMIN} is the minimum gate-source voltage which can turn on the power device.

V_{OL} is the ON voltage of the low-side power device.

V_{RS} is the voltage of the OCP resistance.

The total amount of the charge (Q_{Total}) supplied by the bootstrap capacitor is calculated by the following formula.

$$Q_{Total} = Q_G + (I_{LKGS} + I_{LK} + I_{LKDIO} + I_{QBS}) \cdot t_{HON} \tag{10}$$

where:

Q_G is the total gate charge.

I_{LKGS} is the switch gate-source leakage current.

I_{LKDIO} is the bootstrap diode leakage current.

I_{LK} is the level shifter circuit leakage current.

I_{QBS} is the VB-VS supply current.

t_{HON} is the high-side switch on time.

The bootstrap capacitance should satisfy the following formula.

$$C_{BS} \geq \frac{Q_{Total}}{\Delta V_{BS}} \tag{11}$$

However, VB-VS voltage is the voltage that VF of internal bootstrap diode was dropped. BS2132F has UVLO function between VB and VS. The value of VCC and C_{BS} should be set so that UVLO does not detect and ΔV_{BS} has margin enough. It is recommended to insert a 1 µF ceramic capacitor near VB-VS as a measure against noise.

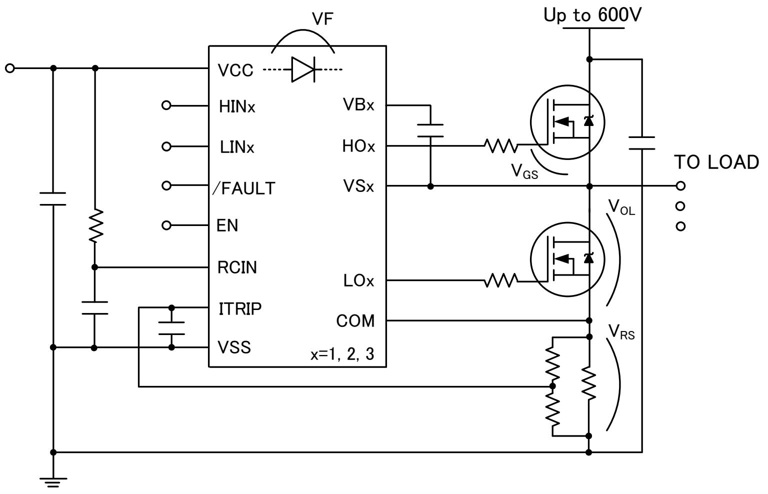


Figure 39. Bootstrap Power Supply Circuit

(2) Bootstrap Capacitor C_{BS} - continued

In addition, average current to charge from VCC to C_{BS} in operation is calculated by the following formula, and V_{BOOT} between VCC-VB voltage is Figure 40.

$$\begin{aligned} I_{CHARGE} &= I_{GC} + I_{LV} \\ &= C_{ISS} \cdot V_{BS0} \cdot f_{OSC} + 2.5 \times 10^{-9} \times f_{OSC} \end{aligned} \qquad (12)$$

where:

I_{GC} is average gate charge current of power device.

I_{LV} is average supply current of level shifter circuit.

V_{BS0} is V_S=0, and voltage between VB-VS of static state ($V_{BS0} = V_{CC} - VF$).

C_{ISS} is input capacitance of power device.

f_{OSC} is operation frequency of high-side.

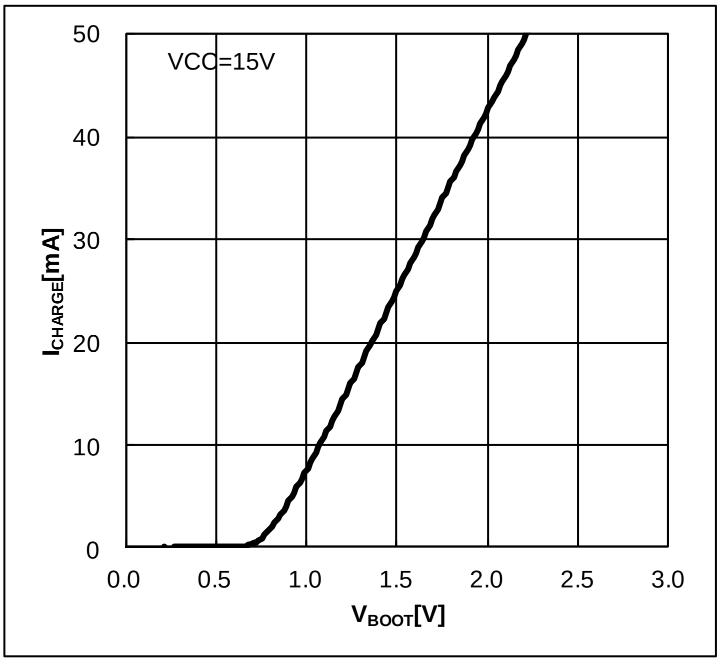


Figure 40. I_{CHARGE} vs V_{BOOT} (VCC-VB voltage)

It is necessary to satisfy following formula not to operate UVLO between VB-VS.

$$V_{CC} - V_{BOOT} - \frac{1}{2}\Delta V_{BS} \geq V_{BSMIN} \qquad (13)$$

where:

V_{BSMIN} is minimum operating voltage between VB-VS.

When equation (13) is not satisfied, it may not operate normally by UVLO detection. In the case, measures such as adding a bootstrap diode of low-VF are required. It is recommended to evaluate enough.

(3) Input Capacitor
A low-ESR ceramic capacitor should be used near the VCC pin to reduce input ripple voltage.
To supply charge to high-side and low-side, the capacitor of VCC is recommended to use a ceramic capacitor four times or more the minimum value of the bootstrap capacitor C_{BS} calculated by equation (11).

Application Components Selection Method – continued

(4) Input Signals Interval Δt_{IN}

The minimum interval of input signals ($\Delta t_{IN(Min)}$) to prevent the power device of high-side and low-side form shoot through can be calculated using the following formula.

$$t_{DEAD} \approx (t_{ON} + \Delta t_{IN}) - (t_{OFF} + t_F) \qquad (14)$$

$$t_F = -\tau \times (\ln 0.1 - \ln 0.9) \qquad (15)$$

$$\tau = (R_{NON} + R_G) \times C_L \qquad (16)$$

where:

t_{ON} is turn-on propagation delay.

t_{OFF} is turn-off propagation delay.

t_F is turn-off fall time.

R_{NON} is on-resistance of Nch-FET constituting the final stage inverter.

R_G is gate resistance.

C_L is load capacitance.

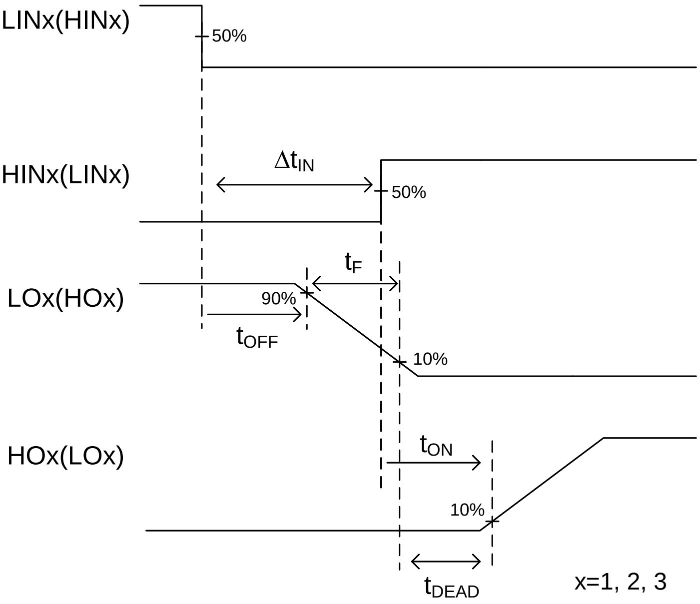


Figure 41. Shoot-Through Prevention Timing Chart

To prevent shoot through, it should be designed the timing to satisfy following formula.

$$t_{DEAD} > 0 \qquad (17)$$

$$(t_{ON} + \Delta t_{IN}) - (t_{OFF} + t_F) > 0 \qquad (18)$$

$$\Delta t_{IN} > (t_{OFF} - t_{ON}) + t_F \qquad (19)$$

$$\Delta t_{IN(Min)} > (t_{OFF(Max)} - t_{ON(Min)}) - (R_{NON(Max)} + R_G) \times C_L \times (\ln 0.1 - \ln 0.9) \qquad (20)$$

Overshoot / Undershoot of The Output Terminal at The Time of The Switching

The occurrence of overshoot / undershoot may be detected by the parasitic inductance of the PCB and the bonding wire in the IC. The mechanism of overshoot in the switching off is Figure 43.

(1) After Pch-FET is turn-off, current flows from HO to VB through capacitance between Gate-Source and Gate-Drain.
(2) The current flows from HO to VB through parasitic diode of Pch-FET by the parasitic inductance. Forward voltage VF of the parasitic diode is increased, and the HO voltage becomes VB+VF. Nch-FET is turn-on and it is discharged to VS.

The undershoot of the switching on may be caused by the same mechanism, too.
In addition, it may be caused in low-side output LO because the circuit structure is the same. The overshoot / undershoot voltage changes by the current of the parasitic diode.
When the overshoot / undershoot voltage is large, please adjust the gate resistance to slow the switching speed and connect to reduce the parasitic inductance.

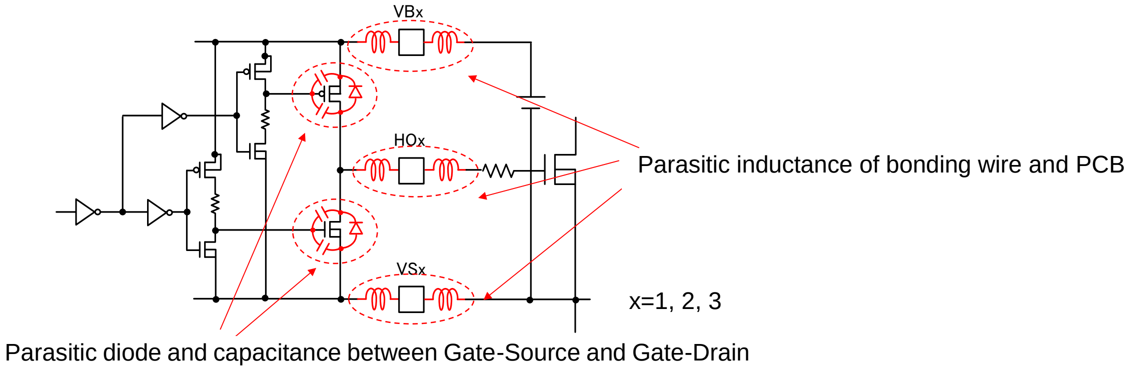


Figure 42. Schematic with Parasitic Inductance

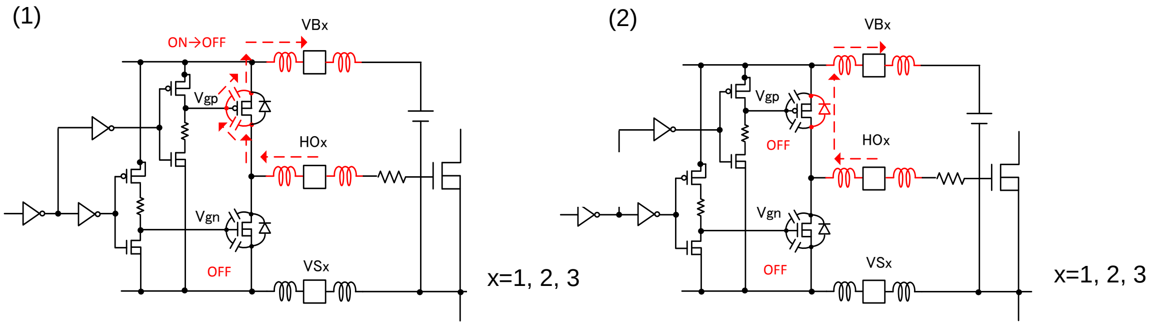


Figure 43. Mechanism of Overshoot

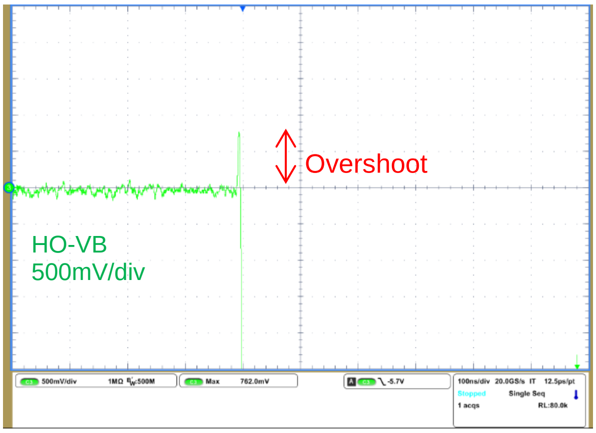


Figure 44. Overshoot Wave

PCB Layout

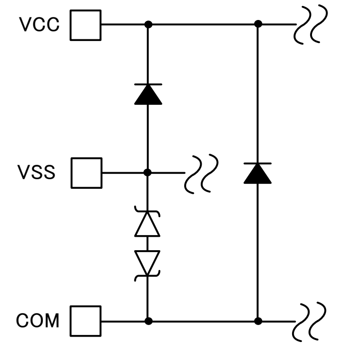
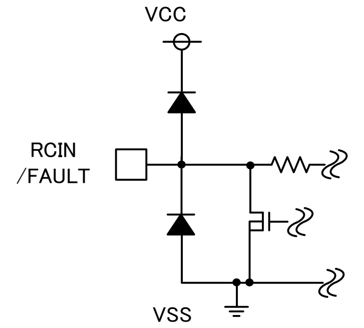
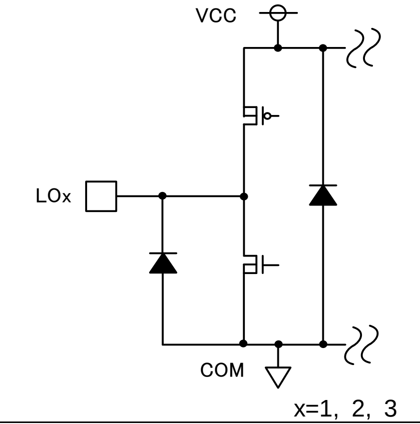
1. Power GND and Logic GND
   Surge voltage is caused by current of Power GND and parasitic inductance of the wire. Logic GND level fluctuates by surge propagating in Logic GND, and incorrect signal may be input to input terminal which is based on Logic GND. It is not recommended to connect Power GND and Logic GND by common all over pattern, and It is recommended to connect Power GND and Logic GND at only a point.

2. Shunt Resistor of OCP detection
   It is recommended to locate a shunt resistor near the external power device of low-side. If the wiring is long, surge voltage is caused by parasitic inductance and it may be incorrectly detected OCP. The wiring of COM devided from the shunt resistor should be divided near the shunt resistor.

3. ITRIP Filter Capacitor
   To prevent a malfunction, it is recommended to locate a ceramic capacitor for filter near the ITRIP pin. GND of the capacitor should be connected to Logic GND.

4. Input Capacitor and Zener Diode
   An input capacitor and a zener diode, a bootstrap capacitor should be located near the pin. It is recommended to select a low ESR capacitor such as a ceramic capacitor.

I/O Equivalence Circuits

Pin No.	Pin Name	Pin Equivalent Circuit
1 12 13	VCC VSS COM	
8 11	/FAULT RCIN	
14,15,16	LO1 LO2 LO3	

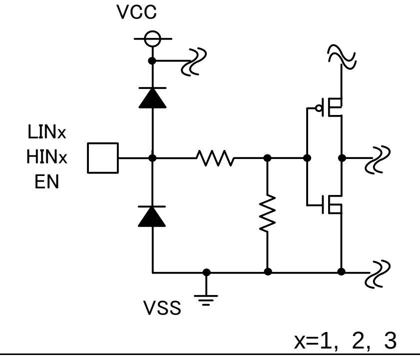
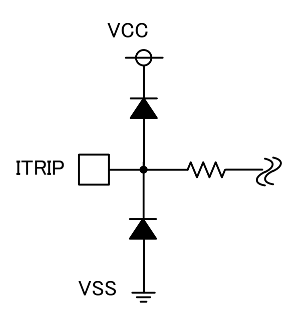
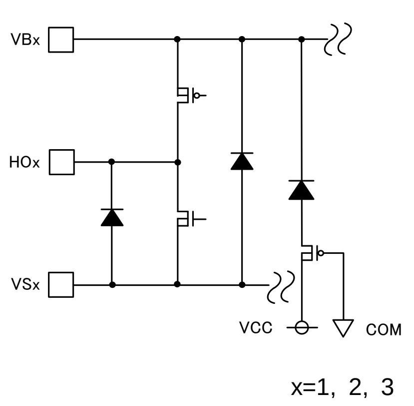
Pin No.	Pin Name	Pin Equivalent Circuit
2,3,4 5,6,7 10	HIN1 HIN2 HIN3 LIN1 LIN2 LIN3 EN	
9	ITRIP	
18,22,26 19,23,27 20,24,28	VS1 VS2 VS3 HO1 HO2 HO3 VB1 VB2 VB3	

Figure 45. I/O Equivalent Circuits

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. **Area of Safe Operation (ASO)**
    Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

Ordering Information

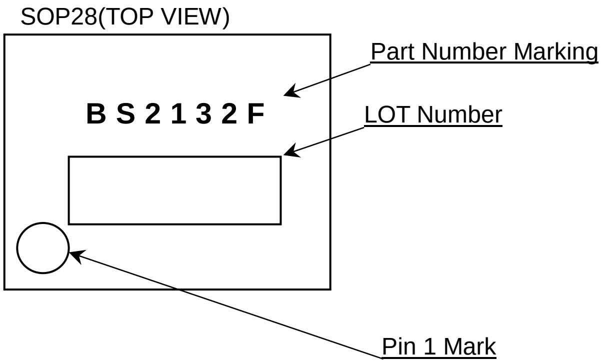
B S 2 1 3 2 F - E 2

Part Number

Package
F : SOP28

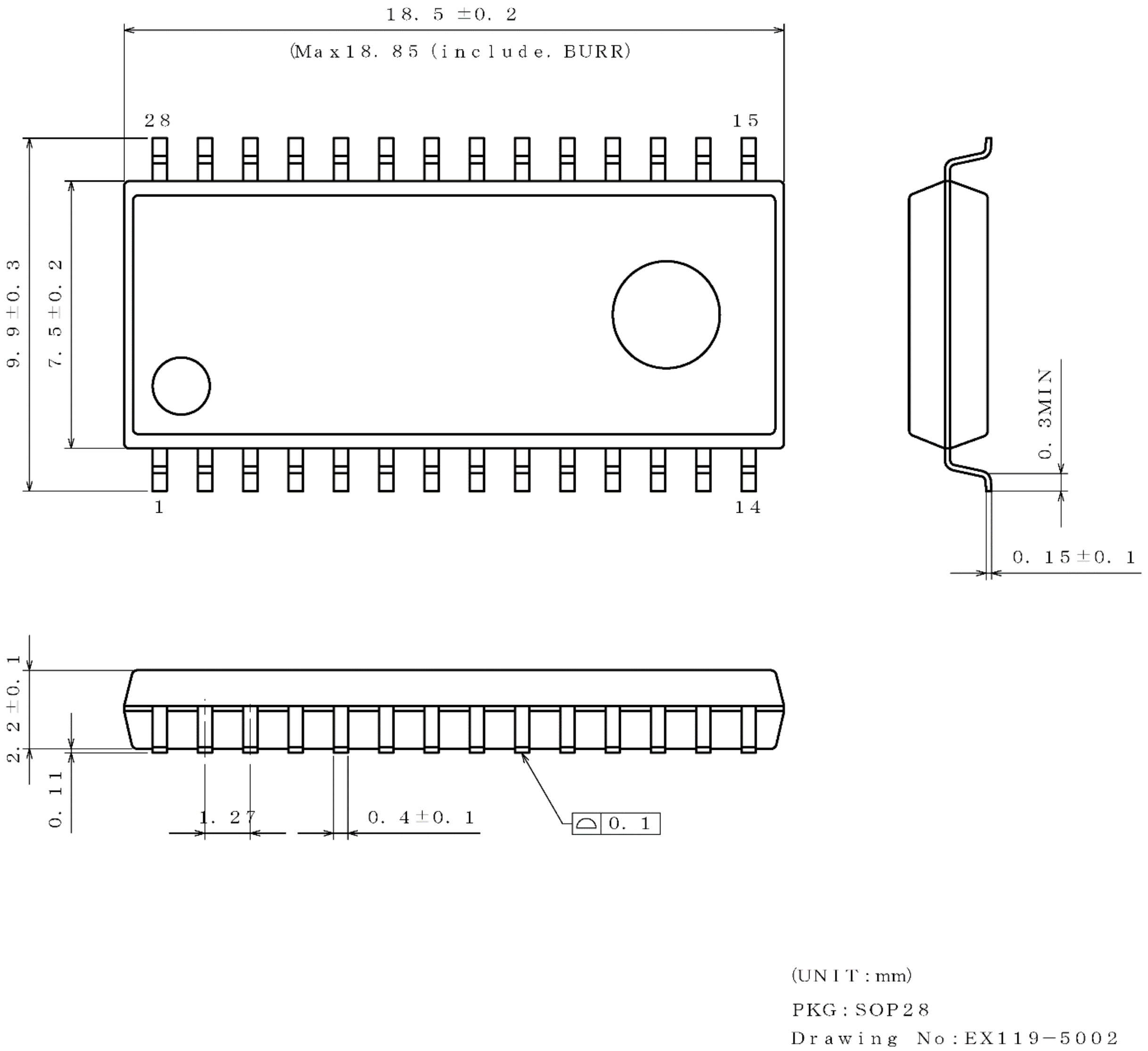
Packaging and forming specification
E2 : Embossed tape and reel

Marking Diagram



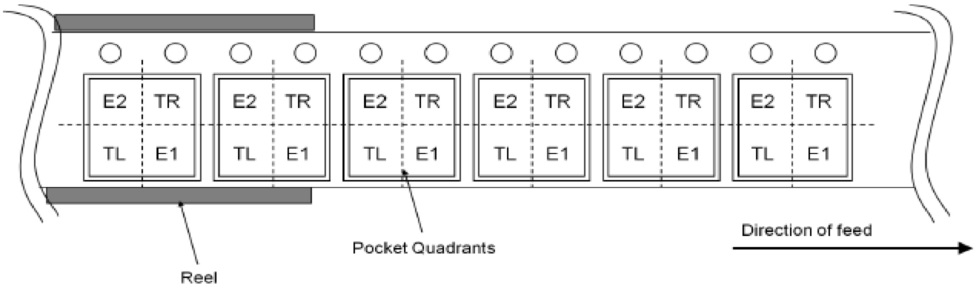
Physical Dimension and Packing Information

Package Name	SOP28



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
18.May.2018	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
    - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
    - [b] the temperature or humidity exceeds those recommended by ROHM
    - [c] the Products are exposed to direct sunshine or condensation
    - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

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3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

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