Gate Driver Providing Galvanic Isolation Series

Isolation Voltage 3750 Vrms 1ch Gate Driver Providing Galvanic Isolation

BM61M41RFV-C

General Description

The BM61M41RFV-C is a gate driver with an isolation voltage of 3750 Vrms, I/O delay time of 65 ns, and minimum input pulse width of 60 ns. It has the Under-Voltage Lockout (UVLO) function and Miller clamp function.

Key Specifications

■ Isolation Voltage:	3750 Vrms
■ Maximum Gate Drive Voltage:	24 V
■ I/O Delay Time:	65 ns(Max)
■ Minimum Input Pulse Width:	60 ns
■ Output Current	4 A

Features

- AEC-Q100 Qualified(Note 1)
- Providing Galvanic Isolation
- Active Miller Clamping
- Under-Voltage Lockout Function
- UL1577 Recognized: File E356010

(Note 1) Grade1

Package

	W(Typ) x D(Typ) x H(Max)
SSOP-B10W	3.5 mm x10.2 mm x 1.9 mm

SSOP-B10W

Applications

- Si MOSFET Gate Drive

Typical Application Circuits

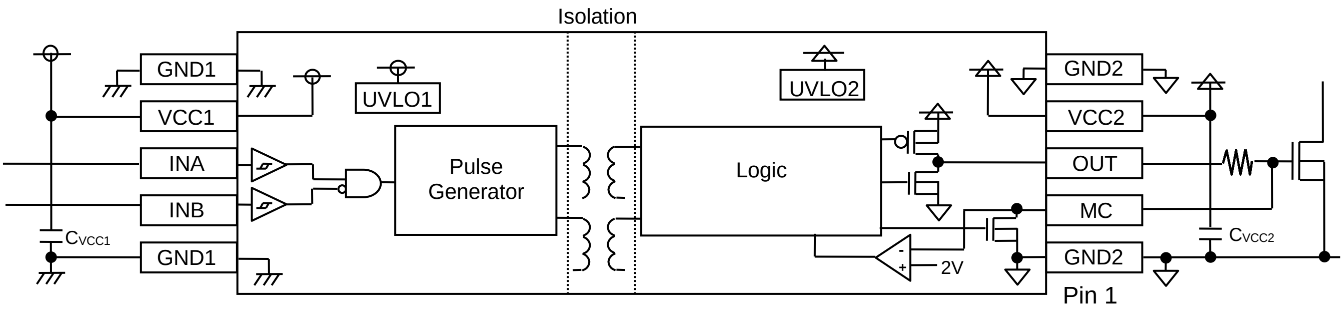


Figure 1. For Driving Si MOSFET without Negative Power Supply

○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays

Contents

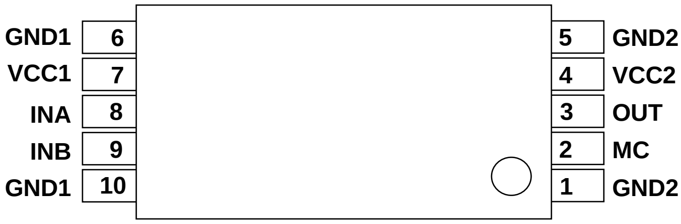
Recommended Range of External Constants

Pin Name	Symbol	Recommended Value			Unit
		Min	Typ	Max	
VCC1	C_{VCC1}	0.1	1.0	-	μF
VCC2	C_{VCC2}	0.01	-(Note 2)	-	μF

(Note 2) Value according to the load

Pin Configurations

(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function
1	GND2	Output-side ground pin
2	MC	Miller clamp pin
3	OUT	Output pin
4	VCC2	Output-side power supply pin
5	GND2	Output-side ground pin
6	GND1	Input-side ground pin
7	VCC1	Input-side power supply pin
8	INA	Control input A pin
9	INB	Control input B pin
10	GND1	Input-side ground pin

Pin Descriptions - continued

1. VCC1 (Input-side Power Supply Pin)
   The VCC1 pin is a power supply pin on the input side. To suppress voltage fluctuations due to the current to drive internal transformers, connect a bypass capacitor between the VCC1 and the GND1 pins.

2. GND1 (Input-side Ground Pin)
   The GND1 pin is a ground pin on the input side.

3. VCC2 (Output-side Power Supply Pin)
   The VCC2 pin is a power supply pin on the output side. To reduce voltage fluctuations due to OUT pin output current, connect a bypass capacitor between the VCC2 and the GND2 pins.

4. GND2 (Output-side Ground Pin)
   The GND2 pin is a ground pin on the output side.

5. INA, INB (Control Input A/B Pin)
   The INA and INB pins are used to determine output logic.

INB	INA	OUT
H	L	L
H	H	L
L	L	L
L	H	H

6. OUT (Output Pin)
   The OUT pin is used to drive the gate of a power device.

7. MC (Miller Clamp Pin)
   The MC pin is for preventing the increase in gate voltage due to the Miller current of the power device connected to the OUT pin. If the Miller Clamp function is not used, short-circuit the MC pin to the GND2 pin.

Description of Functions and Examples of Constant Setting

1. Miller Clamp Function
   When the INA=L or INB=H and OUT pin voltage < V_{MCON} (Typ 2V), the internal MOSFET of the MC pin is turned ON.

INA	INB	MC	Internal MOSFET of the MC Pin
L	X	Less Than V_{MCON}	ON
X	H	Less Than V_{MCON}	ON
H	L	X	OFF

X: Don't care

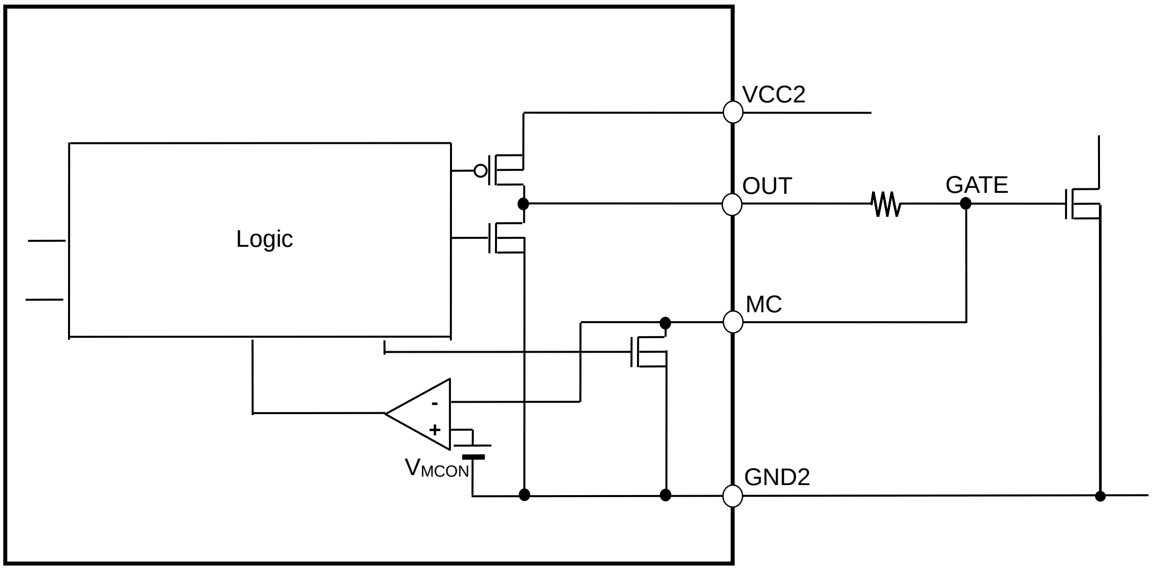


Figure 2. Block Diagram of Miller Clamp Function

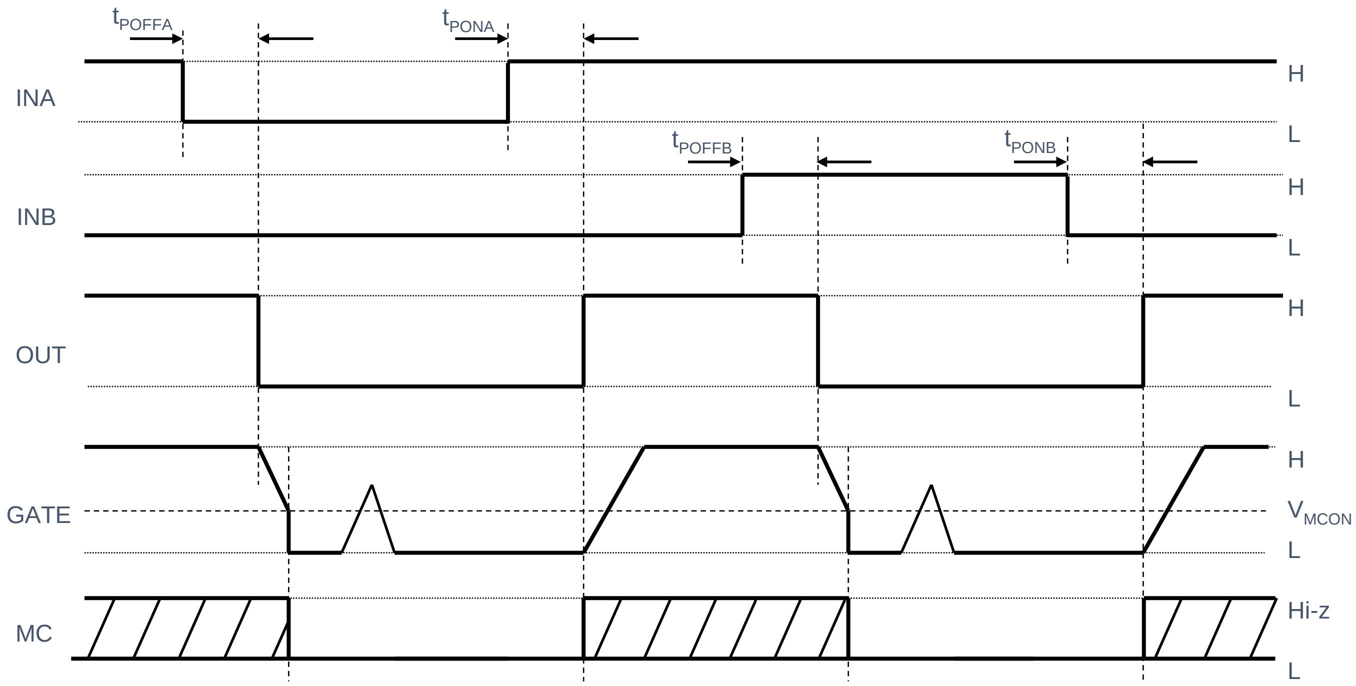


Figure 3. Timing Chart of Miller Clamp Function

Description of Functions and Examples of Constant Setting - continued

2. Under-Voltage Lockout (UVLO) Function

The BM61M41RFV-C has the Under-Voltage Lockout (UVLO) function both on the Input-side and the output-side. When the power supply voltage drops to the UVLO ON voltage (input-side Typ 4.0 V, output-side 7.4 V), the OUT pin will output the "L" signal. In addition, to prevent malfunctions due to noises, a mask time of $t_{UVLO1MSK}$ (Typ 1.5 µs) and $t_{UVLO2MSK}$ (Typ 2.9 µs) are set on both the input-side and the output-side. After the UVLO on Input-side is released, the input signal will take effect from when the time after the input signal switches.

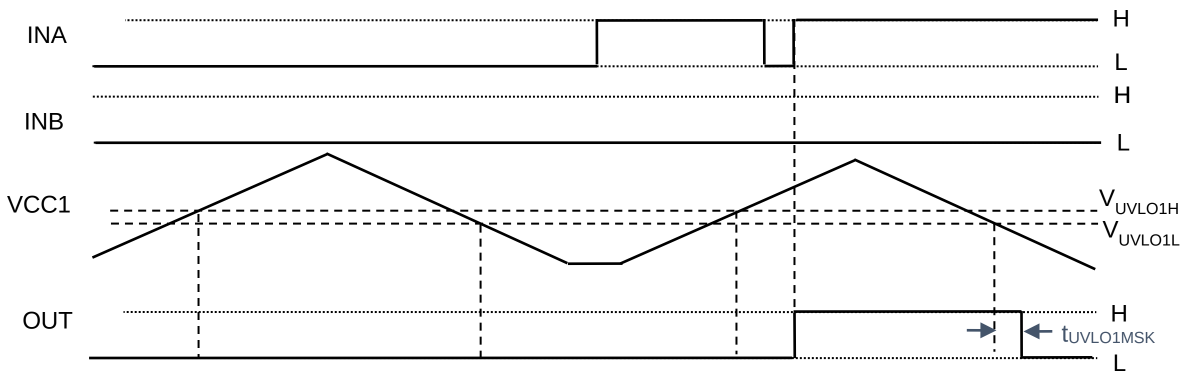


Figure 4. Timing Chart of Input-side UVLO Function

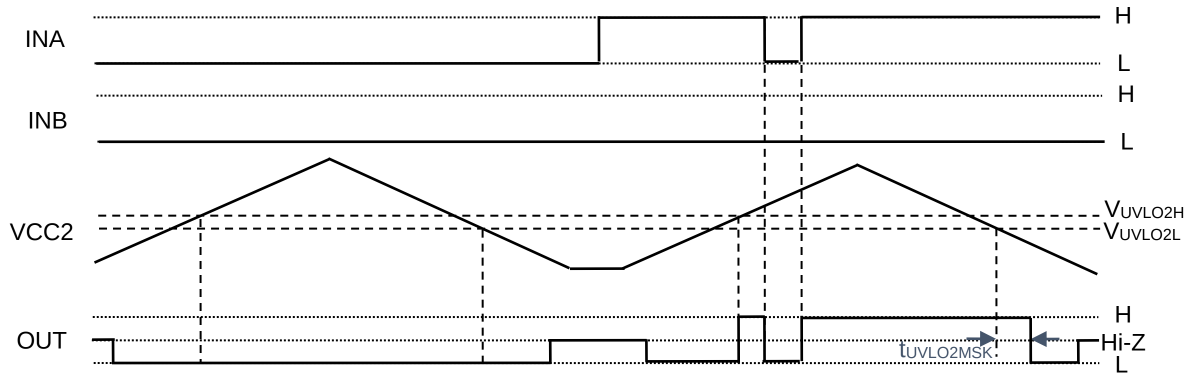


Figure 5. Timing Chart of Output-side UVLO Function

Description of Functions and Examples of Constant Setting - continued

3. I/O Condition Table

No.	Status	Input				Output	
		VCC1	VCC2	INB	INA	OUT	MC
1	VCC1 UVLO	UVLO	X	X	X	L	L
2	VCC2 UVLO	X	UVLO	X	X	L	L
3	INB Active	No UVLO	No UVLO	H	X	L	L
4	Normal Operation L Input	No UVLO	No UVLO	L	L	L	L
5	Normal Operation H input	No UVLO	No UVLO	L	H	H	Hi-Z

X: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Input-side Supply Voltage	V_{CC1}	-0.3 to +7.0 *(Note 3)*	V
Output-side Supply Voltage	V_{CC2}	-0.3 to +30.0 *(Note 4)*	V
INA Pin Input Voltage	V_{INA}	-0.3 to +VCC1+0.3 or +7.0 *(Note 3)*	V
INB Pin Input Voltage	V_{INB}	-0.3 to +VCC1+0.3 or +7.0 *(Note 3)*	V
OUT Pin Output Current (Peak 10µs)	$I_{OUTPEAK}$	self limited	A
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

***Caution 1**: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

***Caution 2**: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 3) Relative to GND1.
(Note 4) Relative to GND2.

Thermal Resistance *(Note 5)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 7)*	2s2p *(Note 8)*	
SSOP-B10W				
Input-side Junction to Ambient	θ_{JA1}	172.1	101.8	°C/W
Output-side Junction to Ambient	θ_{JA2}	180.2	108.9	°C/W
Input-side Junction to Top Characterization Parameter *(Note 6)*	Ψ_{JT1}	32	27	°C/W
Output-side Junction to Top Characterization Parameter *(Note 6)*	Ψ_{JT2}	82	60	°C/W

(Note 5) Based on JESD51-2A (Still-Air)
(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 7) Using a PCB board based on JESD51-3.
(Note 8) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input-side Supply Voltage	V_{CC1}(Note 9)	4.5	5.5	V
Output-side Supply Voltage	V_{CC2}(Note 10)	9	24	V
Operating Temperature	Topr	-40	+125	°C

(Note 9) Relative to GND1.
(Note 10) Relative to GND2.

Insulation Related Characteristics

Basic Insulation Requirements according to VDE0884-11(pending)

Parameter	Symbol	Characteristic	Unit
Insulation Classification Per EN 60664-1, Table 1 For Rated Main Voltage< 150 Vrms For Rated Main Voltage< 300 Vrms For Rated Main Voltage< 450 Vrms For Rated Main Voltage< 600 Vrms		Rated Impulse Voltage I - IV I - IV I - III I - III	-
Climatic Classification		40/125/21	-
Pollution Decree(EN 60664-1)		2	-
Minimum External Clearance	CLR	8.1	mm
Minimum External Creepage	CPG	8.1	mm
Minimum Internal Gap (Internal Clearance)		0.012	mm
Minimum Comparative Tracking Index	CTI	>400	-
Minimum Repetitive Insulation Voltage	V_{IORM}	891	V_{peak}
Input to Output Test Voltage, Method b V_{IORM} × 1.875= VPR, Productive Test, tm = 1 s, Partial Discharge < 5 pC	V_{PR}	1671	V_{peak}
Surge Isolation Voltage	V_{IOSM}	6000	V_{peak}
Highest Allowable Voltage, 1 min	V_{IOTM}	5300	V_{peak}
Insulation Resistance at T_S, V_{IO} = 500 V	R_{IO}	$>10^9$	Ω

Recognized under UL 1577

Description	Symbol	Characteristic	Unit
Insulation Withstand Voltage / 1 min	V_{ISO}	3750	Vrms
Insulation Test Voltage / 1 s	V_{ISO}	4500	Vrms

UL1577 Ratings Table
Following values are described in UL Report.

Parameter	Values	Units	Conditions
Side 1 (Input Side) Circuit Current	0.4	mA	VCC1=5.0V, OUT=L
Side 2 (Output Side) Circuit Current	0.7	mA	VCC2=15V, OUT=L
Side 1 (Input Side) Consumption Power	2	mW	VCC1=5.0V, OUT=L
Side 2 (Output Side) Consumption Power	12.6	mW	VCC2=15V, OUT=L
Isolation Voltage	3750	Vrms	
Maximum Operating (Ambient) Temperature	125	°C	
Maximum Junction Temperature	150	°C	
Maximum Storage Temperature	150	°C	
Maximum Data Transmission Rate	8.33	MHz	

Electrical Characteristics

(Unless otherwise specified Ta=-40°C to +125°C, V_{CC1}=4.5 V to 5.5 V, V_{CC2}=9 V to 24 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
General						
Input-side Circuit Current 1	I_{CC11}	0.2	0.4	1.0	mA	INA=L,INB=H
Input-side Circuit Current 2	I_{CC12}	1.0	2.0	4.0	mA	INA=100kHz, Duty=50%
Output-side Circuit Current 1	I_{CC21}	0.30	0.70	1.20	mA	OUT=L
Output-side Circuit Current 2	I_{CC22}	0.22	0.52	0.90	mA	OUT=H
Logic Block						
Logic High Level Input Voltage	V_{INH}	2.0	-	V_{CC1}	V	INA, INB
Logic Low Level Input Voltage	V_{INL}	0	-	0.8	V	INA, INB
Logic Pull-down Resistance	R_{IND}	25	50	100	kΩ	INA
Logic Pull-up Resistance	R_{INU}	25	50	100	kΩ	INB
Logic Input Minimum Pulse Width	t_{INMIN}	60	-	-	ns	INA, INB
Output						
OUT ON Resistance (Source)	R_{ONH}	0.3	0.67	1.5	Ω	I_{OUT}=-40 mA
OUT ON Resistance (Sink)	R_{ONL}	0.15	0.45	0.98	Ω	I_{OUT}=40 mA
OUT Maximum Current (Source)	$I_{OUTMAXH}$	4.0	-	-	A	V_{CC2}=18 V, Guaranteed by Design
OUT Maximum Current (Sink)	$I_{OUTMAXL}$	4.0	-	-	A	V_{CC2}=18 V, Guaranteed by Design
Turn ON Time	t_{PONA}	45	55	65	ns	INA=PWM, INB=L
	t_{PONB}	45	55	65	ns	INA=H, INB=PWM
Turn OFF Time	t_{POFFA}	45	55	65	ns	INA=PWM, INB=L
	t_{POFFB}	45	55	65	ns	INA=H, INB=PWM
Propagation Distortion	t_{PDISTA}	-10	0	+10	ns	$t_{POFFA} - t_{PONA}$
	t_{PDISTB}	-10	0	+10	ns	$t_{POFFB} - t_{PONB}$
Part to Part Skew	t_{SK-PP}	-	-	20	ns	
Rise Time	t_{RISE}	-	15	-	ns	2 nF between OUT-GND2
Fall Time	t_{FALL}	-	15	-	ns	2 nF between OUT-GND2
MC ON Resistance	R_{ONMC}	0.15	0.45	0.98	Ω	I_{MC}=40 mA
MC ON Threshold Voltage	V_{MCON}	1.8	2	2.2	V	
Common Mode Transient Immunity	CM	100	-	-	kV/µs	Guaranteed by Design
Protection Functions						
V_{CC1} UVLO OFF Voltage	V_{UVLO1H}	3.95	4.2	4.45	V	
V_{CC1} UVLO ON Voltage	V_{UVLO1L}	3.75	4.0	4.25	V	
V_{CC1} UVLO Mask Time	$t_{UVLO1MSK}$	0.4	1.5	5.0	µs	
V_{CC2} UVLO OFF Voltage	V_{UVLO2H}	7.4	7.8	8.2	V	
V_{CC2} UVLO ON Voltage	V_{UVLO2L}	7.0	7.4	7.8	V	
V_{CC2} UVLO Mask Time	$t_{UVLO2MSK}$	1.0	2.9	5.0	µs	

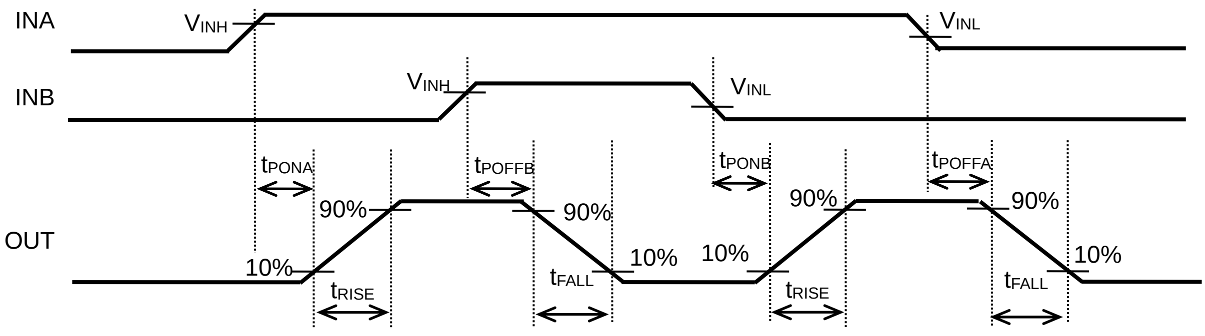


Figure 6. Timing Chart of IN-OUT

Typical Performance Curves

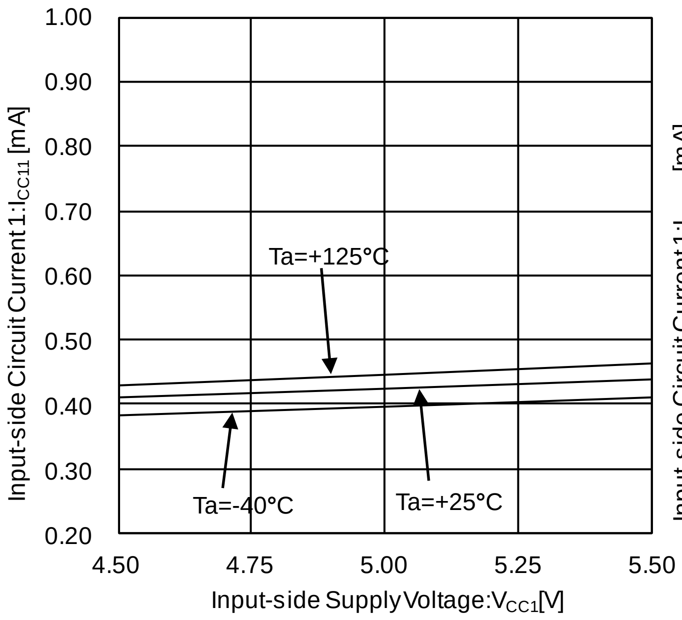


Figure 7. Input-side Circuit Current 1 vs Input-side Supply Voltage

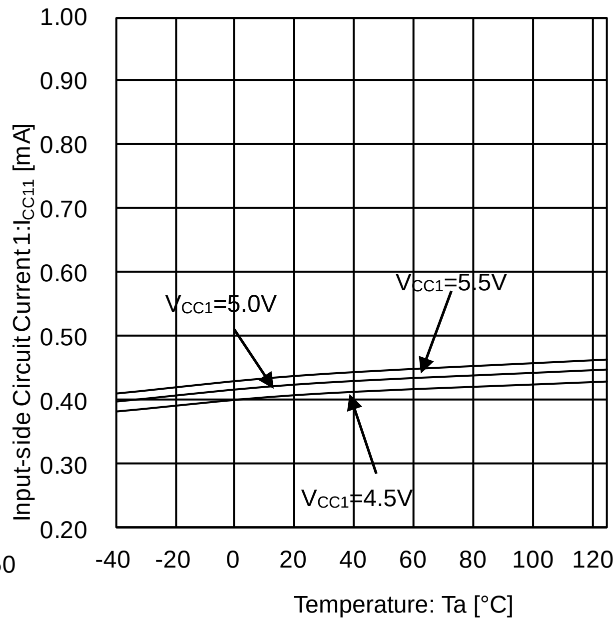


Figure 8. Input-side Circuit Current 1 vs Temperature

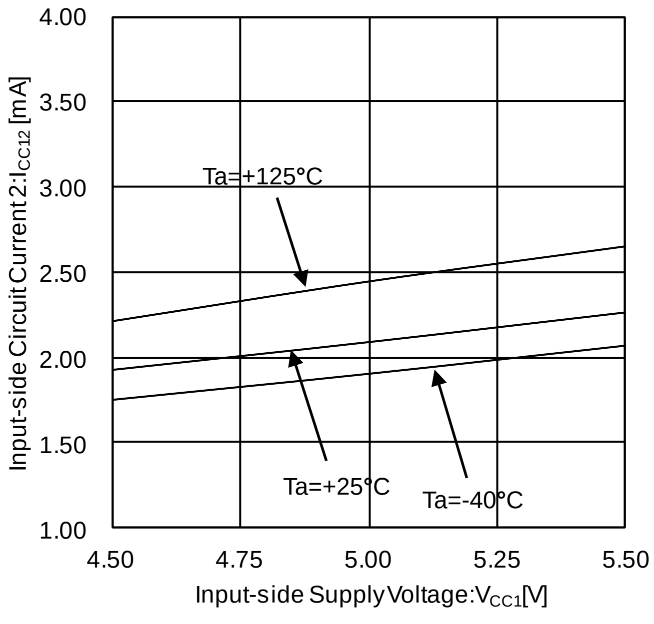


Figure 9. Input-side Circuit Current 2 vs Input-side Supply Voltage (At INA=100 kHz, Duty=50 %)

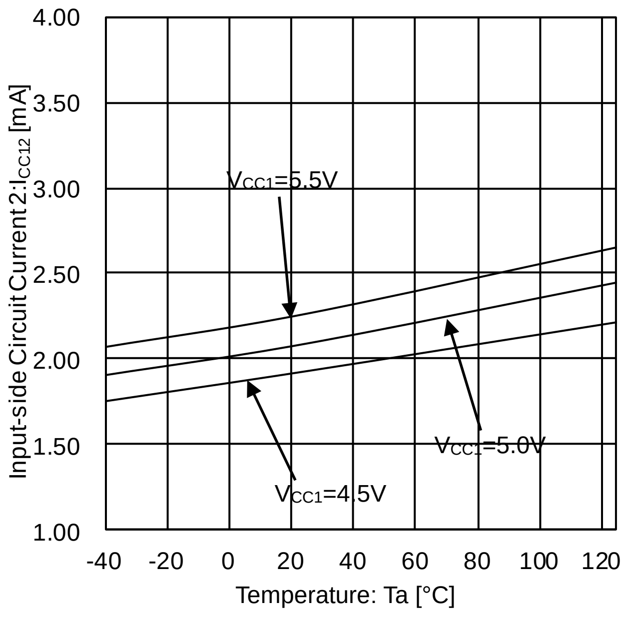


Figure 10. Input-side Circuit Current 2 vs Temperature (At INA=100 kHz, Duty=50 %)

Typical Performance Curves - continued

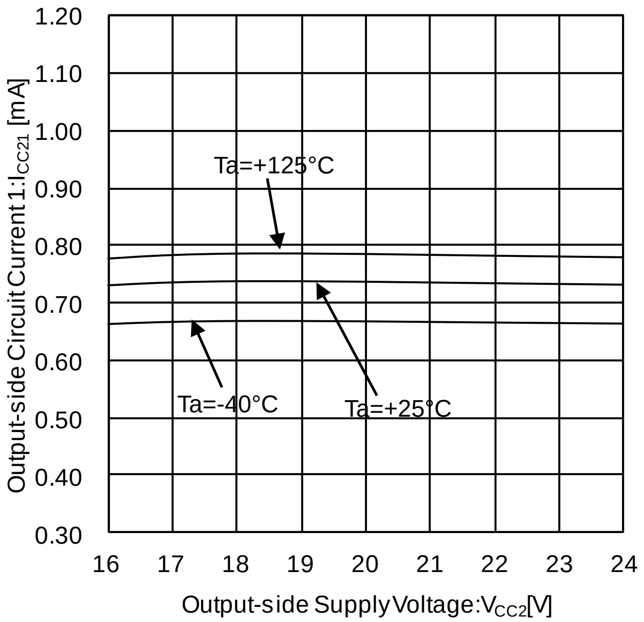


Figure 11. Output-side Circuit Current 1 vs Output-side Supply Voltage (At OUT=L)

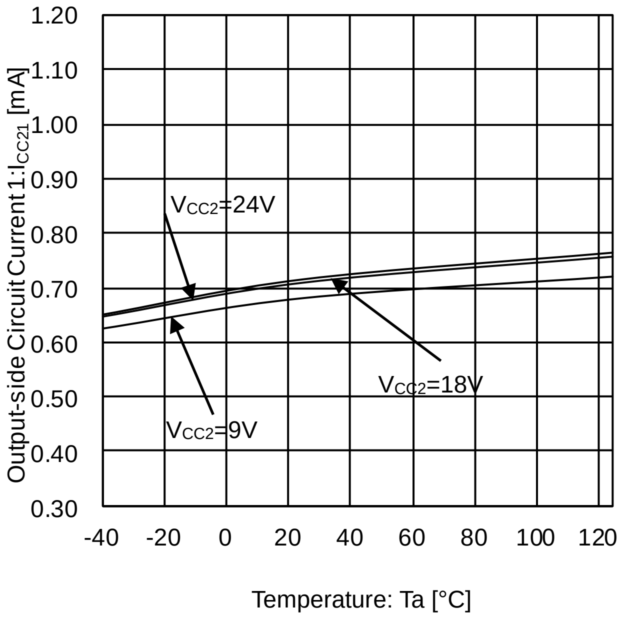


Figure 12. Output-side Circuit Current 1 vs Temperature (At OUT=L)

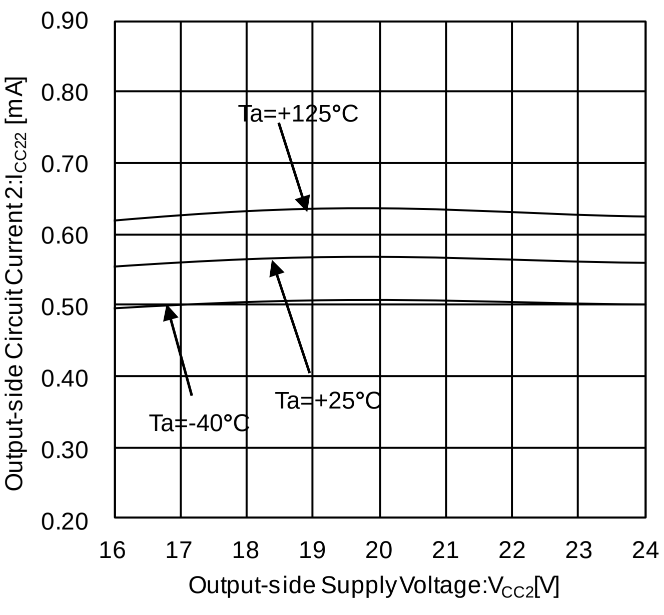


Figure 13. Output-side Circuit Current 2 vs Output-side Supply Voltage (At OUT=H)

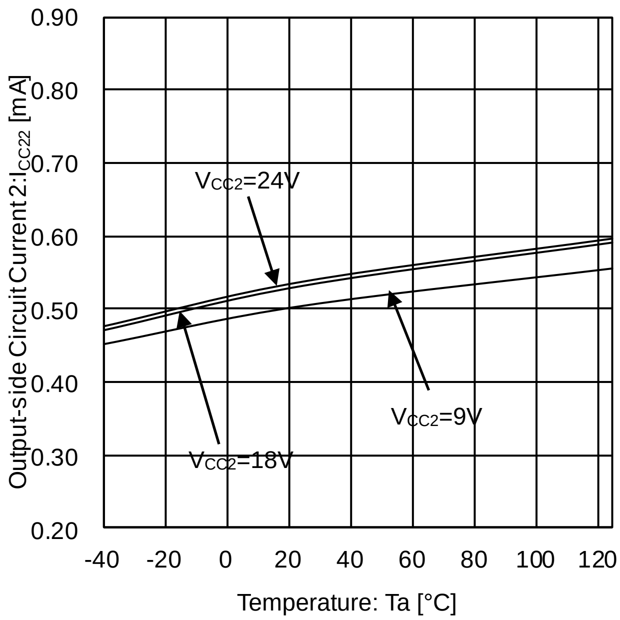


Figure 14. Output-side Circuit Current 2 vs Temperature (At OUT=H)

Typical Performance Curves - continued

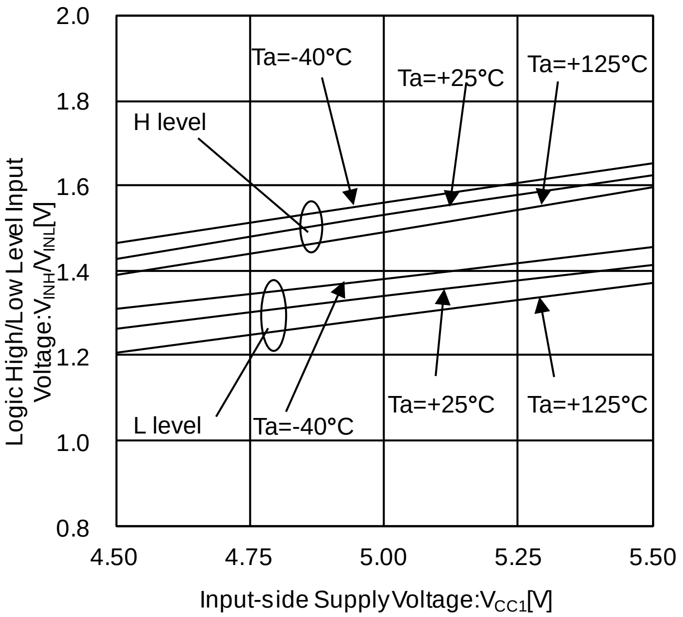


Figure 15. Logic High/Low Level Input Voltage vs Input-side Supply Voltage

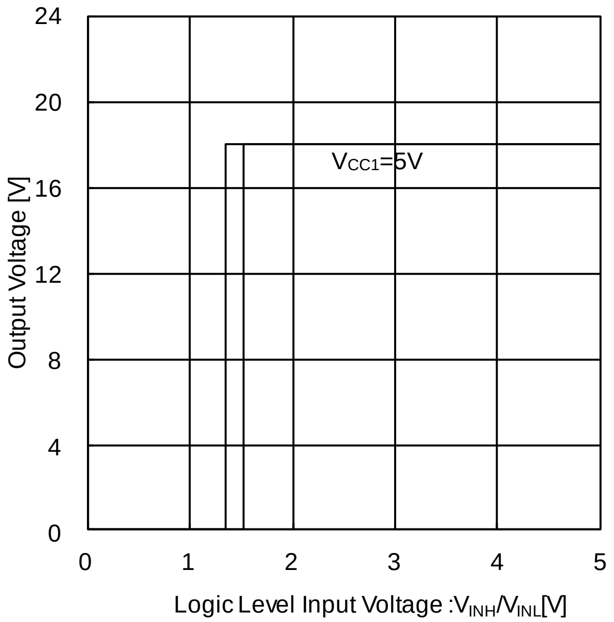


Figure 16. Output Voltage vs Logic Level Input Voltage (INA)
(V_{CC1}=5 V, V_{CC2}=18 V, Ta=25 °C)

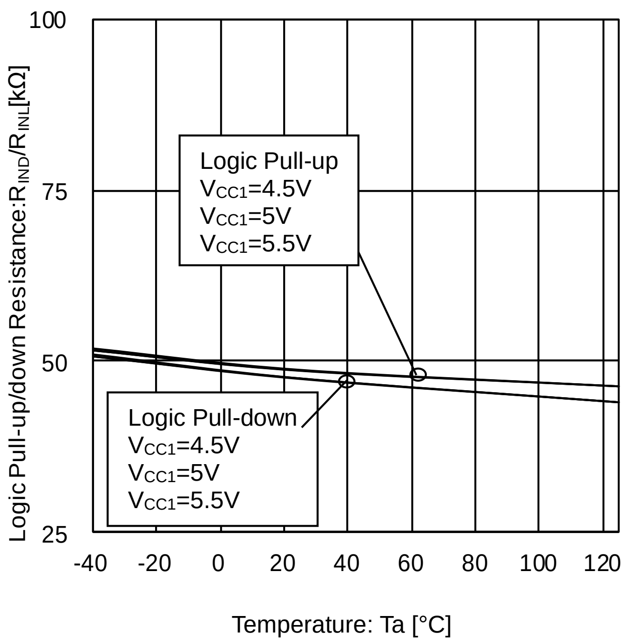


Figure 17. Logic Pull-up/down Resistance vs Temperature

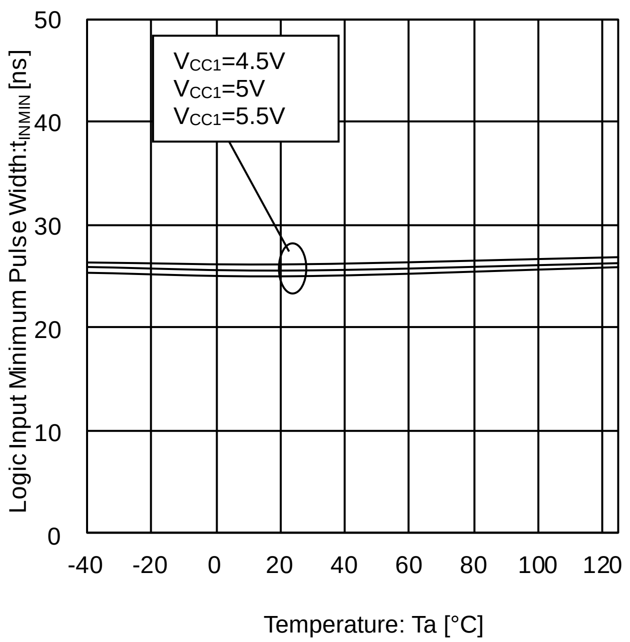


Figure 18. Logic Input Minimum Pulse Width vs Temperature

Typical Performance Curves - continued

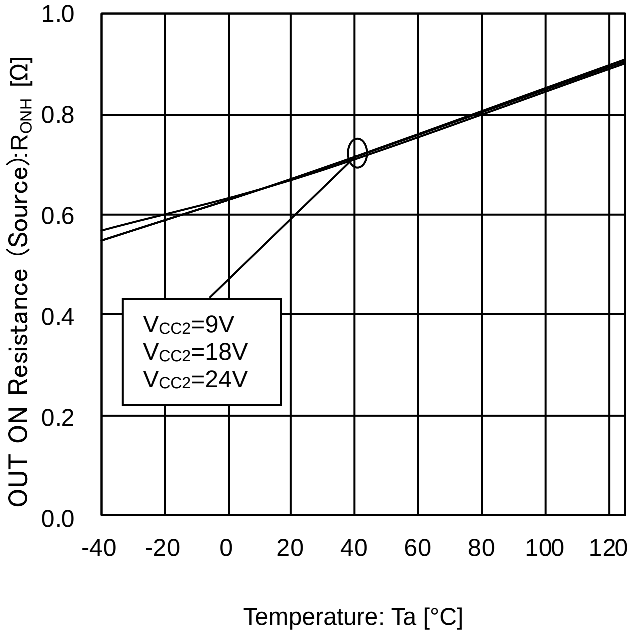


Figure 19. OUT ON Resistance (Source) vs Temperature

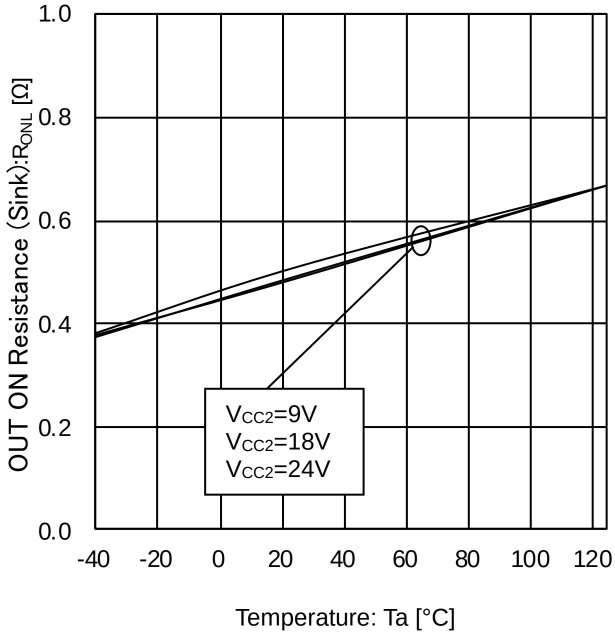


Figure 20. OUT ON Resistance (Sink) vs Temperature

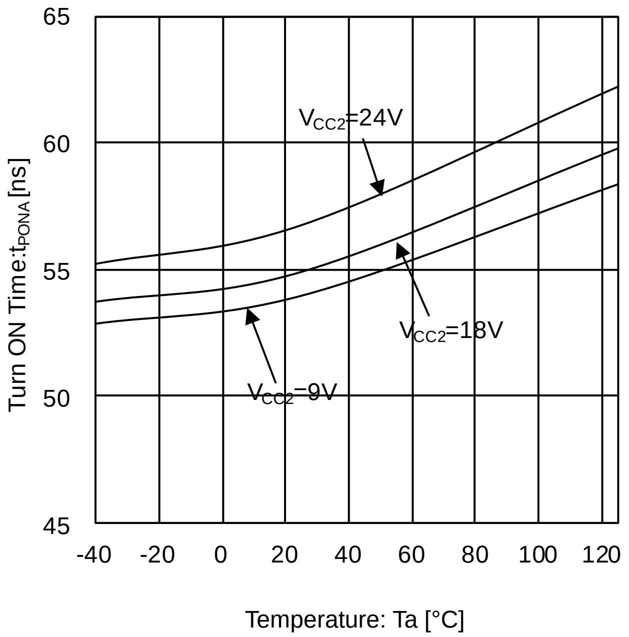


Figure 21. Turn ON Time vs Temperature (INA=PWM, INB=L)

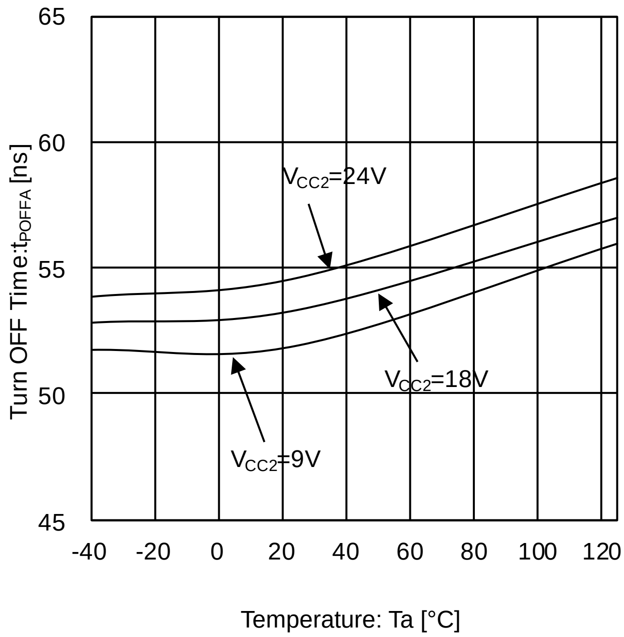


Figure 22. Turn OFF Time vs Temperature (INA=PWM, INB=L)

Typical Performance Curves - continued

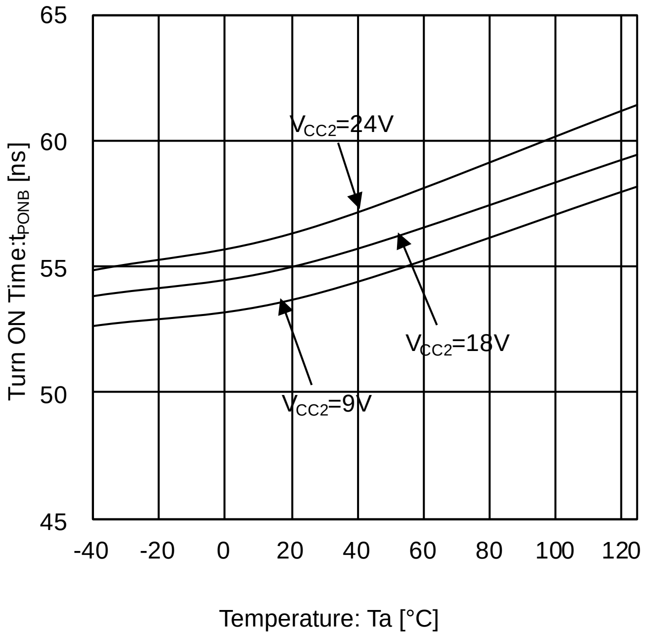


Figure 23. Turn ON Time vs Temperature
(INA=H, INB=PWM)

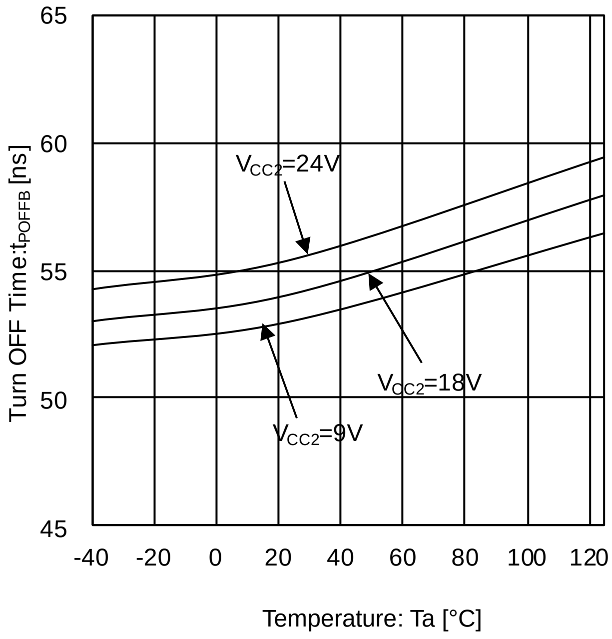


Figure 24. Turn OFF Time vs Temperature
(INA=H, INB=PWM)

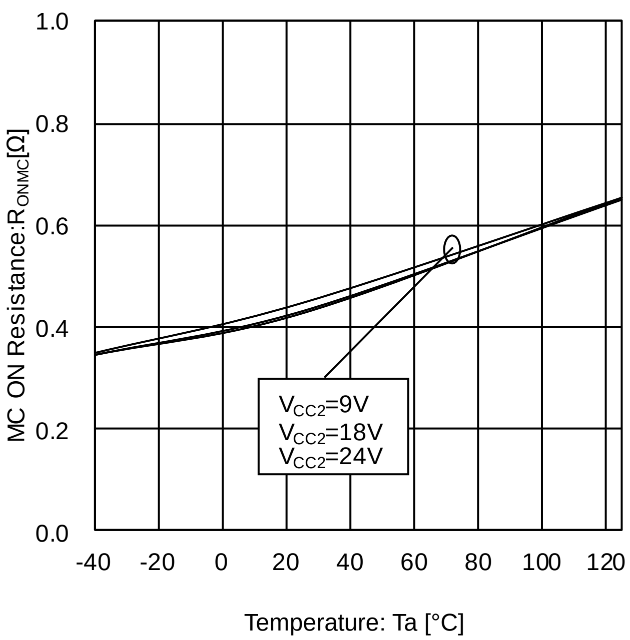


Figure 25. MC ON Resistance vs Temperature

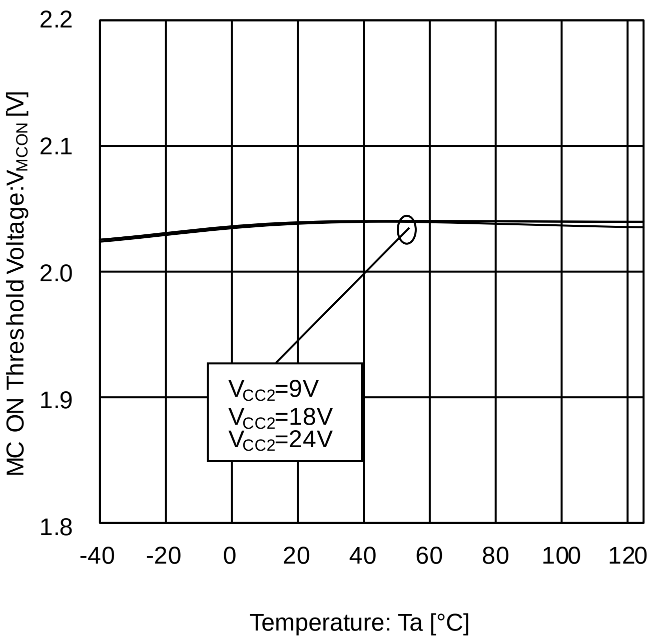


Figure 26. MC ON Threshold Voltage vs Temperature

Typical Performance Curves - continued

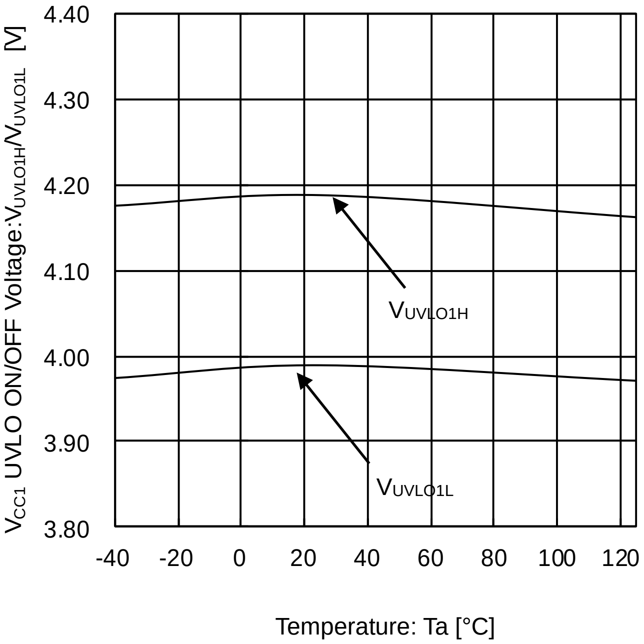


Figure 27. V_{CC1} UVLO ON/OFF Voltage vs Temperature

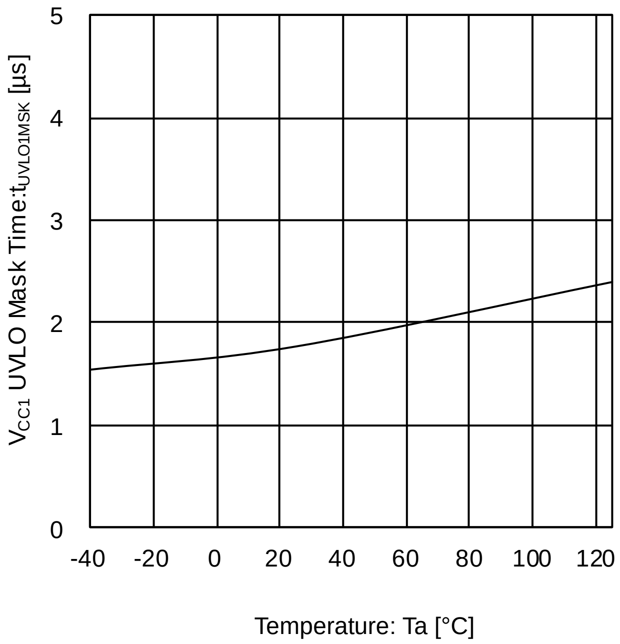


Figure 28. V_{CC1} UVLO Mask Time vs Temperature

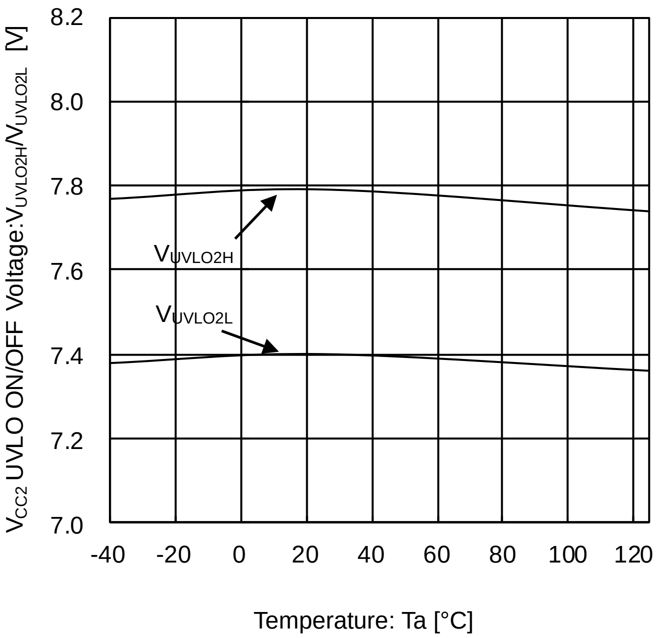


Figure 29. V_{CC2} UVLO ON/OFF Voltage vs Temperature

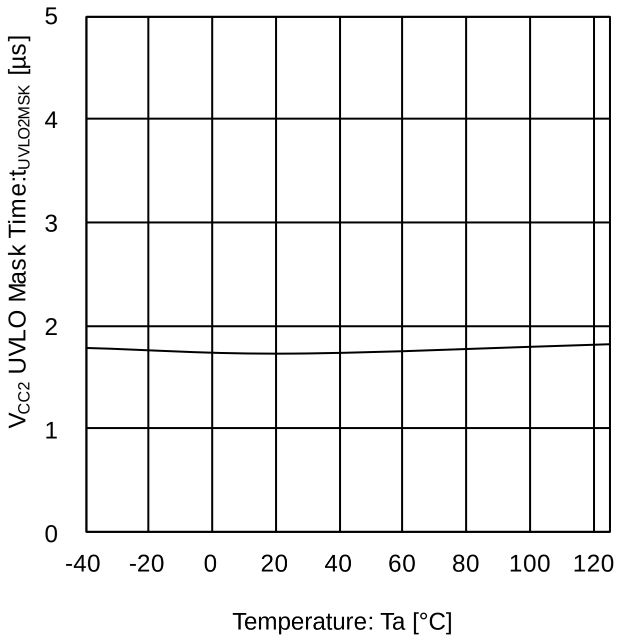


Figure 30. V_{CC2} UVLO Mask Time vs Temperature

Application Examples

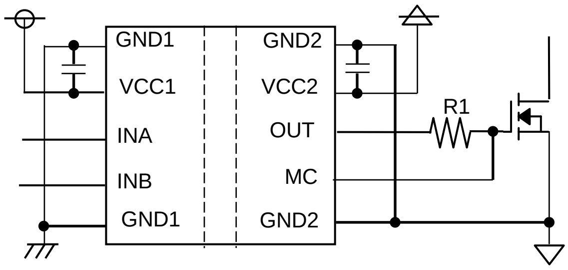


Figure 31. Driving Si MOSFET

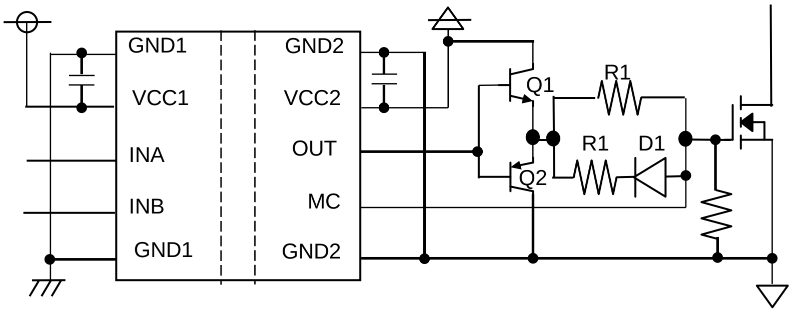
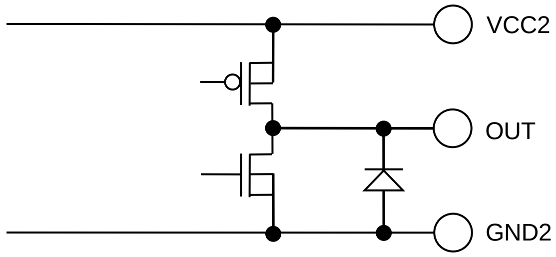
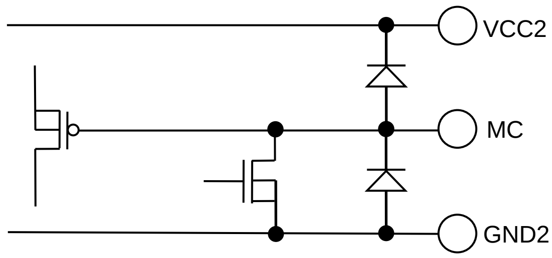
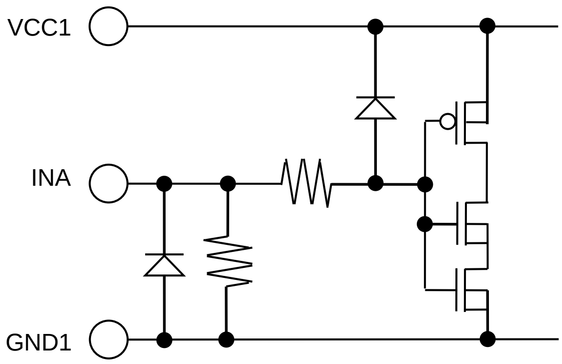
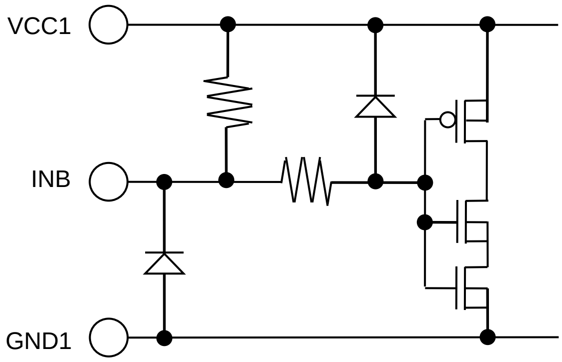


Figure 32. Driving Si MOSFET with Buffer Circuit

Recommended Parts

	Manufacturer	Element	Part Number
R1	ROHM	Resistor	LTR18EZP,LTR50UZP
Q1	ROHM	NPN Transistor	2SCR542PFRA
Q2	ROHM	PNP Transistor	2SAR542PFRA
D1	ROHM	Diode	RBR3MM30ATF,RBR5LAM30ATF

I/O Equivalence Circuits

<table>
<tr><td rowspan="2">Pin No.</td><td>Pin Name</td><td rowspan="2">I/O Equivalence Circuits</td></tr>
<tr><td>Function</td></tr>
<tr><td rowspan="2">3</td><td>OUT</td><td rowspan="2">
</td></tr>
<tr><td>Output Pin</td></tr>
<tr><td rowspan="2">2</td><td>MC</td><td rowspan="2">
</td></tr>
<tr><td>Miller Clamp pin</td></tr>
<tr><td rowspan="2">8</td><td>INA</td><td rowspan="2">
</td></tr>
<tr><td>Control Input A pin</td></tr>
<tr><td rowspan="2">9</td><td>INB</td><td rowspan="2">
</td></tr>
<tr><td>Control Input B pin</td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. Regarding the Input Pin of the IC

This IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

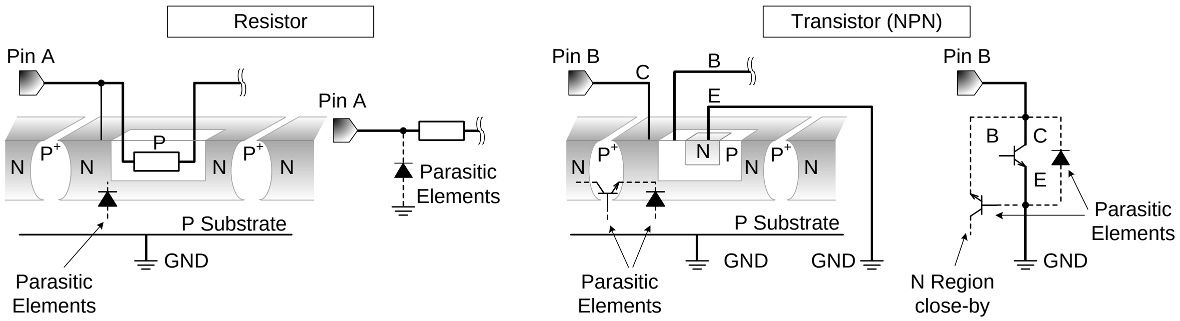


Figure 33. Example of IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

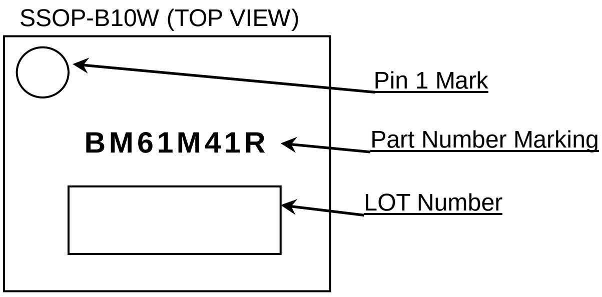
B	M	6	1	M	4	1	R	F	V	-	CE2

Part Number

Package
FV: SSOP-B10W

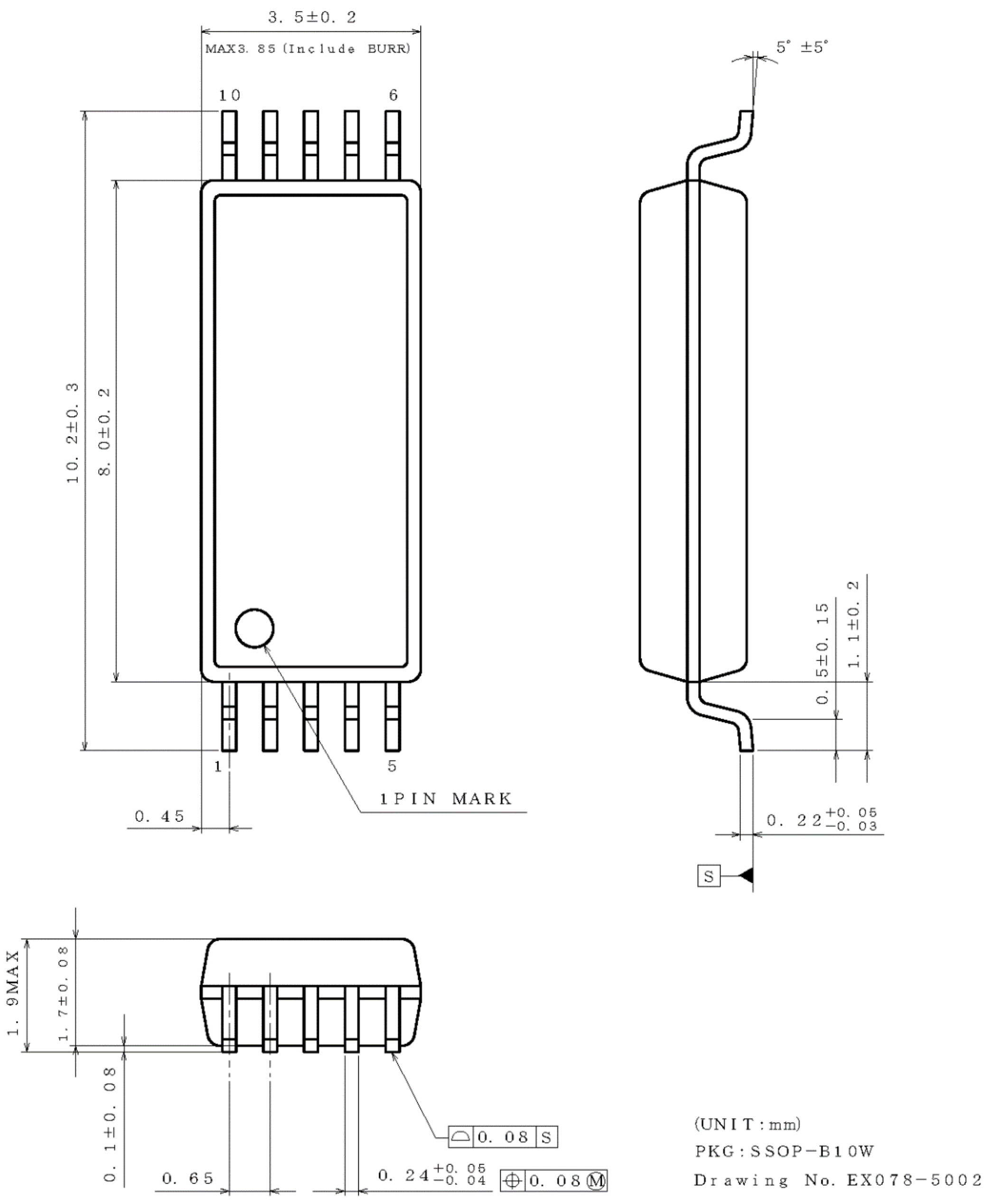
Product class
C: for Automotive applications
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



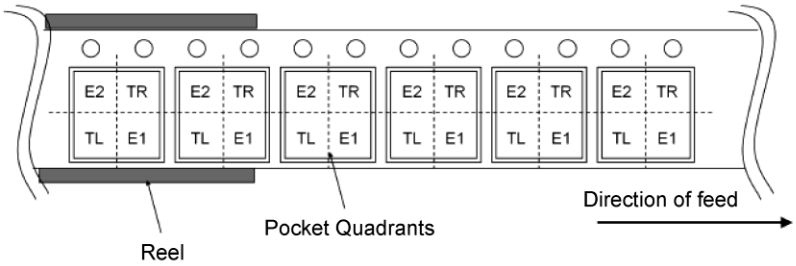
Physical Dimension and Packing Information

Package Name	SSOP-B10W



< Tape and Reel Information >

Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
24.Aug.2018	001	New Release
03.Sep.2019	002	Page 1: Changed the sentence in “Applications” Before: SiC MOSFET Gate Drive → After: Si MOSFET Gate Drive Page 6: Corrected the value of UVLO ON voltage in “Under-Voltage Lockout (UVLO) Function” Before: output-side 7.8 V → After: output-side 7.4V Page 10: Corrected “V_{CC2} UVLO OFF Voltage” Before: Min = 7.0 V, Typ = 7.4 V, Max = 7.8 V → After: Min = 7.4 V, Typ = 7.8 V, Max = 8.2 V Corrected “V_{CC2} UVLO ON Voltage” Before: Min = 7.4 V, Typ = 7.8 V, Max = 8.2 V → After: Min = 7.0 V, Typ = 7.4 V, Max = 7.8 V Page 16: Corrected the graph on Figure 29. “V_{CC2} UVLO ON/OFF Voltage vs Temperature” Page 17: Changed the title of Figure 31and Figure 32. Before: Driving SiC → After: Driving Si MOSFET (Figure 31) Before: Driving SiC with Buffer Circuit → After: Driving Si MOSFET with Buffer Circuit (Figure 32)
30.Mar.2020	003	Page 1: Changed Features Before: UL1577(pending) → After: UL1577 Recognized Page 9: Corrected Insulation Related Characteristic Before: Reinforced Insulation → After: Basic Insulation Before: VDE0884-10(pending) → After: VDE0884-11(pending) Before: Recognized under UL 1577(pending) → After: Recognized under UL 1577 Before: V_{pk} → After: V_{peak} Corrected Highest Allowable Voltage, 1min Before: 3750Vrms → After: 5300V_{peak} Page 10: Added UL1577 Rating Table

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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    - [b] the temperature or humidity exceeds those recommended by ROHM
    - [c] the Products are exposed to direct sunshine or condensation
    - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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