

D/A Converters

Standard 8bit 4ch・6ch Type

BH2227FV BH2228FV

General Description

The BH2227FV and BH2228FV ICs are 8bit R-2R-type D/A converters with 4 and 6 channels, respectively. Optimized circuitry allows two output voltages to be supplied (3V/5V). Furthermore, the built-in RESET function ensures that the output voltage at all channels is LOW during power up. A broad power supply voltage range is available (2.7V to 5.5V), providing design flexibility.

Features

- Suitable for 2 independent power sources (3V/5V)
- Built-in RESET function
- High speed output response characteristics
- 3-line serial interface

Applications

DVCs, DSCs, DVDs, CD-Rs, CD-RWs

Key Specifications

- Power Source Voltage Range: 2.7V to 5.5V
- Current Consumption: 0.8mA(Typ)
- Differential Non Linearity Error: $\pm 1.0\text{LSB}$
- Integral non Linearity Error: $\pm 1.5\text{LSB}$
- Output current Performance: $\pm 1.0\text{mA}$
- Settling Time: 100 μs (Min)
- Data Transfer Frequency: 10MHz(Max)
- Action Temperature Range: -20°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)



Lineup

Number of channels	Input method	Data latch method	Package		Orderable Part Number
4ch	CMOS	CSB method	SSOP-B14	Reel of 2500	BH2227FV-E2
6ch					BH2228FV-E2

Pin Descriptions and Block Diagrams

(BH2227FV)

Terminal	Terminal Name	Function
1	AO1	Analog output terminal
2	AO2	
3	TESTMONI1	Test terminal (OPEN at normal use)
4	TESTMONI2	
5	AO3	Analog output terminal
6	AO4	
7	NC	Internally not connected yet
8	NC	
9	VDD	Power source terminal (AO3, 4 full scale voltage use in common)
10	CSB	Chip select signal input terminal
11	CLK	Serial clock input terminal
12	DI	Serial data input terminal
13	VFS	AO1,2 full scale Voltage setting terminal
14	VSS	Ground terminal

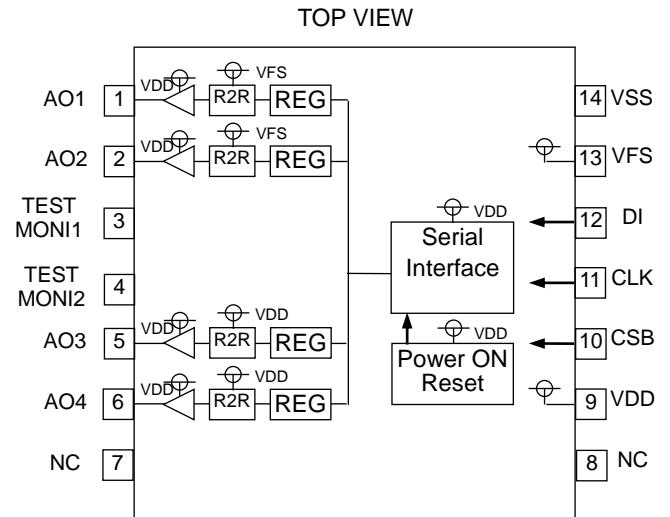


Figure 1. BH2227FV

(BH2228FV)

Terminal	Terminal Name	Function
1	AO1	Analog output terminal
2	AO2	
3	AO3	
4	AO4	
5	AO5	
6	AO6	Internally not connected yet
7	NC	
8	NC	Internally not connected yet
9	VDD	
10	CSB	Chip select signal input terminal
11	CLK	Serial clock input terminal
12	DI	Serial data input terminal
13	VFS	AO1,2,3 full scale Voltage setting terminal
14	VSS	Ground terminal

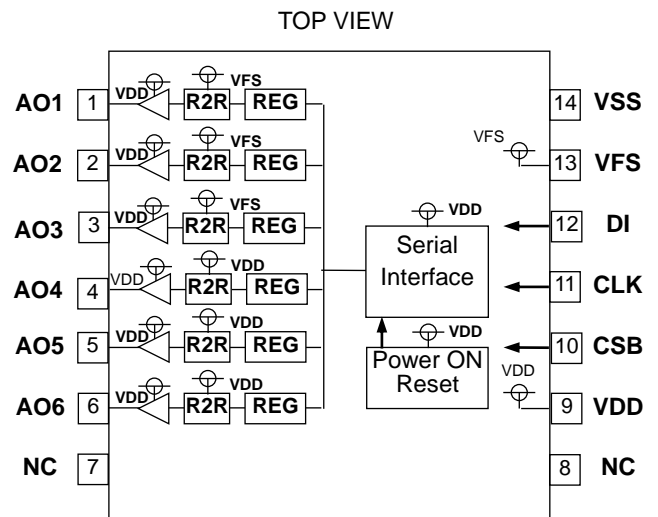


Figure 2. BH2228FV

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit	Remark
Power Source Voltage	V _{DD}	-0.3 to +7.0	V	-
Terminal Voltage	V _{IN}	-0.3 to V _{CC}	V	-
Storage Temperature Range	T _{stg}	-55 to +125	°C	-
Power Dissipation	P _d	0.40 (Note 1)	W	-

(Note 1) Derated at 4.0mW/°C at Ta>25°C

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Limit			Unit	Remark
		Min	Typ	Max		
VDD Power Source Voltage	V _{DD}	2.7	-	5.5	V	(Note 2)
VFS Voltage to be Impressed	V _{FS}	2.7	-	V _{DD}	V	(Note 2)
Terminal Input Voltage Range	V _{IN}	0	-	V _{DD}	V	-
Analog Output Current	I _{OUT}	-1.0	-	+1.0	mA	-
Action Temperature Range	T _{opr}	-20	-	+85	°C	-
Serial Clock Frequency	f _{CLK}	-	1.0	10.0	MHz	-
Limit Load Capacitance	C _L	-	-	0.1	μF	-

(Note 2) Set the power source voltage so that V_{DD} ≥ V_{FS}.

Electrical Characteristics

(Unless otherwise specified, V_{DD}=V_{FS}=3.0V, R_L=OPEN, C_L=0pF, Ta=25°C)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
<Current Consumption>						
VDD System	I _{DD}	-	0.5	1.5	mA	V _{DD} =5V , CLK=1MHz
VFS System	I _{FS}	-	0.3	0.9	mA	
<Logic Interface>						
L Input Voltage	V _{IL}	V _{SS}	-	0.6	V	V _{DD} =5.0V
H Input Voltage	V _{IH}	2.4	-	V _{DD}	V	V _{DD} =5.0V
Input Current	I _{IN}	-10	-	+10	μA	
<Buffer Amplifier>						
Output Zero Scale Voltage	V _{ZS1}	V _{SS}	-	0.1	V	00h setting, at no load
	V _{ZS2}	V _{SS}	-	0.3	V	00H setting, I _{OL} =1.0mA
Output Full Scale Voltage	V _{FS1}	V _{DD} -0.1	-	V _{DD}	V	FFH setting, at no load
	V _{FS2}	V _{DD} -0.3	-	V _{DD}	V	FFH setting, I _{OH} =1.0mA
	V _{FS3}	V _{FS} -0.1	-	V _{FS}	V	FFH setting, at no load
	V _{FS4}	V _{FS} -0.3	-	V _{FS}	V	FFH setting, I _{OH} =1.0mA
<D/A Converter Precision>						
Differential Non Linearity Error	DNL	-1.0	-	+1.0	LSB	Input code 02H to FDH
Integral Non Linearity Error	INL	-1.5	-	+1.5	LSB	Input code 02H to FDH
VDD Power Source Voltage Rise Time	t _{rVDD}	100	-	-	μs	V _{DD} =0V to 2.7V
Power ON Reset Release Voltage	V _{POR}	-	1.9	-	V	

Timing Chart

(Unless otherwise specified, $V_{DD} = V_{FS} = 3.0V$, $R_L = OPEN$, $C_L = 0pF$, $T_a = 25^\circ C$)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
CLK L Level Time	t_{CLKL}	50	-	-	ns	
CLK H Level Time	t_{CLKH}	50	-	-	ns	
DI Setup Time	t_{sDI}	20	-	-	ns	
DI Hold Time	t_{hDI}	40	-	-	ns	
CSB Setup Time	t_{sCSB}	50	-	-	ns	
CSB Hold Time	t_{hCSB}	50	-	-	ns	
CSB H Level Time	t_{CSBH}	50	-	-	ns	
D/A Output Settling Time	t_{OUT}	-	-	100	μs	$C_L=50pF, R_L=10k\Omega$

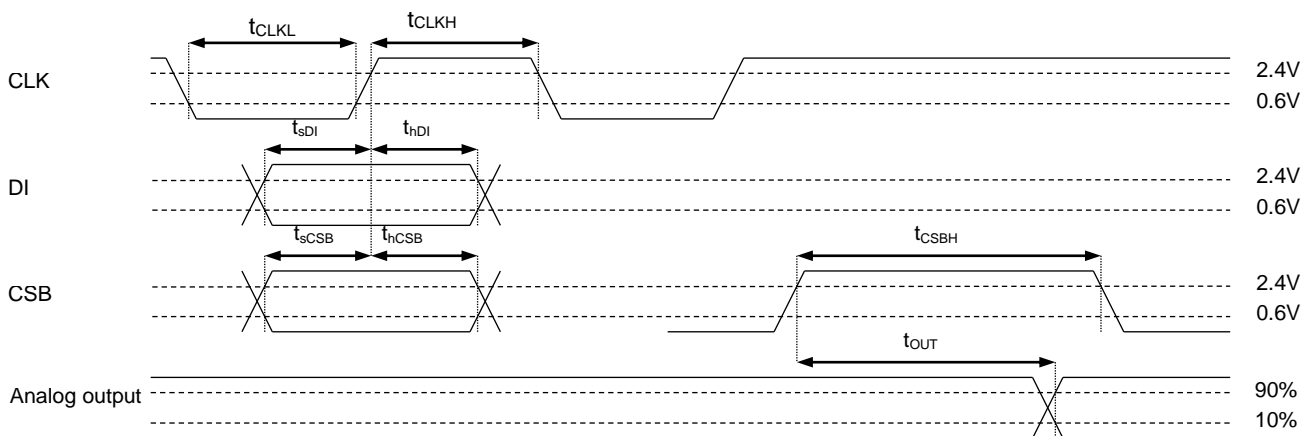


Figure 3

Typical Performance Curves

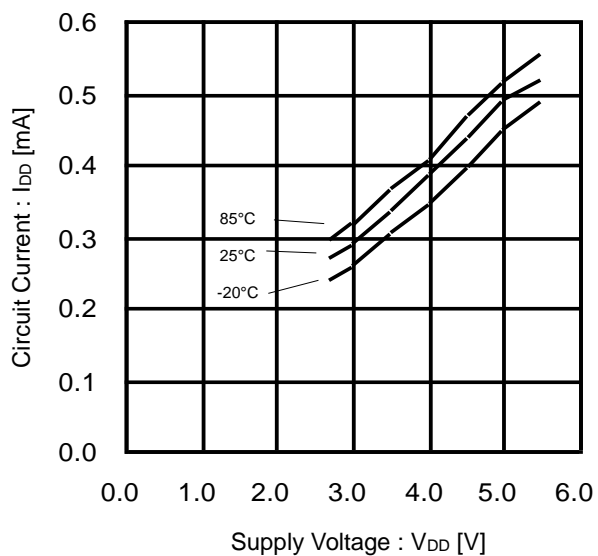


Figure 4. Circuit Current vs Supply Voltage (VDD Current Consumption)

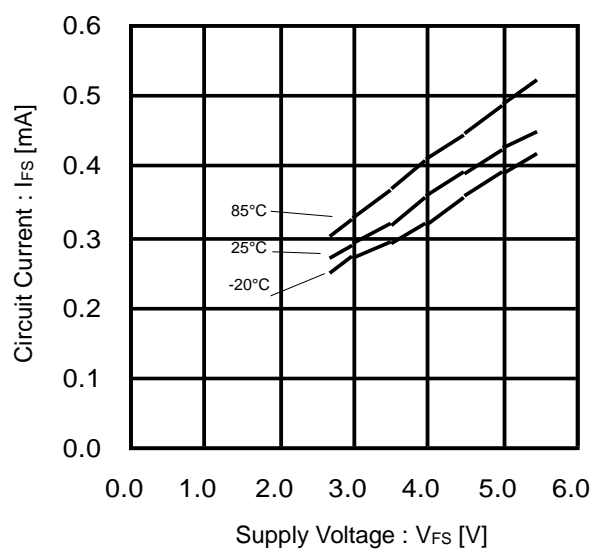


Figure 5. Circuit Current vs Supply Voltage (VFS Current Consumption)

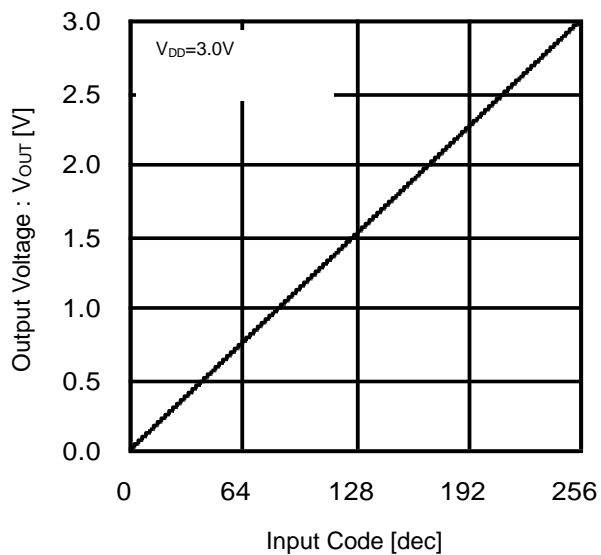


Figure 6. Output Voltage vs Input Code

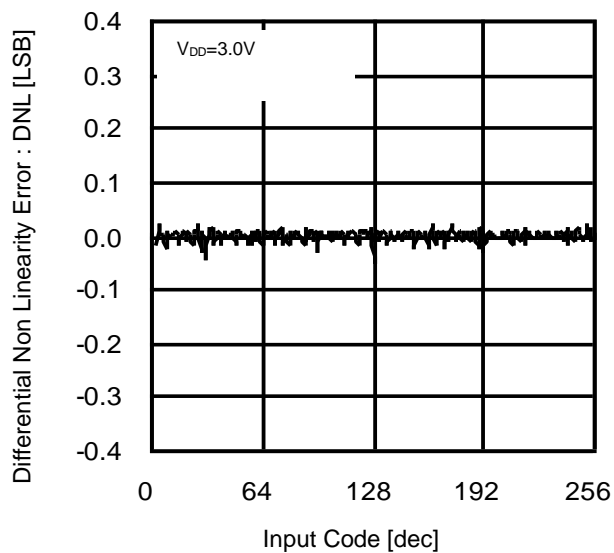


Figure 7. Differential Non Linearity Error vs Input Code

Typical Performance Curves – continued

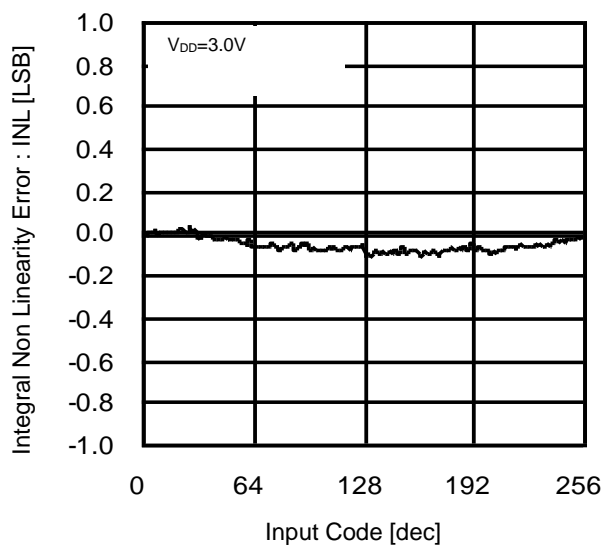


Figure 8. Integral Non Linearity Error vs Input Code

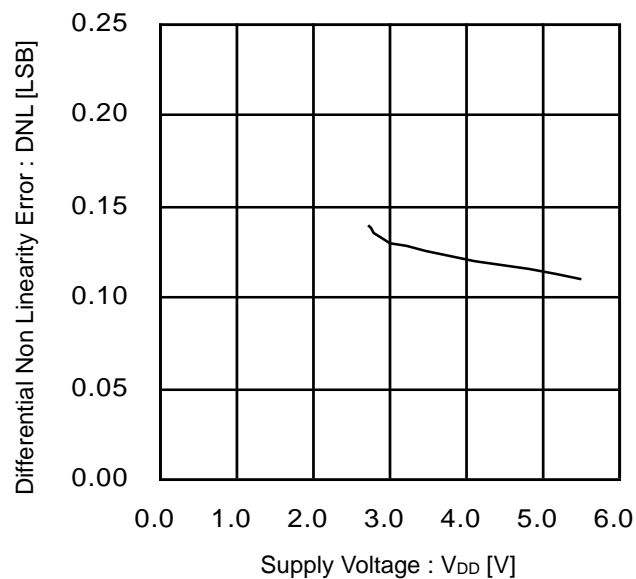


Figure 9. Differential Non Linearity Error vs Supply Voltage

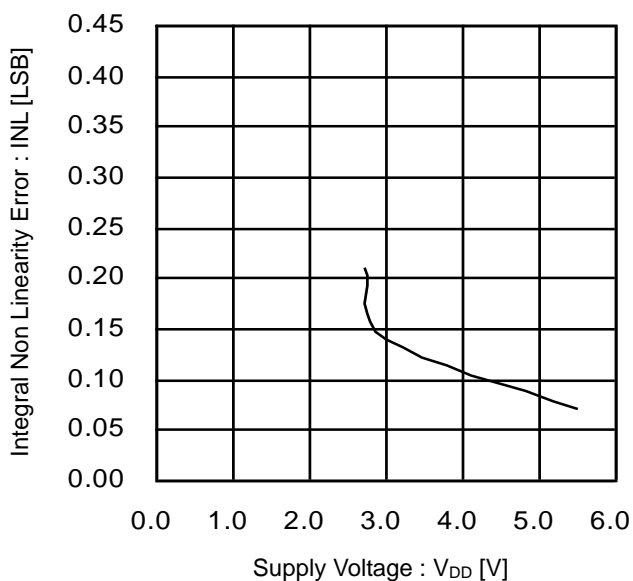


Figure 10. Integral Non Linearity Error vs Supply Voltage

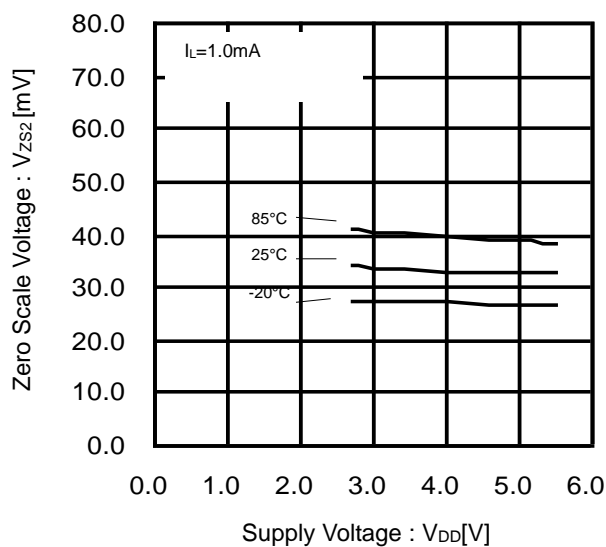


Figure 11. Output Zero Scale Voltage vs Supply Voltage

Typical Performance Curves – continued

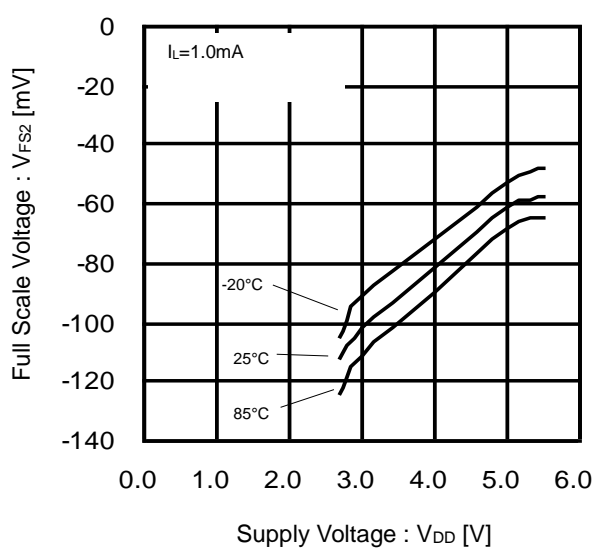


Figure 12. Output Full Scale Voltage vs Supply Voltage

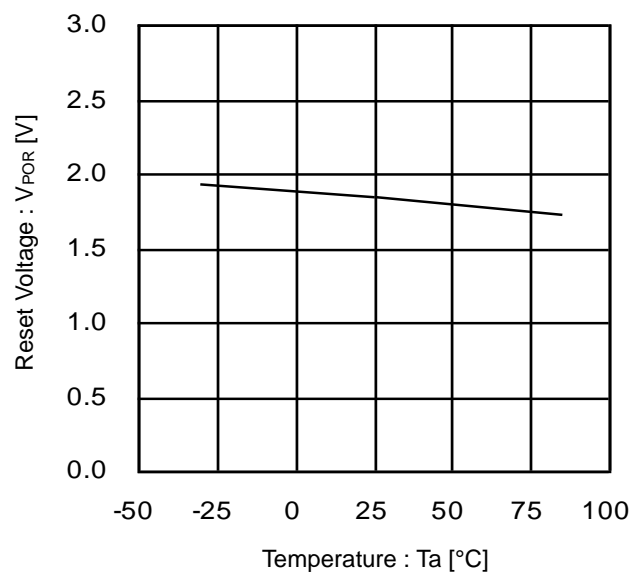


Figure 13. Reset Release Voltage vs Temperature

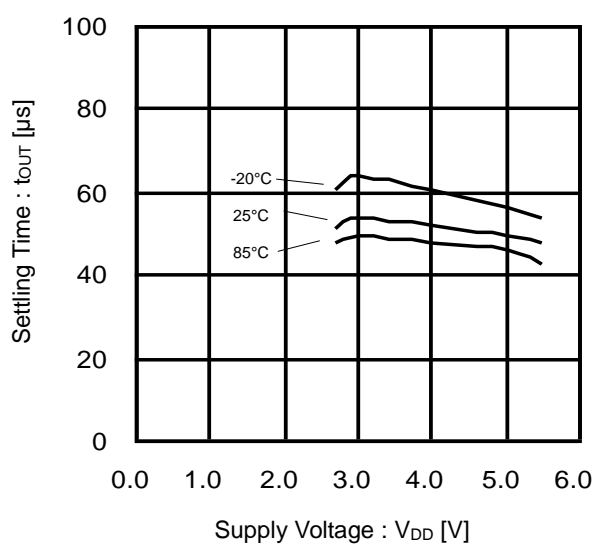


Figure 14. Settling Time vs Supply Voltage

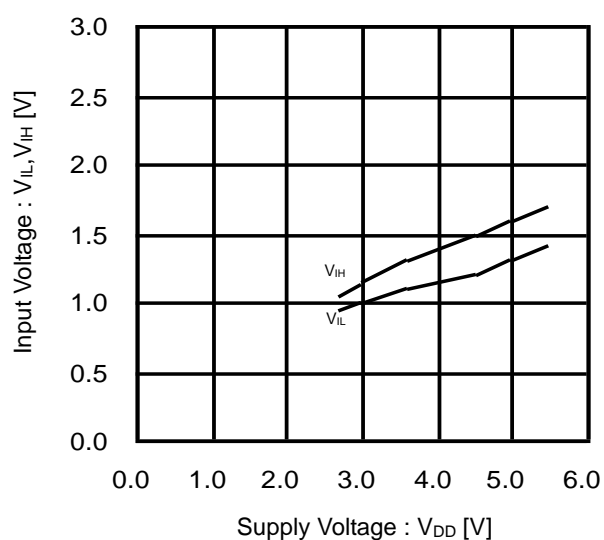


Figure 15. Input Voltage vs Supply Voltage

Application Information

Operation Description

The Serial Control Interface is 3-line serial interface 1) CSB, 2) CLK and 3) DI.

Every command is composed of 12 bits data sent through DI line (MSB first).

DI data is read every rising edge of the CLK while CSB is LOW.

Last 12 bits of data are latched when CSB goes HIGH.

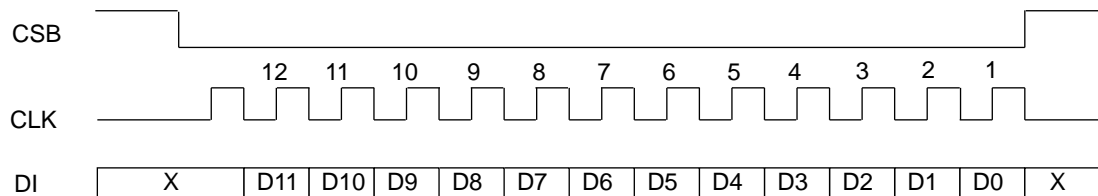


Figure 16

Data Settings

D0	D1	D2	D3	D4	D5	D6	D7	Setting
0	0	0	0	0	0	0	0	GND
1	0	0	0	0	0	0	0	(V _{DD} or V _{FS} -GND)/256x1
0	1	0	0	0	0	0	0	(V _{DD} or V _{FS} -GND)/256x2
1	1	0	0	0	0	0	0	(V _{DD} or V _{FS} -GND)/256x3
0	0	1	0	0	0	0	0	(V _{DD} or V _{FS} -GND)/256x4
...								
0	1	1	1	1	1	1	1	(V _{DD} or V _{FS} -GND)/256x254
1	1	1	1	1	1	1	1	(V _{DD} or V _{FS} -GND)/256x255

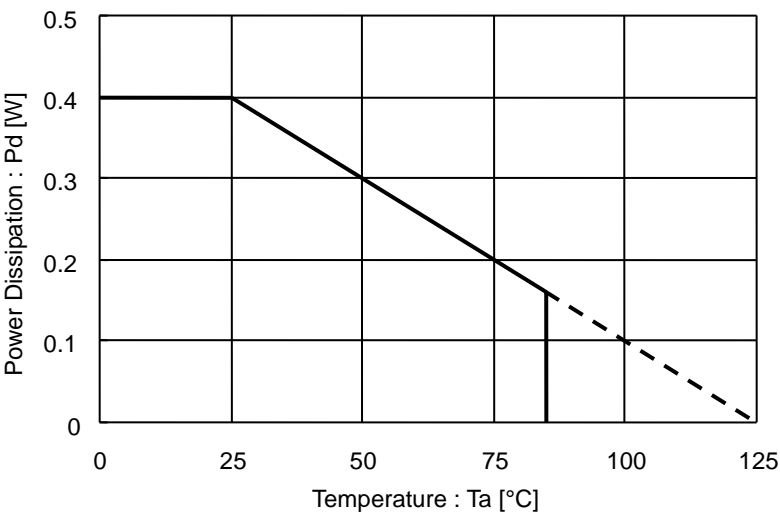
(Note) Initial status D[7:0]=00h

Channel Settings

D8	D9	D10	D11	BH2227FV	BH2228FV
0	0	0	0	Not used	Not used
0	0	0	1	AO1	AO1
0	0	1	0	AO2	AO2
0	0	1	1	Not used	AO3
0	1	0	0	Not used	AO4
0	1	0	1	AO3	AO5
0	1	1	0	AO4	AO6
0	1	1	1	Not used	Not used
1	0	0	0	Not used	Not used
1	0	0	1	Not used	Not used
1	0	1	0	Not used	Not used
1	0	1	1	Not used	Not used
1	1	0	0	Not used	Not used
1	1	0	1	Not used	Not used
1	1	1	0	Not used	Not used
1	1	1	1	Not used	Not used

Power Dissipation

· SSOP-B14



Board size : 70mm x 70mm x 1.6mm Material : FR4 glass epoxy board (copper foil area less than 3%)

I/O Equivalent Circuit

Terminal	Equivalent Circuit	Terminal	Equivalent Circuit
AO1 AO2 AO3 AO4 AO5 AO6		DI CLK CSB	

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

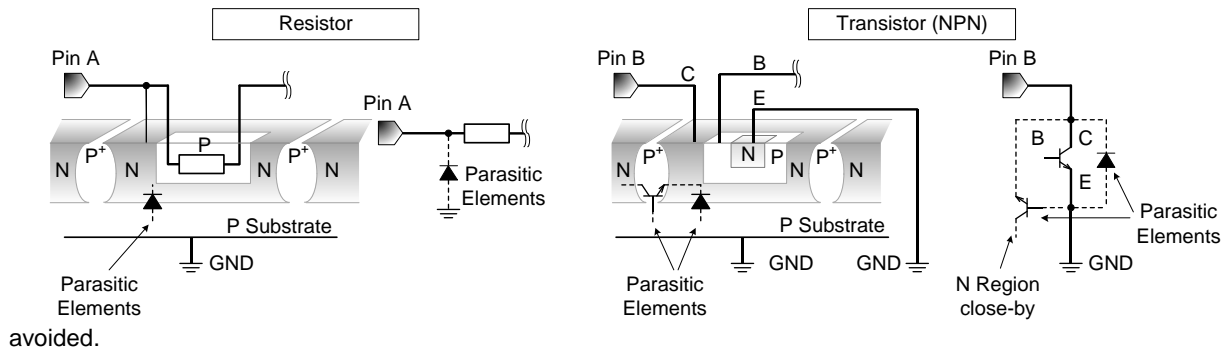


Figure 17. Example of monolithic IC structure

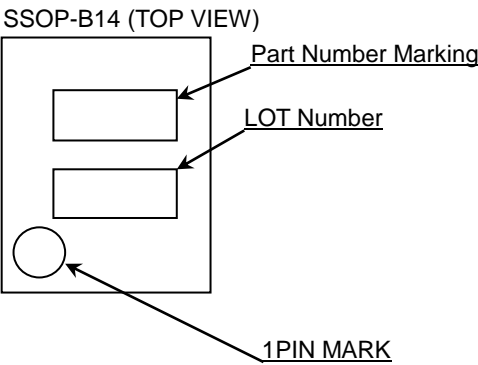
13. Reset Function

The power on reset circuit, which initializes internal settings, may malfunction during abrupt power ons. Therefore, set the time constant so as to satisfy the power source rise time.

Ordering Information

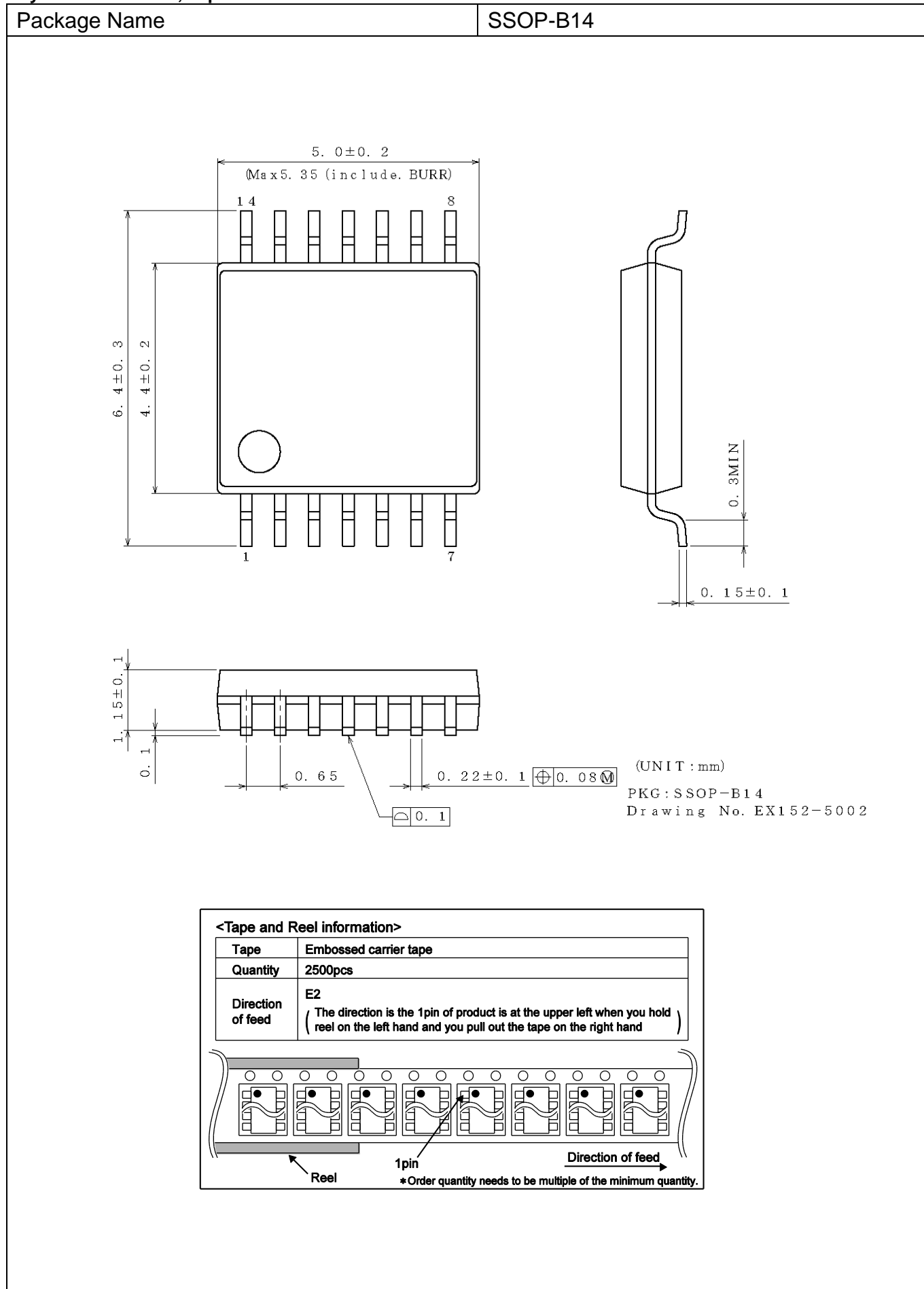
B H 2 2 2 x F V								-	E 2		
Part Number				Package				Packaging and forming specification			
2227				FV: SSOP-B14				E2: Embossed tape and reel			
2228											

Marking Diagram



Part Number	Part Number Marking
BH2227FV-E2	H2227
BH2228FV-E2	H2228

Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
06.Nov.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of the Products in places subject to dew condensation
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 - [d] the Products are exposed to high Electrostatic
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