2.7V to 5.5V Input, 2A Integrated MOSFET Single Synchronous Buck DC/DC Converter For Automotive

BD9S200MUF-C

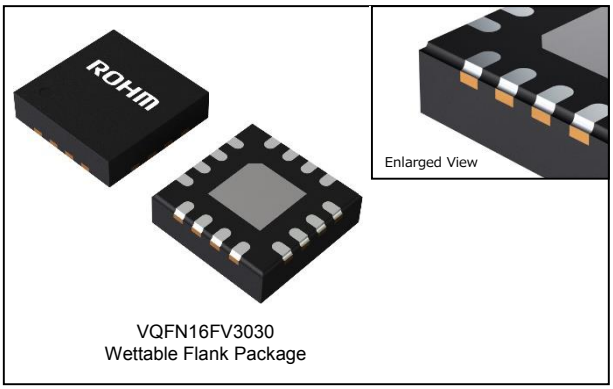
General Description

BD9S200MUF-C is a synchronous buck DC/DC Converter with built-in low On Resistance power MOSFETs. It is capable of providing current up to 2A. The SLLM™ control provides excellent efficiency characteristics in light-load conditions which make the product ideal for reducing standby power consumption of equipment. Small inductor is applicable due to high switching frequency of 2.2MHz. It is a current mode control DC/DC Converter and features high-speed transient response. Phase compensation can also be set easily.
It can also be synchronized to external pulse.

Key Specifications

- Input Voltage: 2.7V to 5.5V
- Output Voltage Setting: 0.8V to V_{PVIN} x 0.8V
- Output Current: 2A(Max)
- Switching Frequency: 2.2MHz(Typ)
- High Side MOSFET ON Resistance: 35mΩ (Typ)
- Low Side MOSFET ON Resistance: 35mΩ (Typ)
- Shutdown Circuit Current: 0μA (Typ)
- Operating Temperature: -40°C to +125°C

Package	W(Typ) x D(Typ) x H(Max)
VQFN16FV3030	3.00mm x 3.00mm x 1.00mm



VQFN16FV3030
Wettable Flank Package

Features

- SLLM™ (Simple Light Load Mode) Control
- AEC-Q100 Qualified(Note 1)
- Single Synchronous Buck DC/DC Converter
- Adjustable Soft Start Function
- Power Good Output
- Input Under Voltage Lockout Protection
- Short Circuit Protection
- Output Over Voltage Protection
- Over Current Protection
- Thermal Shutdown Protection
- Wettable Flank QFN Package

(Note 1) Grade 1

Applications

- Automotive Equipment
  (Cluster Panel, Infotainment Systems)
- Other Electronic Equipment

Typical Application Circuit

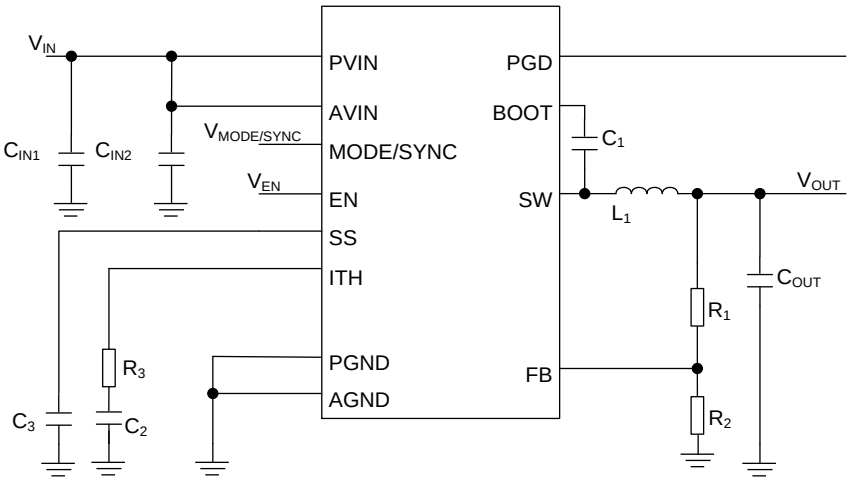


Figure 1. Application Circuit

SLLM™ is a trademark of ROHM Co., Ltd.

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

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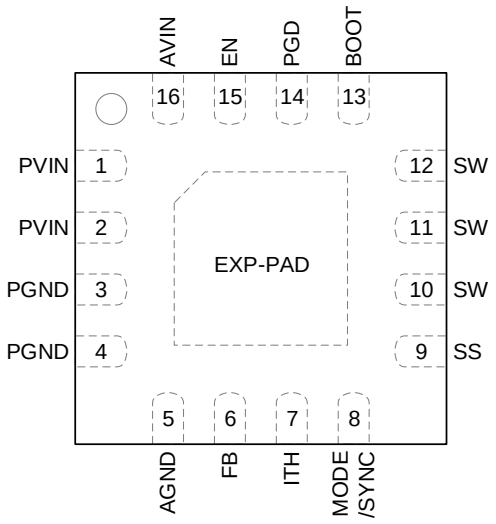
Pin Configuration



(TOP VIEW)

Figure 2. Pin Configuration

Pin Descriptions

Pin No.	Pin Name	Function
1, 2	PVIN	Power supply pins for the DC/DC Converter. Connecting a 10µF ceramic capacitor is recommended.
3, 4	PGND	Ground pins for the DC/DC Converter.
5	AGND	Ground pin.
6	FB	V_{OUT} voltage feedback pin. An inverting input node for the gm error amplifier. Connect output voltage divider to this pin to set the output voltage. See page 17 on how to compute for the resistor values.
7	ITH	An output pin of the gm error amplifier and the input of PWM comparator. Connect phase compensation components to this pin. See page 20 on calculate the resistance and capacitance of phase compensation.
8	MODE /SYNC	Pin for selecting the SLLM™ control mode and the Forced PWM mode. Turning this pin signal Low forces the device to operate in the Forced PWM mode. Turning this pin signal High enables the SLLM™ control and the mode is automatically switched between the SLLM™ control and PWM mode according to the load current. In addition, external synchronization operation is started by inputting synchronous pulse signal to this pin.
9	SS	Pin for setting the soft start time. The rise time of the output voltage can be specified by connecting a capacitor to this pin. See page 19 on calculate the capacitance.
10, 11, 12	SW	Switch pin. These pins are connected to the source of the High Side MOSFET and drain of the Low Side MOSFET. Connect a bootstrap capacitor of 0.1µF between these pins and the BOOT pin.
13	BOOT	Connect a bootstrap capacitor of 0.1µF between this pin and the SW pins. The voltage of this capacitor is the gate drive voltage of the High Side MOSFET.
14	PGD	Power Good pin, an open drain output. Use of pull up resistor is needed. See page 12 on setting the resistance.
15	EN	Pin for controlling the device. Turning this pin signal Low forces the device to enter the shutdown mode. Turning this pin signal High enables the device.
16	AVIN	Power supply input pin of the analog circuitry. Connect this pin to PVIN. Connecting a 0.1µF ceramic capacitor is recommended.
-	EXP-PAD	A backside heat dissipation pad. Connecting to the internal PCB ground plane by using via provides excellent heat dissipation characteristics.

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Block Diagram

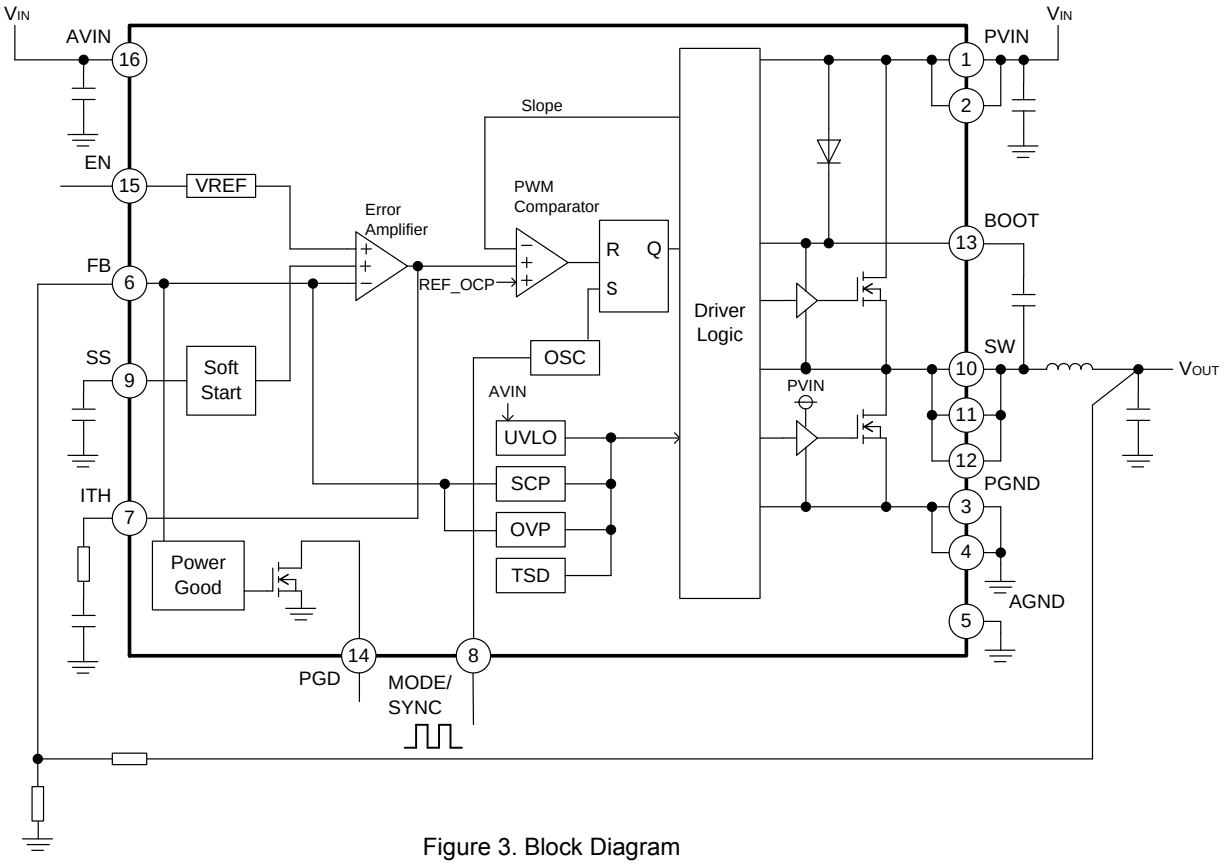

Figure 3. Block Diagram

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Description of Blocks

1. VREF
   The VREF block generates the internal reference voltage.

2. UVLO (Under Voltage Lockout)
   The UVLO block is for under voltage lockout protection. It will shutdown the device when the V_{IN} falls to 2.45V(Typ) or lower. The threshold voltage has a hysteresis of 100mV(Typ).

3. SCP (Short Circuit Protection)
   This is the short circuit protection circuit. After soft start is judged to be completed, if the FB pin voltage falls to 0.56V(Typ) or less and remain in that state for 1ms(Typ), output MOSFET will turn OFF for 14ms(Typ) and then restart the operation.

4. OVP (Over Voltage Protection)
   This is the output over voltage protection circuit. When the FB pin voltage becomes 0.880V(Typ) or more, it turns the output MOSFET OFF. After output voltage falls 0.856V(Typ) or less, the output MOSFET returns to normal operation.

5. TSD (Thermal Shutdown)
   This is the thermal shutdown circuit. It will shutdown the device when the junction temperature (Tj) reaches to 175°C(Typ) or more. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation with hysteresis of 25°C(Typ).

6. OCP (Over Current Protection)
   The Over Current Protection function operates by limiting the current that flows through High Side MOSFET at each cycle of the switching frequency.

7. Soft Start
   The Soft Start circuit slows down the rise of output voltage during startup, which allows the prevention of output voltage overshoot. The soft start time of the output voltage can be specified by connecting a capacitor to the SS pin. See page 19 on calculate the capacitance. A built-in soft start function is provided and a soft start is initiated in 1ms(Typ) when the SS pin is open.

8. Error Amplifier
   The Error Amplifier block is an error amplifier and its inputs are the reference voltage 0.8V(Typ) and the FB pin voltage. Phase compensation can be set by connecting a resistor and a capacitor to the ITH pin. See page 20 on calculate the resistance and capacitance of phase compensation.

9. PWM Comparator
   The PWM Comparator block compares the output voltage of the Error Amplifier and the Slope signal to determine the switching duty.

10. OSC (Oscillator)
    This block generates the oscillating frequency.

11. Driver Logic
    This block controls switching operation and various protection functions.

12. Power Good
    When the FB pin voltage reaches 0.8V(Typ) within ±7%, the built-in Nch MOSFET turns OFF and the PGD output turns high. In addition, the PGD output turns low when the FB pin voltage reaches outside ±10% of 0.8V(Typ).

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Input Voltage	V_{PVIN}, V_{AVIN}	-0.3 to +7	V
EN Voltage	V_{EN}	-0.3 to V_{AVIN}	V
MODE / SYNC Voltage	$V_{MODE/SYNC}$	-0.3 to V_{AVIN}	V
PGD Voltage	V_{PGD}	-0.3 to +7	V
BOOT Voltage	V_{BOOT}	-0.3 to +14	V
Voltage from SW to BOOT	ΔV_{BOOT}	-0.3 to +7	V
FB ITH SS Voltage	V_{FB}, V_{ITH}, V_{SS}	-0.3 to V_{AVIN}	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance*(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
VQFN16FV3030				
Junction to Ambient	θ_{JA}	189.0	57.5	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	23	10	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via*(Note 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{PVIN}, V_{AVIN}	2.7	5.5	V
Operating Temperature	Topr	-40	+125	°C
Output Current	I_{OUT}	-	2	A
Output Voltage Setting	V_{OUT}	0.8(Note 1)	V_{PVIN} x 0.8	V
SW Minimum ON Time	t_{ON_MIN}	-	95	ns
External Clock Frequency	f_{SYNC}	1.8	2.4	MHz
Synchronous Operation Input Duty	D_{SYNC}	25	75	%

(Note 1) Although the output voltage is configurable at 0.8V and higher, it may be limited by the SW min ON pulse width. For the configurable range, please refer to the Output Voltage Setting in Selection of Components Externally Connected.

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Electrical Characteristics (Unless otherwise specified Ta=-40°C to +125°C, AVIN=PVIN=5V, EN=5V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
AVIN						
Shutdown Circuit Current	I_{SDN}	-	0	10	µA	V_{EN}=0V, Ta=25°C
Circuit Current	I_{CC}	400	650	900	µA	I_{OUT}=0mA Non-switching, Ta=25°C
UVLO Detection Voltage	V_{UVLO1}	2.30	2.45	2.60	V	V_{AVIN} Falling
UVLO Release Voltage	V_{UVLO2}	2.40	2.55	2.70	V	V_{AVIN} Rising
UVLO Hysteresis Voltage	$V_{UVLO-HYS}$	50	100	125	mV	Ta=25°C
ENABLE						
EN Threshold Voltage High	V_{ENH}	2.0	-	V_{IN}	V	
EN Threshold Voltage Low	V_{ENL}	GND	-	0.8	V	
EN Input Current	I_{EN}	2	5	8	µA	V_{EN}=5V, Ta=25°C
MODE/SYNC						
MODE/SYNC Threshold Voltage High	$V_{MODESYNCH}$	2.0	-	V_{IN}	V	
MODE/SYNC Threshold Voltage Low	$V_{MODESYNCL}$	GND	-	0.8	V	
MODE/SYNC Input Current	$I_{MODESYNC}$	4	10	16	µA	$V_{MODESYNC}$=5V, Ta=25°C
Reference Voltage, Error Amplifier						
FB Pin Voltage	V_{FB}	0.788	0.8	0.812	V	
FB Input Current	I_{FB}	-	0	0.2	µA	V_{FB}=0.8V, Ta=25°C
ITH Sink Current	I_{ITHSI}	12	19	25	µA	V_{FB}=0.9V, Ta=25°C
ITH Source Current	I_{ITHSO}	-25	-19	-12	µA	V_{FB}=0.7V, Ta=25°C
Soft Start Time	t_{SS}	0.5	1.0	2.0	ms	V_{AVIN}=5V, The SS Pin OPEN
		0.6	1.2	2.4	ms	V_{AVIN}=3.3V, The SS Pin OPEN
SS Charge Current	I_{SS}	-2.34	-1.8	-1.26	µA	
Switching Frequency						
Switching Frequency	f_{SW}	2.0	2.2	2.4	MHz	
Power Good						
PGD Falling (Fault) Voltage	V_{PGDTH_FF}	V_{FB} x 0.87	V_{FB} x 0.90	V_{FB} x 0.93	V	V_{FB} Falling
PGD Rising (Good) Voltage	V_{PGDTH_RG}	V_{FB} x 0.90	V_{FB} x 0.93	V_{FB} x 0.96	V	V_{FB} Rising
PGD Rising (Fault) Voltage	V_{PGDTH_RF}	V_{FB} x 1.07	V_{FB} x 1.10	V_{FB} x 1.13	V	V_{FB} Rising
PGD Falling (Good) Voltage	V_{PGDTH_FG}	V_{FB} x 1.04	V_{FB} x 1.07	V_{FB} x 1.10	V	V_{FB} Falling
PGD Output Leakage Current	$I_{LEAKPGD}$	-	0	2	µA	V_{PGD}=5V, Ta=25°C
PGD FET ON Resistance	R_{PGD}	10	30	60	Ω	
PGD Output Low Level Voltage	V_{PGDL}	0.01	0.03	0.06	V	I_{PGD}=1mA
Switch MOSFET						
High Side FET ON Resistance	R_{ONH}	10	35	60	mΩ	V_{PVIN}=5V
		15	38	65	mΩ	V_{PVIN}=3.3V
Low Side FET ON Resistance	R_{ONL}	10	35	60	mΩ	V_{PVIN}=5V
		15	38	65	mΩ	V_{PVIN}=3.3V
High Side FET Leakage Current	$I_{LEAKSWH}$	-	0	5	µA	V_{PVIN}=5.5V, V_{SW}=0V Ta=25˚C
Low Side FET Leakage Current	$I_{LEAKSWL}$	-	0	5	µA	V_{PVIN}=5.5V, V_{SW}=5.5V Ta=25˚C
SW Current of Over Current Protection*(Note1)*	I_{OCP}	2.8	4.0	5.5	A	
SCP, OVP						
Short Circuit Protection Detection Voltage	V_{SCP}	0.45	0.56	0.67	V	
Output Over Voltage Protection Detection Voltage	V_{OVP}	0.856	0.880	0.904	V	

(Note 1) This is design value. Not production tested.

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Typical Performance Curves

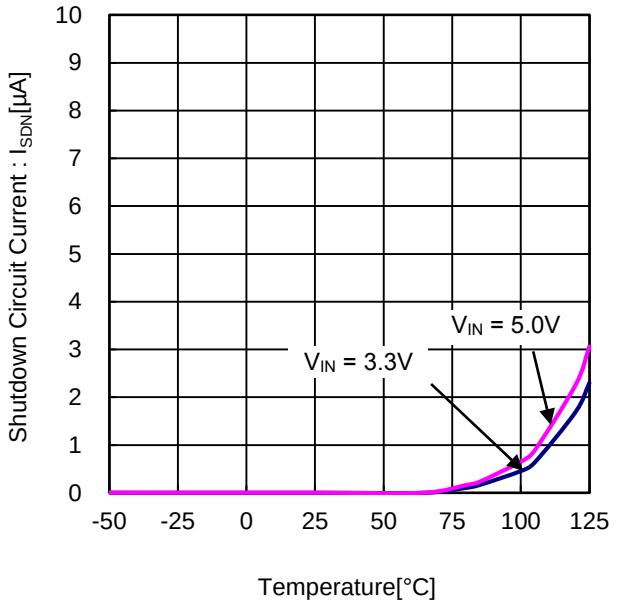

Figure 4. Shutdown Circuit Current vs Temperature

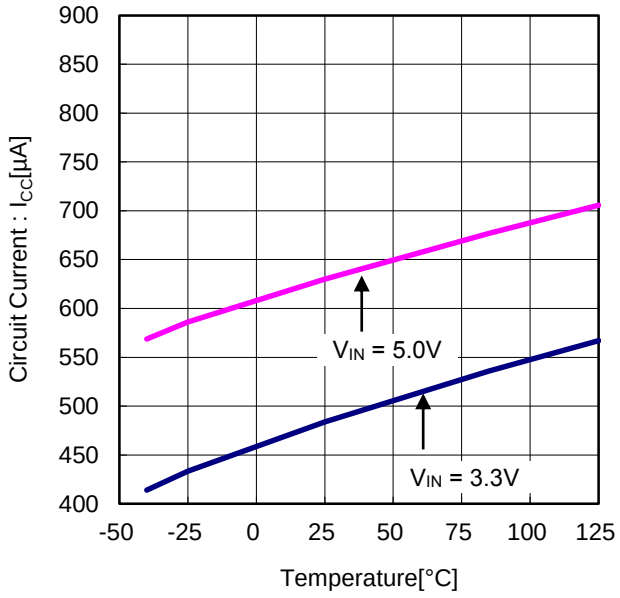

Figure 5. Circuit Current vs Temperature

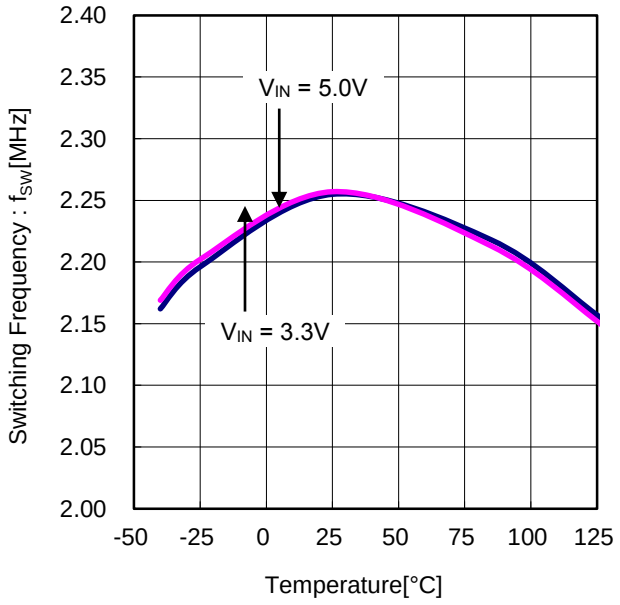

Figure 6. Switching Frequency vs Temperature

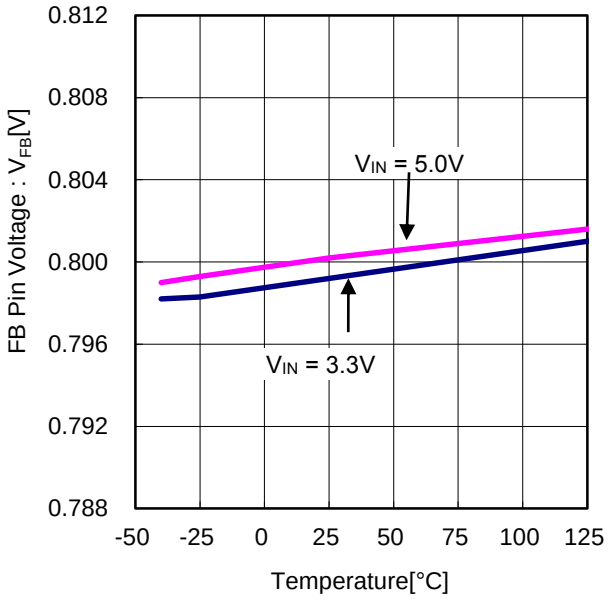

Figure 7. FB Pin Voltage vs Temperature

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Typical Performance Curves – continued

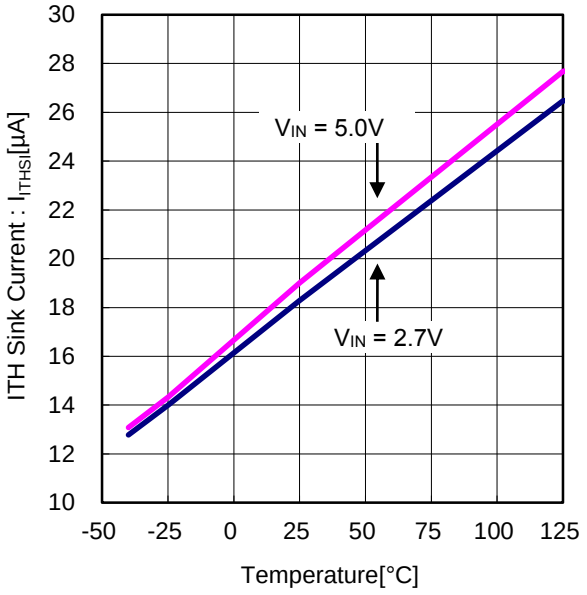

Figure 8. ITH Sink Current vs Temperature

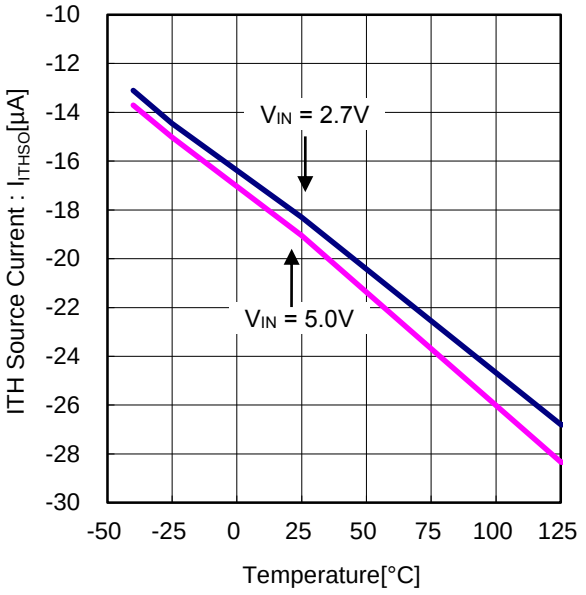

Figure 9. ITH Source Current vs Temperature

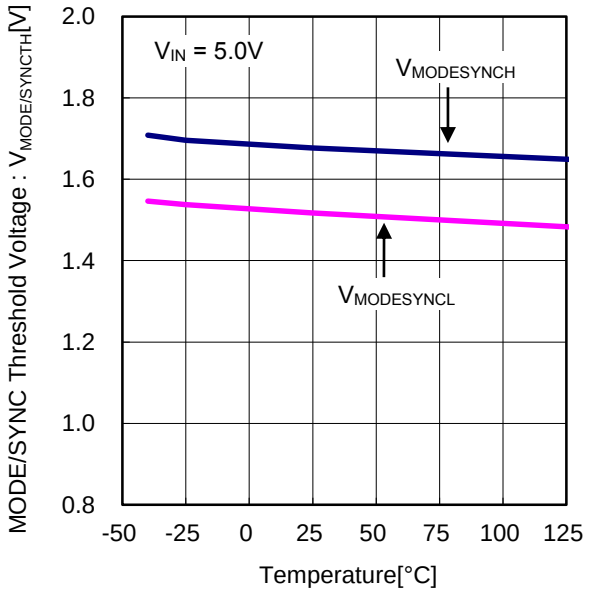

Figure 10. MODE/SYNC Threshold Voltage vs Temperature

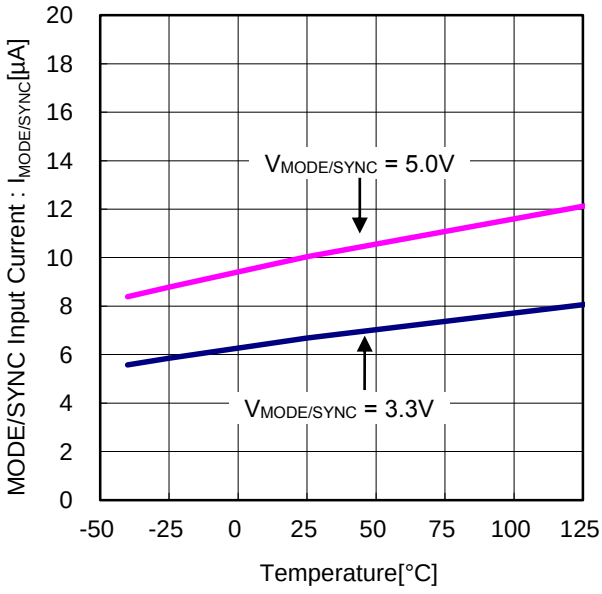

Figure 11. MODE/SYNC Input Current vs Temperature

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Typical Performance Curves – continued

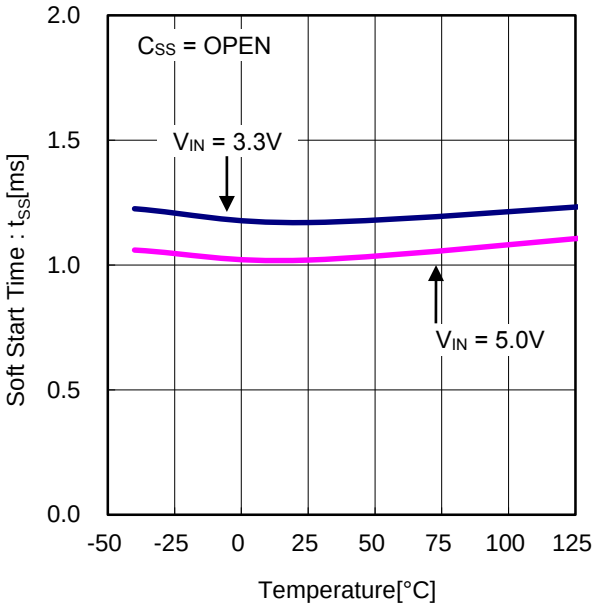

Figure 12. Soft Start Time vs Temperature

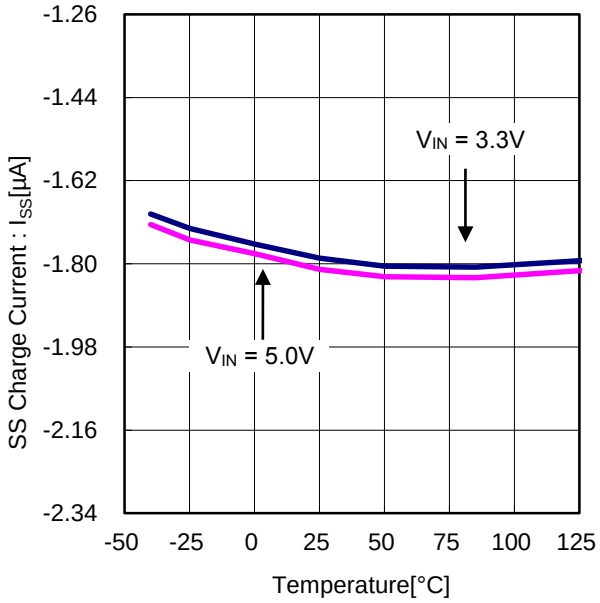

Figure 13. SS Charge Current vs Temperature

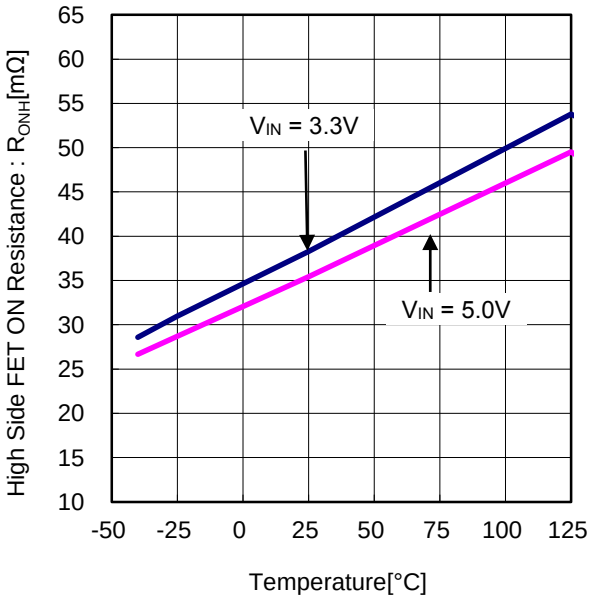

Figure 14. High Side FET ON Resistance vs Temperature

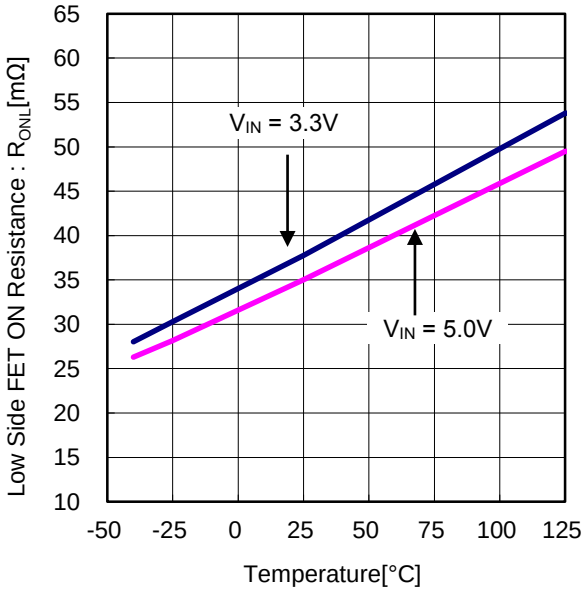

Figure 15. Low Side FET ON Resistance vs Temperature

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Typical Performance Curves – continued

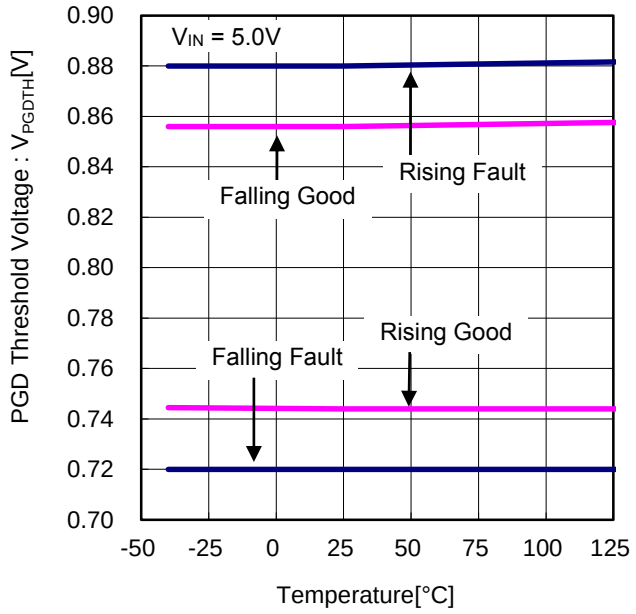

Figure 16. PGD Threshold Voltage vs Temperature

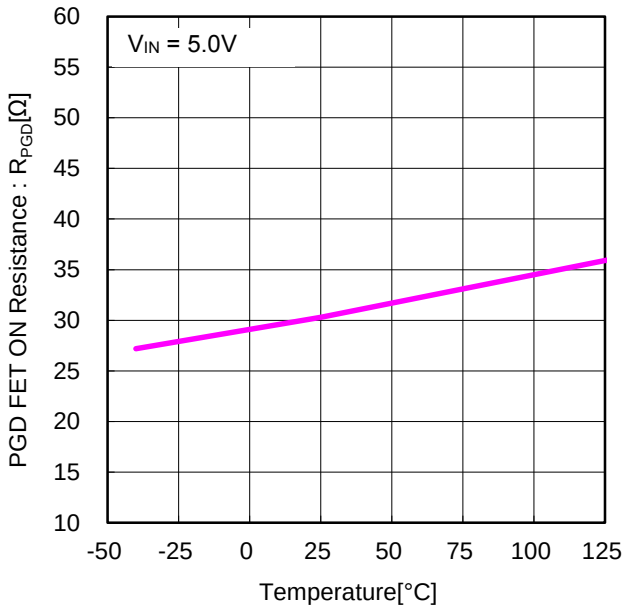

Figure 17. PGD FET ON Resistance vs Temperature

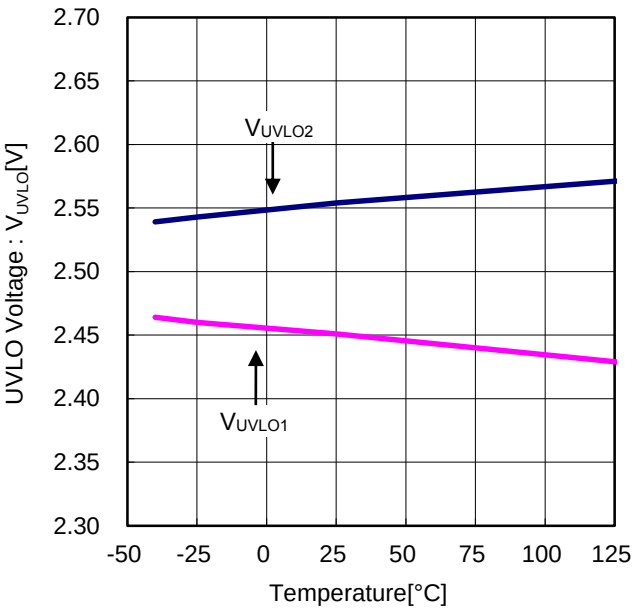

Figure 18. UVLO Voltage vs Temperature

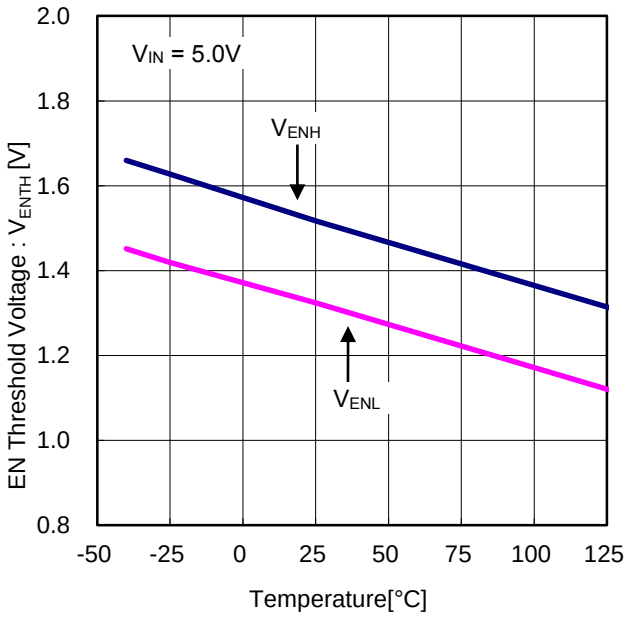

Figure 19. EN Threshold Voltage vs Temperature

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Typical Performance Curves – continued

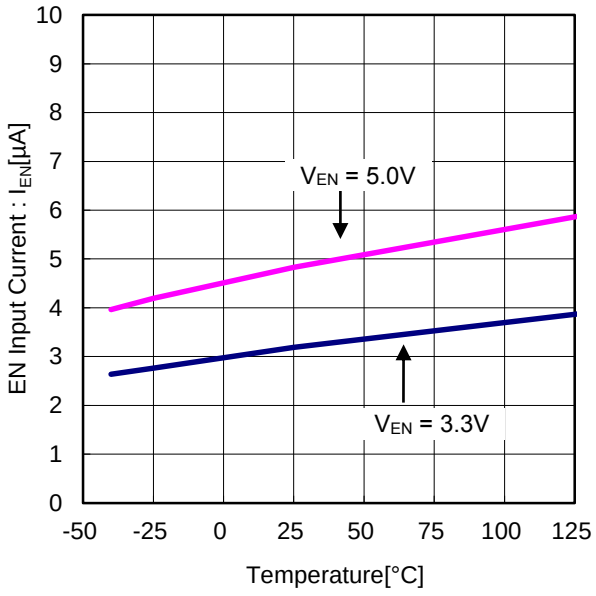

Figure 20. EN Input Current vs Temperature

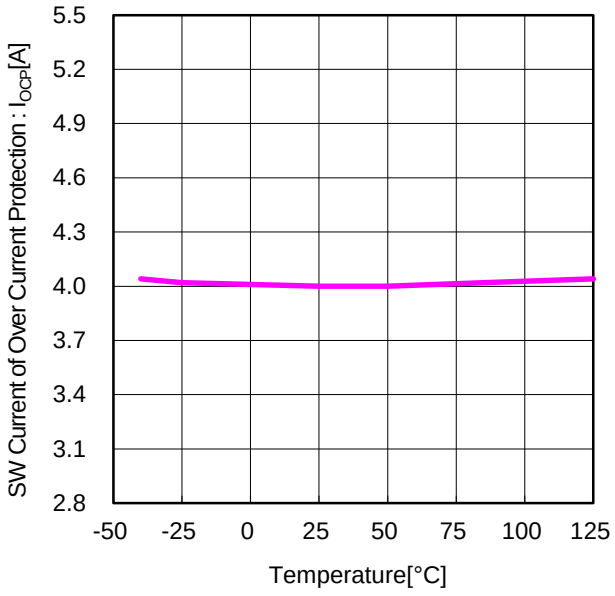

Figure 21 SW Current of Over Current Protection vs Temperature

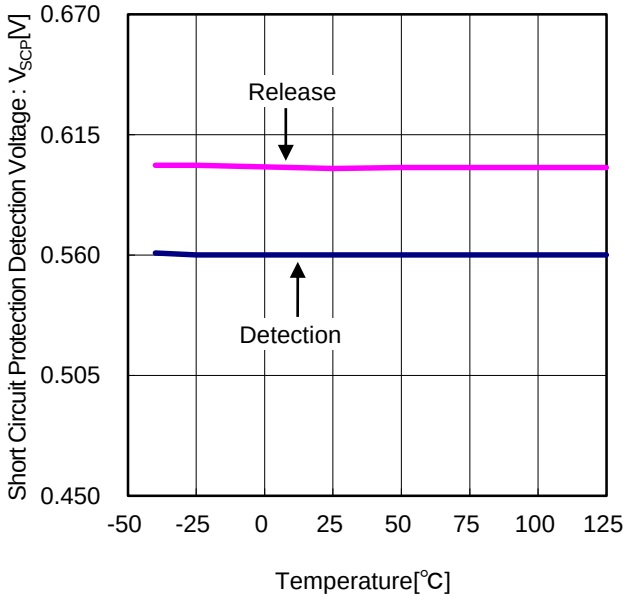

Figure 22. Short Circuit Protection Detection Voltage vs Temperature

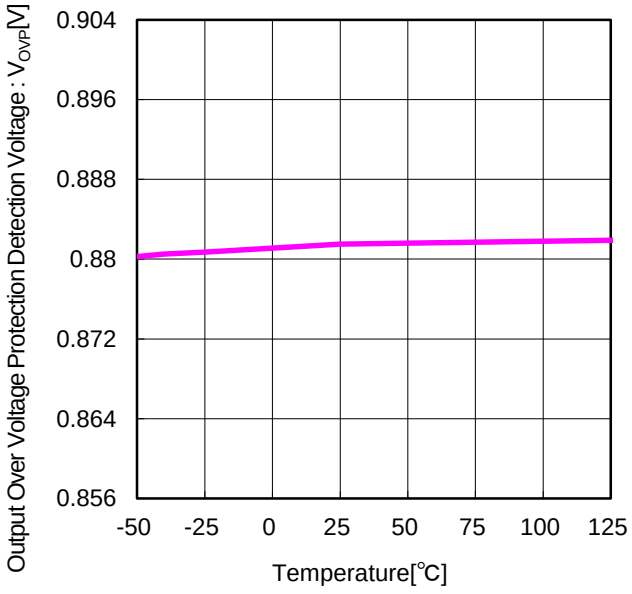

Figure 23. Output Over Voltage Protection Detection Voltage vs Temperature

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Function Explanations

1. Enable Control

The device shutdown can be controlled by the voltage applied to the EN pin. When V_{EN} becomes 2.0V or more, the internal circuit is activated and the device starts up with soft start. When V_{EN} becomes 0.8V or less, the device will be shutdown.

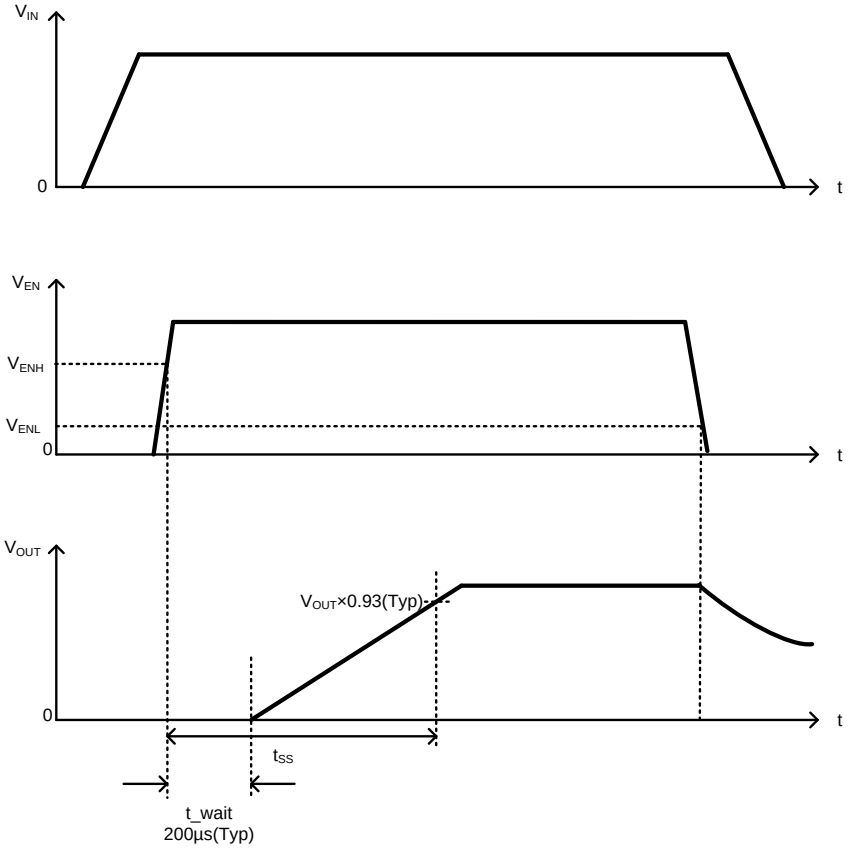

Figure 24. Enable ON/OFF Timing Chart

2. Power Good Function

When the FB pin voltage reaches 0.8V(Typ) within ±7%, the PGD pin open drain MOSFET turns OFF and the output turns high. In addition, when the FB pin voltage reaches outside ±10% of 0.8V(Typ), the PGD pin open drain MOSFET turns ON and the PGD pin is pulled down with impedance of 30Ω(Typ). It is recommended to use a pull-up resistor of about 10kΩ to 100kΩ for the power source.

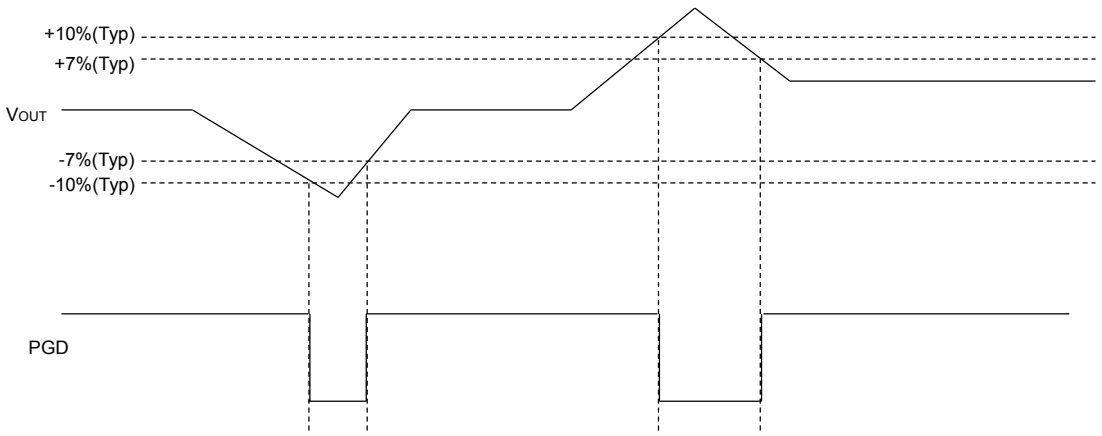

Figure 25. Power Good Timing Chart

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Function Explanations – continued

3. External Synchronization Function

By inputting synchronous pulse signal to the MODE/SYNC pin, the switching frequency can be synchronized to external synchronous pulse signal. When pulse signal is applied at a frequency of 1.8MHz or higher, the external synchronization operation is started after the falls of the synchronous pulse are detected 7 times.
Input the signal with the synchronization frequency range between 1.8MHz and 2.4MHz and the duty range between 25% and 75%.
Please note that the output voltage fluctuates by about 2% for a moment when switching between the synchronized operation to external signal and internal CLK frequency.

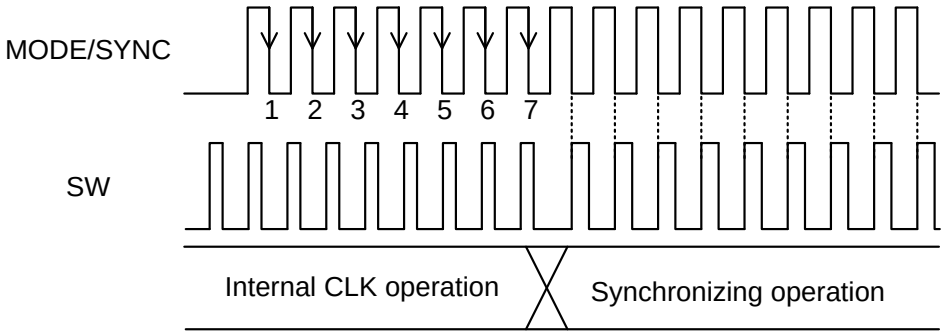

Figure 26. External Synchronization Function Timing Chart

When using the external synchronization function, connect a capacitor of 10pF in parallel to the phase compensation components (resistor and capacitor) connected to the ITH pin, as a countermeasure against the interference to the ITH pin of the Error Amplifier output.

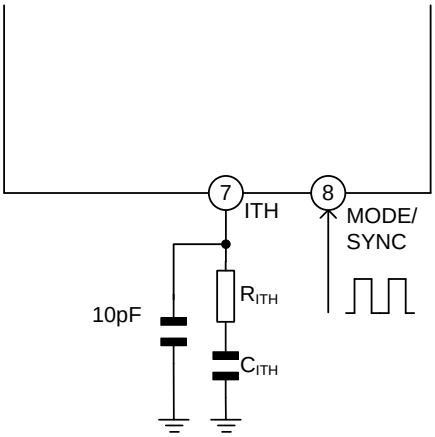

Figure 27. Recommended Circuit When Using External Synchronization Function

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Function Explanations – continued

4. SLLM™ Control and Forced PWM Control

SLLM™(Simple Light Load Mode) is a technology that enables the OFF control of switching pulses while operating with Pulse Width Modulation(PWM) control loop under light load condition. Therefore, it allows the linear operation without excessive voltage drop or deterioration in transient response during the switching from light load to heavy load or vice versa.

By utilizing this technology, BD9S200MUF-C operates in PWM mode switching under heavy load condition and automatically switches to SLLM™ control under light load condition in order to improve the efficiency. By keeping the MODE/SYNC pin voltage level 0.8V or less, it forces the device to operate with Forced PWM mode. And, by applying 2.0V or more to MODE/SYNC pin, it allows the device to operate with SLLM™ control. As for the Forced PWM mode, it has lower efficiency compared to SLLM™ control under light load condition. However, since the device operates with a constant switching frequency under varying load conditions, the countermeasure against noise is relatively easier.

Please note that SLLM™ does not operate adequately when the switching Duty is 50% or more.

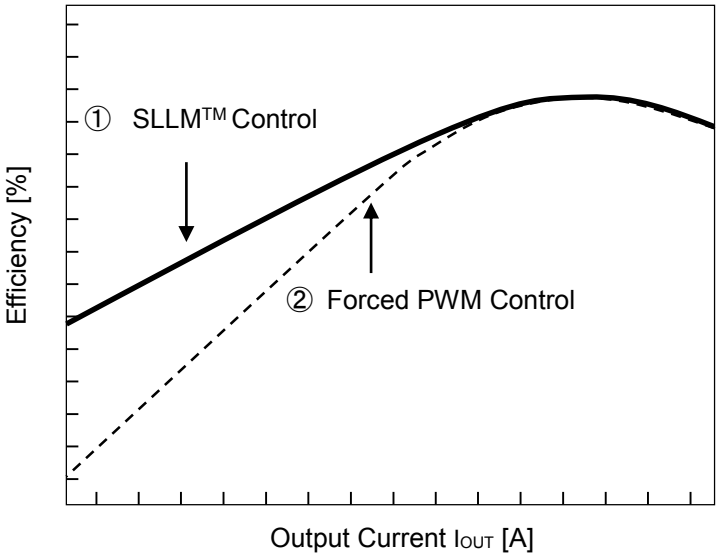

Figure 28. Efficiency (SLLM™ Control and Forced PWM Control)

① SLLM™ Control

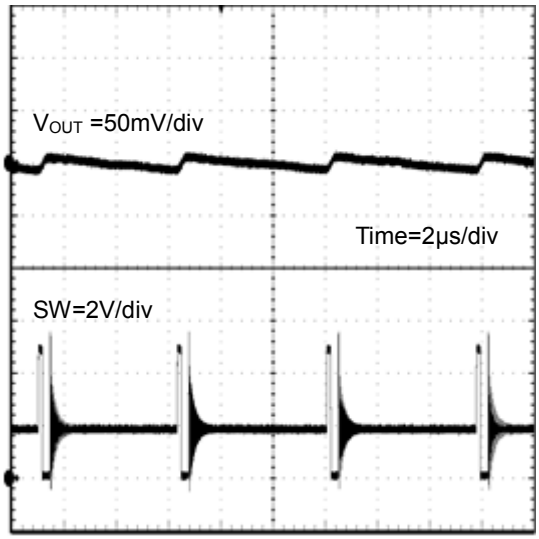

Figure 29. SW Waveform (SLLM™ Control)
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=50mA)

② Forced PWM Control

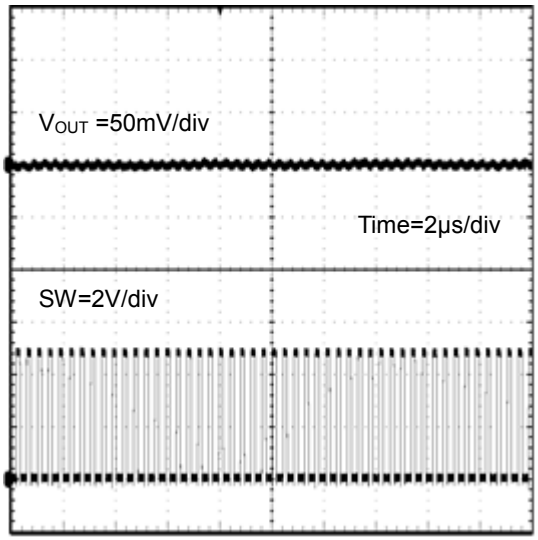

Figure 30. SW Waveform (Forced PWM Control)
(V_{IN}=5.0V, V_{OUT}=1.8V, I_{OUT}=1A)

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Protection

1. Short Circuit Protection (SCP)

The Short Circuit Protection block compares the FB pin voltage with the internal reference voltage VREF. When the FB pin voltage has fallen to 0.56V(Typ) or less and remained there for 1ms(Typ), SCP stops the operation for 14ms(Typ) and subsequently initiates a restart. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

The EN Pin	The FB Pin	Short Circuit Protection	Short Circuit Protection Operation
2.0V or higher	≤0.56V(Typ)	Enabled	ON
	≥0.60V(Typ)		OFF
0.8V or lower	-	Disabled	OFF

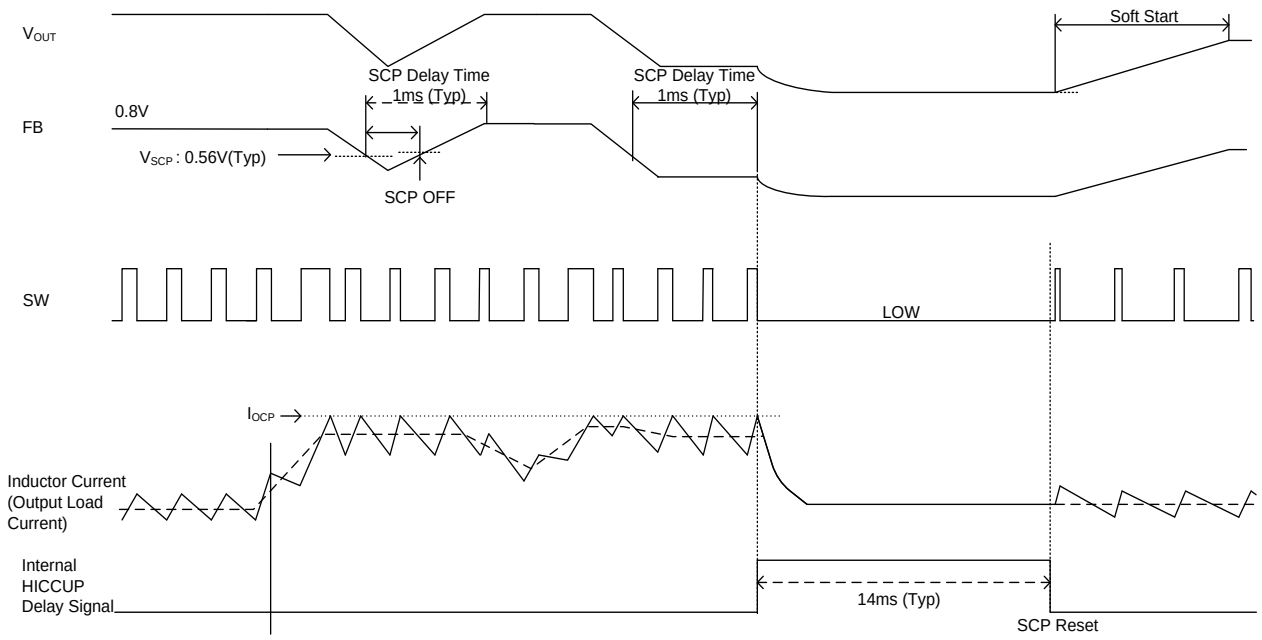

Figure 31. Short Circuit Protection (SCP) Timing Chart

2. Over Current Protection (OCP)

The Over Current Protection function operates by limiting the current that flows through High Side MOSFET at each cycle of the switching frequency. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the device should not be used in applications characterized by continuous operation of the protection circuit (e.g. when a load that significantly exceeds the output current capability of the chip is connected).

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Protection – continued

3. Under Voltage Lockout Protection (UVLO)

It will shutdown the device when the AVIN pin falls to 2.45V(Typ) or lower.
The threshold voltage has a hysteresis of 100mV(Typ).

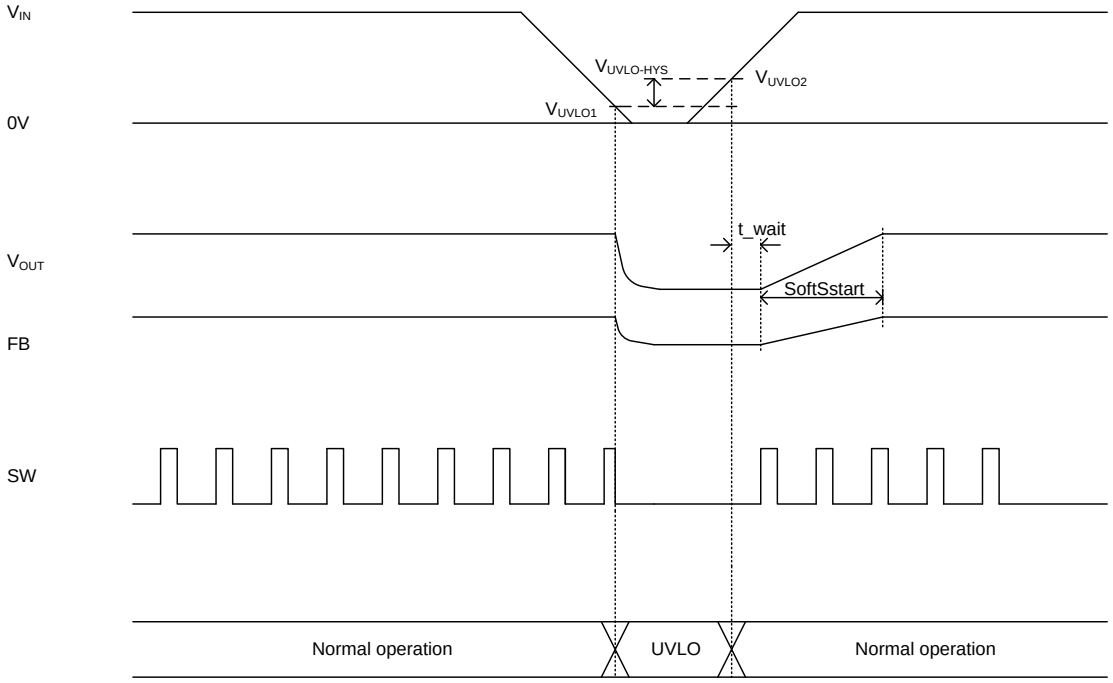

Figure 32. UVLO Timing Chart

4. Thermal Shutdown

This is the thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. However, if the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit[Tj ≥175°C (Typ)] that will turn OFF output MOSFET. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation. Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

5. Over Voltage Protection (OVP)

The device incorporates an over voltage protection circuit to minimize the output voltage overshoot when recovering from strong load transients or output fault conditions. If the FB pin voltage exceeds Output Over Voltage Protection Detection Voltage at 0.880V(Typ), the MOSFET on the output stage is turned OFF to prevent the increase in the output voltage. After the detection, the switching operation resumes if the output decreases and the over voltage state is released. Output Over Voltage Protection Detection Voltage and release voltage have a hysteresis of 3%.

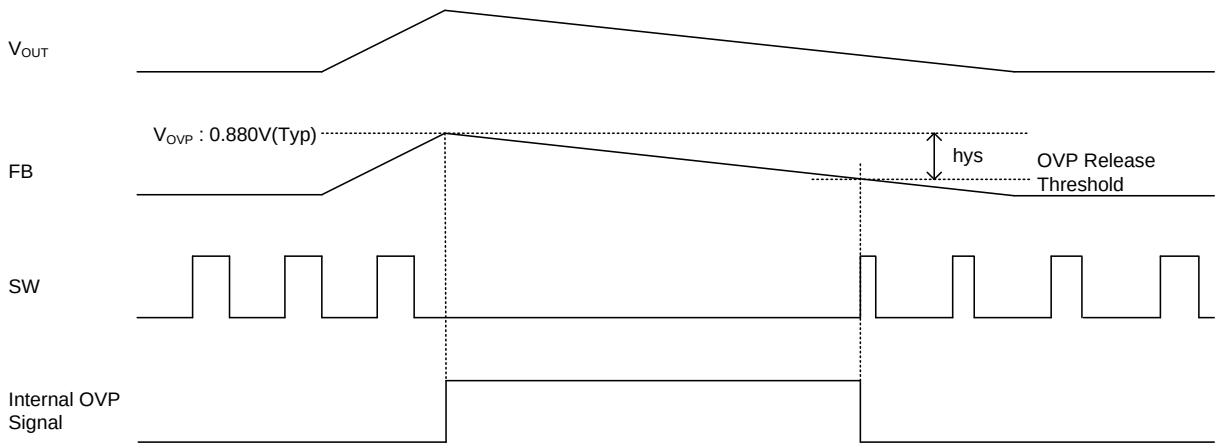

Figure 33. OVP Timing Chart

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Selection of Components Externally Connected

Contact us if not use the recommended constant in the application circuit.

Necessary parameters in designing the power supply are as follows:

Table 1. Application Specification

Parameter	Symbol	Example Value
Input Voltage	V_{IN}	5.0V
Output Voltage	V_{OUT}	1.2V
Switching Frequency	f_{SW}	2.2MHz(Typ)
Inductor Ripple Current	ΔI_L	0.4A
Output Capacitor	C_{OUT}	44µF
Soft Start Time	t_{SS}	4.5ms(Typ)
Maximum Output Current	I_{OUTMAX}	2A

Application Example

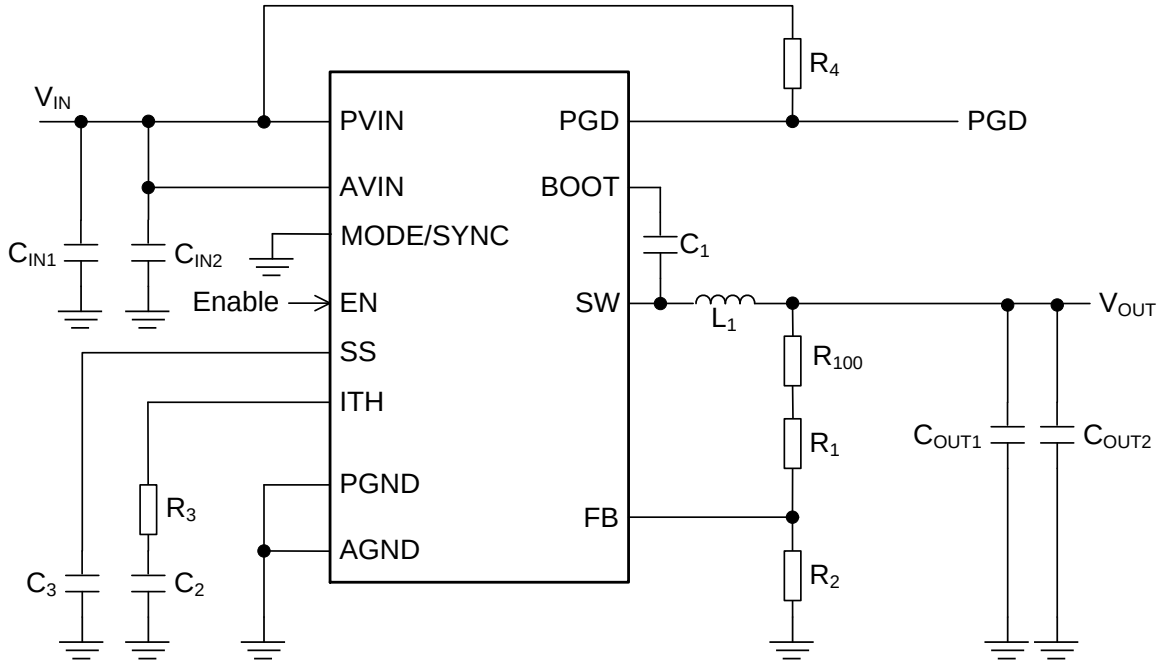

Figure 34. Typical Application

1. **Switching Frequency**
   The switching frequency f_{SW} is fixed at 2.2MHz(Typ) inside the IC.

2. **Selection of Output Voltage Setting**
   The output voltage value can be set by the feedback resistance ratio.

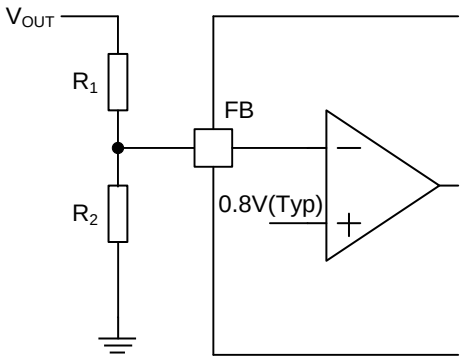

Figure 35. Feedback Resistor Circuit

$$V_{OUT} = \frac{R_1+R_2}{R_2} \times 0.8 \text{ [V]}$$

SW Minimum ON Time that BD9S200MUF-C can output stably in the entire load range is 95ns.
Use this value to calculate the input and output conditions that satisfy the following equation

$$95 \text{ [ns]} \leq \frac{V_{OUT}}{V_{IN} \times f_{OSC}}$$

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Selection of Components Externally Connected – continued

3. Selection of Input Capacitor

The input capacitor requires a large capacitor value for C_{IN1} and a small capacitor value for C_{IN2}. Please use ceramic type capacitor for these capacitors. C_{IN1} is used to suppress the ripple noise, and C_{IN2} is used to suppress the switching noise. These ceramic capacitors are effective by being placed as close as possible to the PVIN pin and the AVIN pin. Capacitor with value 4.7µF or more for C_{IN1}, and 0.06µF or more for C_{IN2} are necessary. In addition, the voltage rating for both capacitors has to be twice the typical input voltage. Set the capacitor value so that it does not fall to its minimum required value against the capacitor value variances, temperature characteristics, DC bias characteristics, aging characteristics, and etc. Please use components which are comparatively same with the components used in "Application Example" on page 22. Moreover, factors like the PCB layout and the position of the capacitor may lead to IC malfunction. Please refer to "Notes on the PCB layout Design" on page 34 and 35.

4. Selection of Output LC Filter

In order to supply a continuous current to the load, the DC/DC converter requires an LC filter for smoothing the output voltage. When an inductor with a higher inductance value is selected, the ripple current flowing through the inductor ΔI_L and the ripple voltage generated in the output voltage are reduced. However, the load transient response characteristic becomes slow. If an inductor with a lower inductance value is selected, its transient response characteristic is faster. However, the ripple current flowing through the inductor becomes larger and the ripple voltage in the output voltage becomes larger, causing a trade-off between the response characteristic and the ripple current and voltage. Here, the inductance value is selected so that the ripple current component is in the range between 200mA and 1000mA.

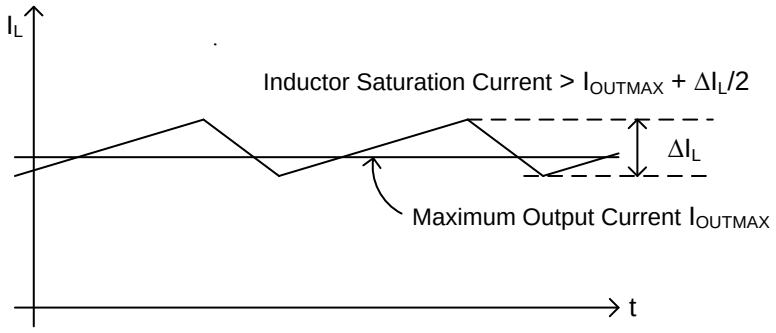

Figure 36. Waveform of Current Through Inductor

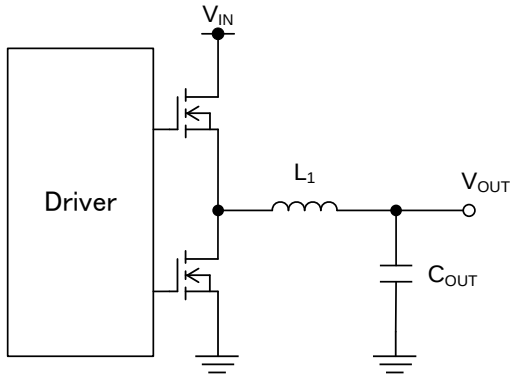

Figure 37. Output LC Filter Circuit

Inductor ripple current ΔI_L can be represented by the following equation.

$$\Delta I_L = V_{OUT} \times (V_{IN} - V_{OUT}) \times \frac{1}{V_{IN} \times f_{SW} \times L_1} = 414 \text{ [mA]}$$

where

V_{IN} is the 5.0V
V_{OUT} is the 1.2V
L_1 is the 1.0µH
f_{SW} is the 2.2MHz (Switching Frequency)

The rated current of the inductor must be larger than the sum of the maximum output current and 1/2 of the inductor ripple current ΔI_L. The output capacitor C_{OUT} affects the output ripple voltage characteristics. The output capacitor C_{OUT} must satisfy the required ripple voltage characteristics.
The output ripple voltage can be represented by the following equation.

$$\Delta V_{RPL} = \Delta I_L \times \left(R_{ESR} + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right) \text{ [V]}$$

Where

R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor

The output ripple voltage ΔV_{RPL} can be represented by the following equation.

$$\Delta V_{RPL} = 0.414 \times \left(10 + \frac{1}{8 \times 44 \times 2.2}\right) = 4.67 \text{ [mV]}$$

where

C_{OUT} is the 44µF
R_{ESR} is the 10mΩ

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Selection of Components Externally Connected – continued

In addition, for the total value of capacitance in the output line C_{OUT}(Max), choose a capacitance value less than the value obtained by the following equation:

$$C_{OUT(Max)} < \frac{(t_{SS(Min)} - 200[\mu s]) \times (I_{OCP(Min)} - I_{SWSTART})}{V_{OUT}} \text{ [F]}$$

Where:

$I_{SWSTART}$	is the maximum output current during startup
$I_{OCP(Min)}$	is the minimum OCP operation SW current 2.8A
$t_{SS(Min)}$	is the minimum Soft Start Time
V_{OUT}	is the output voltage

Startup failure may happen if the limits from the above-mentioned are exceeded. Especially if the capacitance value is extremely large, over current protection may be activated by the inrush current at startup and prevented to turn on the output. Please confirm this on the actual application. Stable transient response and the loop is dependent to C_{OUT}. Please select after confirming the setting of the phase compensation circuit.
Also, in case of large changing input voltage and output current, select the capacitance accordingly by verifying that the actual application setup meets the required specification.

5. Selection of Soft Start Capacitor

Turning the EN pin signal high activates the soft start function. This causes the output voltage to rise gradually while the current at startup is placed under control. This allows the prevention of output voltage overshoot and inrush current. The rise time t_{SS_EXT} depends on the value of the capacitor connected to the SS pin. The capacitance value should be set to 0.22µF or less.

$$t_{SS_EXT} = \frac{(C_3 \times V_{FB})}{I_{SS}} \text{ [s]}$$

where

t_{SS_EXT}	is the Soft Start Time
C_3	is the Capacitor connected to the SS pin
V_{FB}	is the FB pin Voltage 0.8V(Typ)
I_{SS}	is the SS Charge Current 1.8µA(Typ)

With C_3=0.01µF

$$t_{SS_EXT} = \frac{(0.010 \times 0.8)}{1.8} = 4.44 \text{ [ms]}$$

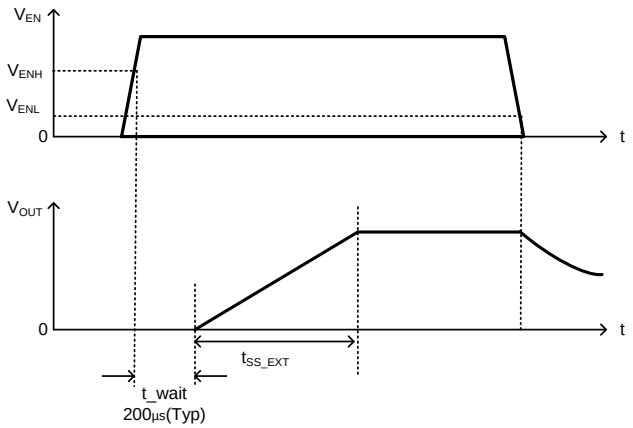

Figure 38. Soft Start Timing chart

Turning the EN pin High without connecting capacitor to the SS pin and keeping the SS pin either OPEN condition or about 10kΩ to 100kΩ pull up condition to power source, the output will rise in 1ms(Typ).

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Selection of Components Externally Connected – continued

6. Selection of Phase Compensation Components

A current mode control buck DC/DC converter is two-pole, one-zero system. Two poles are formed by an error amplifier and load, and the one zero point is added by phase compensation. The phase compensation resistor R_3 determines the crossover frequency f_{CRS} that the total loop gain of the DC/DC converter is 0dB.The crossover frequency should be set 20kHz to 100kHz. A high value f_{CRS} provides a good load transient response characteristic but instability. Conversely, a low value f_{CRS} greatly stabilizes the characteristics but the load transient response characteristic is impaired.

(1) Selection of Phase Compensation Resistor R_3

The Phase Compensation Resistance R_3 can be determined by using the following equation.

$$R_3 = \frac{2\pi \times V_{OUT} \times f_{CRS} \times C_{OUT}}{V_{FB} \times G_{MP} \times G_{MA}} \ [\Omega]$$

where

V_{OUT}	is the Output Voltage
f_{CRS}	is the Crossover Frequency
C_{OUT}	is the Output Capacitance
V_{FB}	is the Feedback Reference Voltage 0.8V(Typ)
G_{MP}	is the Current Sense Gain 14.3A/V(Typ)
G_{MA}	is the Error Amplifier Trans conductance 260μA/V(Typ)

(2) Selection of Phase Compensation Capacitance C_2

For stable operations of DC/DC converter, the zero point (phase lead) to cancel the phase lag formed by loads is determined with C_2.

C_2 can be calculated with the following equation.

$$C_2 = \frac{1}{2\pi \times f_{CRS} \times \frac{1}{0.003} \times V_{OUT}} \ [F]$$

(3) Loop Stability

Actually, characteristics will vary depending on PCB layout, arrangement of wiring, kinds of parts used and use conditions (temperature, etc.). Be sure to check stability and responsiveness with actual apparatus. Phase margin of at least 45° in the worst conditions is recommended. Gain Phase Analyzer or Frequency Response Analyzer FRA is used to check frequency characteristics with actual apparatus. Contact the measurement apparatus manufacturer for measurement method. When these measurement apparatuses are not available, there is a method of assuming Phase margin by load response. Monitor variation of output when the apparatus shifts from no load state to maximum load. And it can be said that responsiveness is low if variation amount is large, and phase margin is small if ringing occurs frequently (twice or more as a guide) after variation.

However, confirmation of quantitative phase margin is not possible.

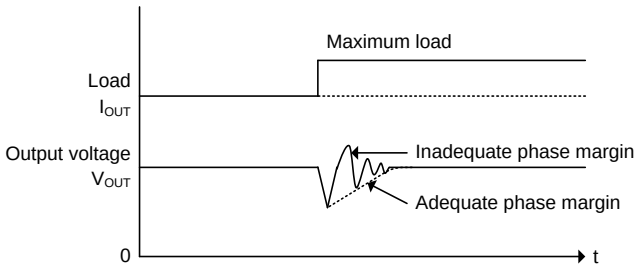

Figure 39. Load Response

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Selection of Components Externally Connected – continued

7. Input Voltage Startup

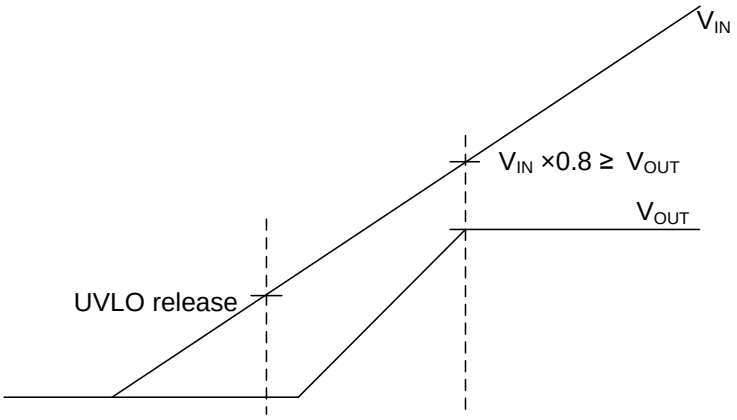

Figure 40. Input Voltage Startup Time

The soft start function starts up the device according to the specified soft start time. After UVLO is released, the voltage range that can be outputted during the soft start operation is 80% or less of the input voltage. Note that the input voltage during the startup with soft start should satisfy the following expression

$$V_{IN} \geq \frac{V_{OUT}}{0.8} \text{ [V]}$$

8. Bootstrap Capacitor

Bootstrap capacitor C_1 shall be 0.1µF. Connect a bootstrap capacitor between the SW pin and the BOOT pin.
For capacitance of bootstrap capacitor, take temperature characteristics, DC bias characteristics and etc. into consideration to set minimum value to no less than 0.047µF.

Recommended Parts Manufacturer List

Shown below is the list of the recommended parts manufacturers for reference.

Table 2.

Device	Type	Manufacturer	URL
C	Ceramic capacitors	Murata	www.murata.com
C	Ceramic capacitors	TDK	product.tdk.com
L	Inductors	Coilcraft	www.coilcraft.com
L	Inductors	Cyntec	www.cyntec.com
L	Inductors	Murata	www.murata.com
L	Inductors	Sumida	www.sumida.com
L	Inductors	TDK	www.product.tdk.com
R	Resisters	ROHM	www.rohm.com

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Application Example 1

Table 3. Specification Example 1

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	3.3V
Output Voltage	V_{OUT}	1.0V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C

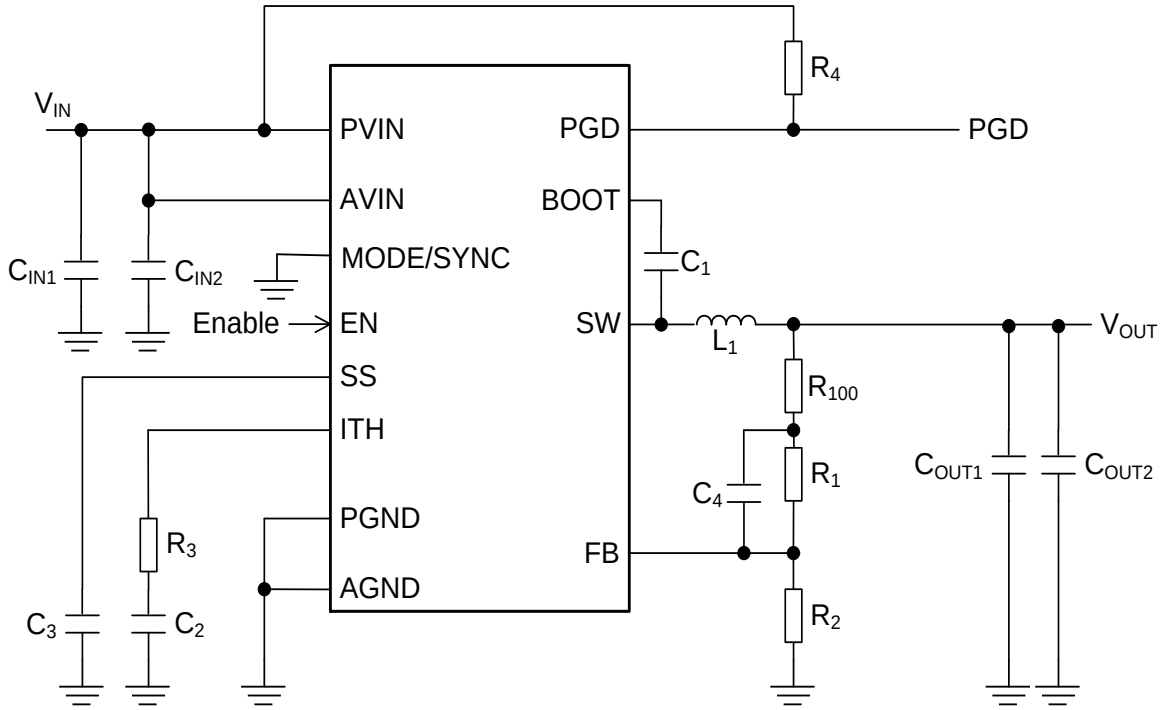

Figure 41. Reference Circuit 1

Table 4. Parts List 1

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		1.0µH	CLF5030NIT-1R0N-D	Inductor	TDK
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	7.5kΩ, 1%, 1/16W	MCR01MZPF7501	Chip Resistor	ROHM
R_2	1005	30kΩ, 1%, 1/16W	MCR01MZPF3002	Chip Resistor	ROHM
R_3	1005	8.2kΩ, 1%, 1/16W	MCR01MZPF8201	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	4700pF, X7R, 50V	GCM155R71H472K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 1)

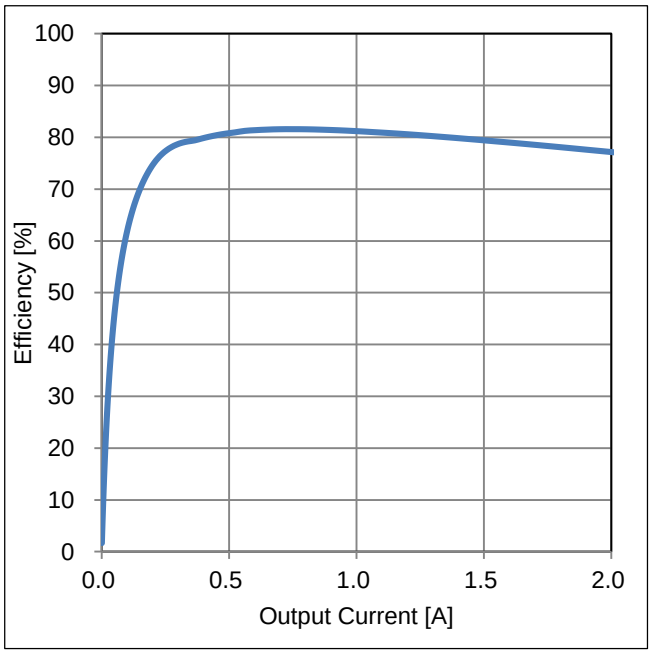

Figure 42. Efficiency vs Output Current

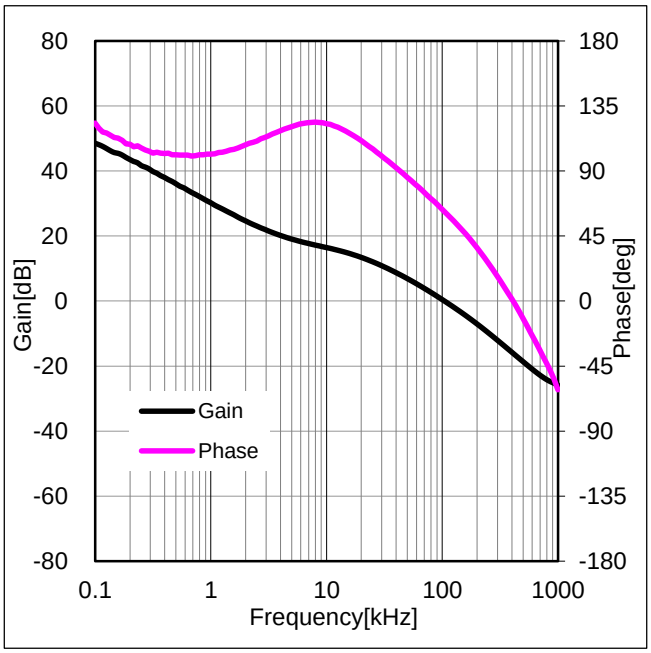

Figure 43. Frequency Characteristics
(I_{OUT}=2A)

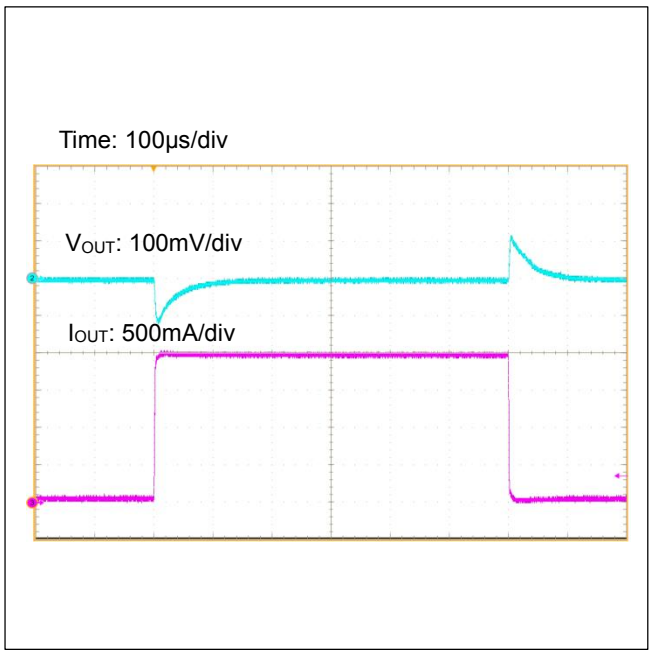

Figure 44. Load Transient Response
(I_{OUT}=0A↔2A)

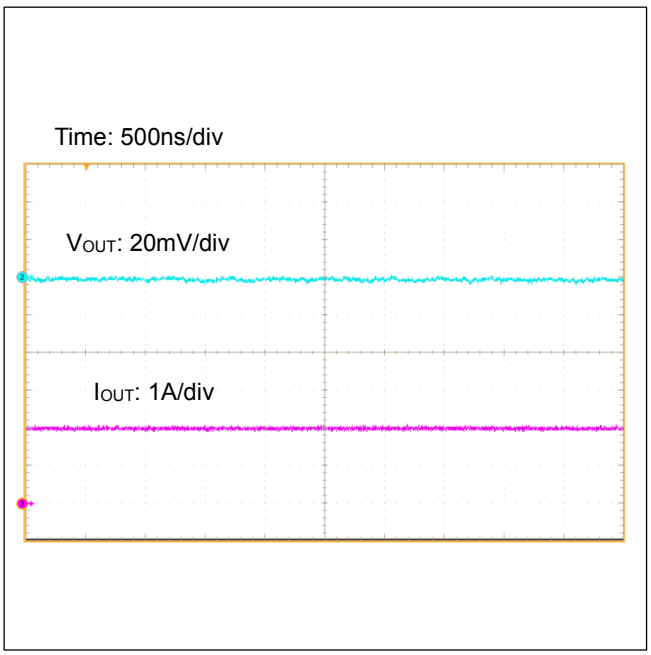

Figure 45. Output Ripple Voltage
(I_{OUT}=2A)

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Application Example 2

Table 5. Specification Example 2

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	3.3V
Output Voltage	V_{OUT}	1.0V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C
Output Capacitor	C_{OUT}	88µF

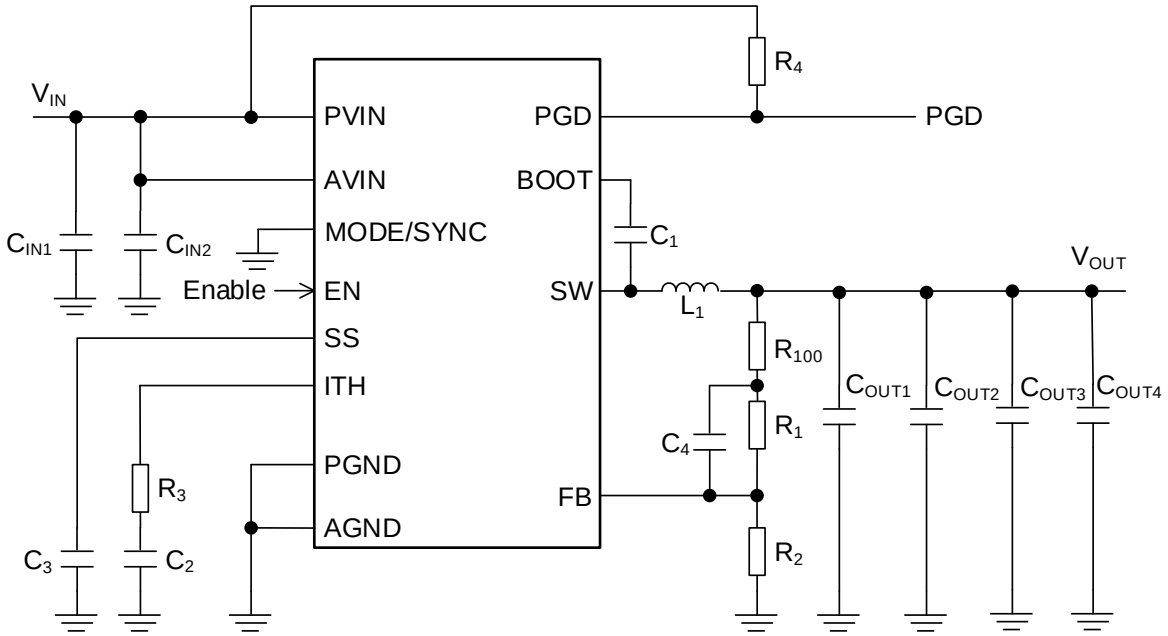

Figure 46. Reference Circuit 2

Table 6. Parts List 2

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		0.47µH	XEL4030-471ME	Inductor	Coilcraft
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT3}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT4}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	7.5kΩ, 1%, 1/16W	MCR01MZPF7501	Chip Resistor	ROHM
R_2	1005	30kΩ, 1%, 1/16W	MCR01MZPF3002	Chip Resistor	ROHM
R_3	1005	30kΩ, 1%, 1/16W	MCR01MZPF3002	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	1000pF, X7R, 50V	GCM155R71H102K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 2)

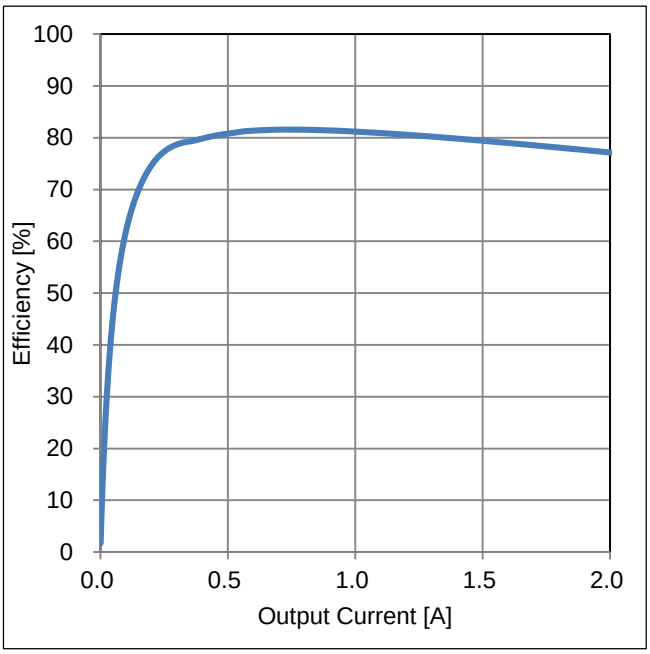

Figure 47. Efficiency vs Output Current

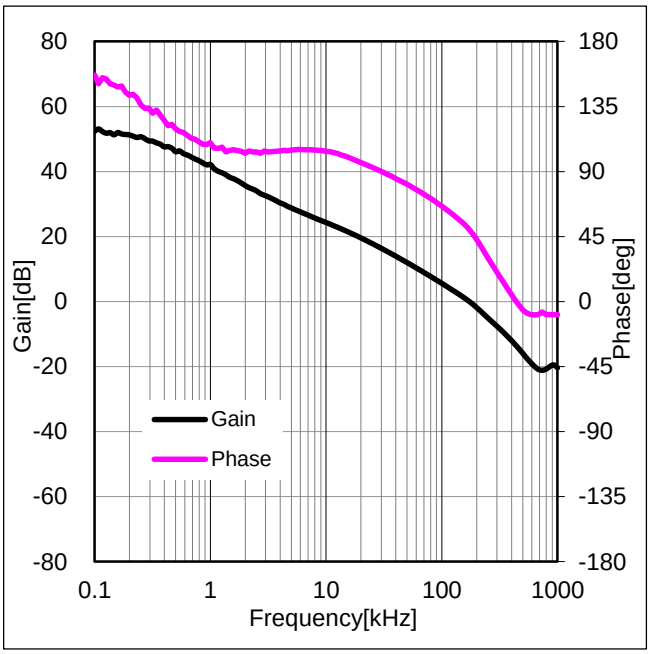

Figure 48. Frequency Characteristic
(I_{OUT}=2A)

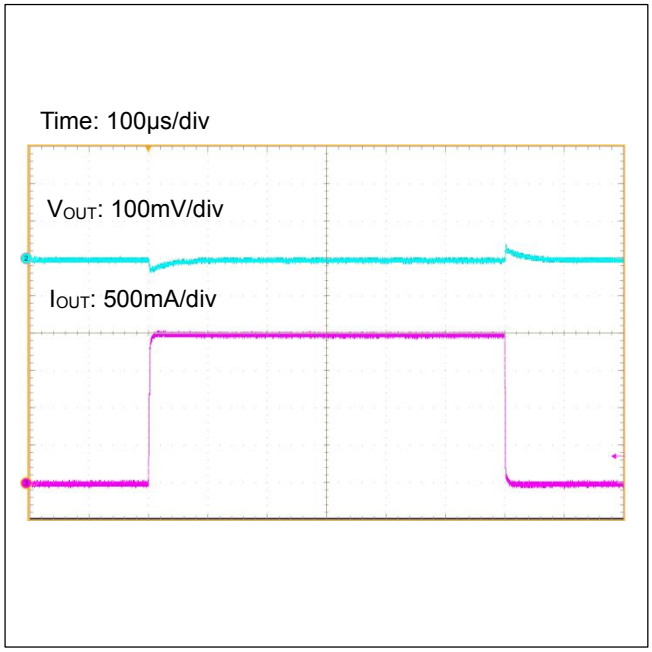

Figure 49. Load Transient Response
(I_{OUT}=0A↔2A)

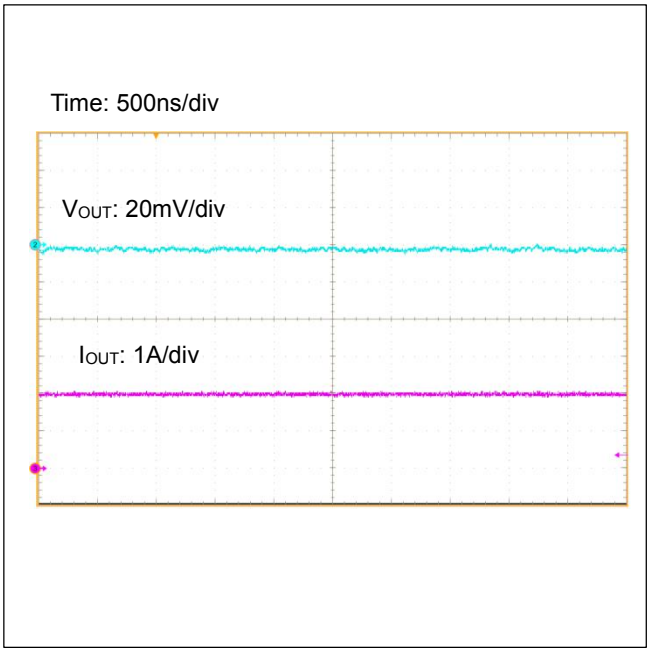

Figure 50. Output Ripple Voltage
(I_{OUT}=2A)

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Application Example 3

Table 7. Specification Example 3

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	5.0V
Output Voltage	V_{OUT}	1.2V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C

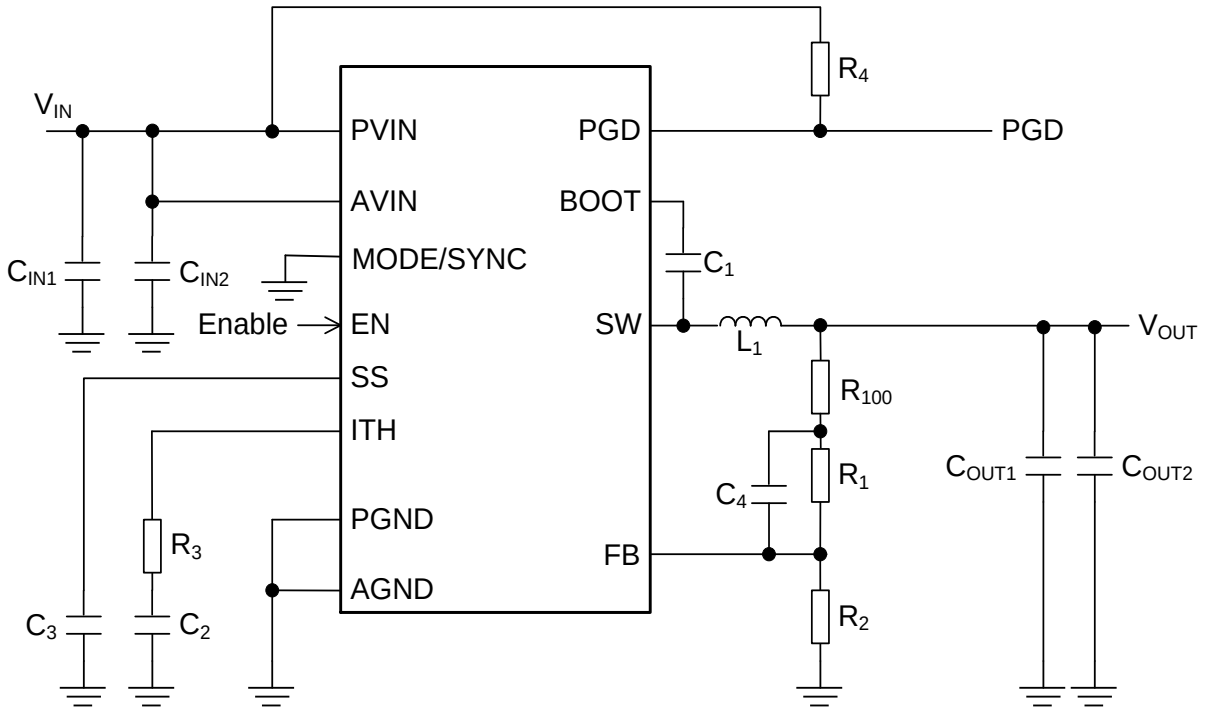

Figure 51. Reference Circuit 3

Table 8. Parts List 3

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		1.0µH	CLF5030NIT-1R0N-D	Inductor	TDK
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	10kΩ, 1%, 1/16W	MCR01MZPF1002	Chip Resistor	ROHM
R_2	1005	20kΩ, 1%, 1/16W	MCR01MZPF2002	Chip Resistor	ROHM
R_3	1005	8.2kΩ, 1%, 1/16W	MCR01MZPF8201	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	4700pF, X7R, 50V	GCM155R71H472K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 3)

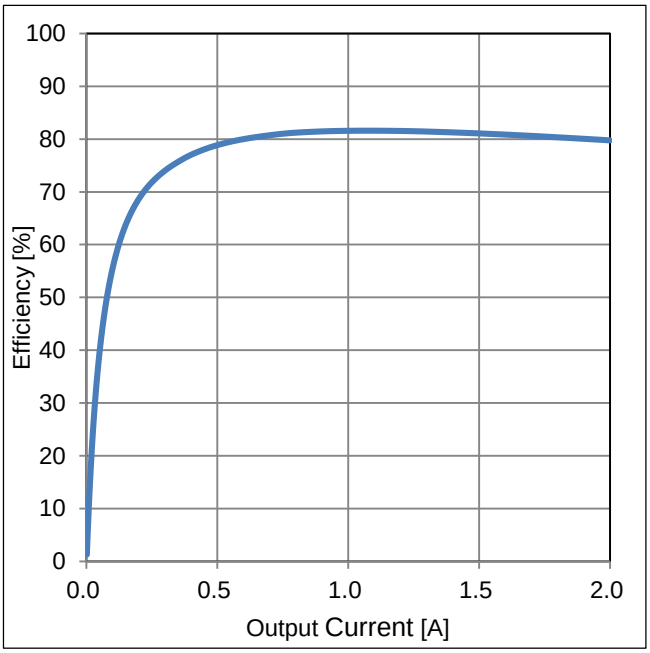

Figure 52. Efficiency vs Output Current

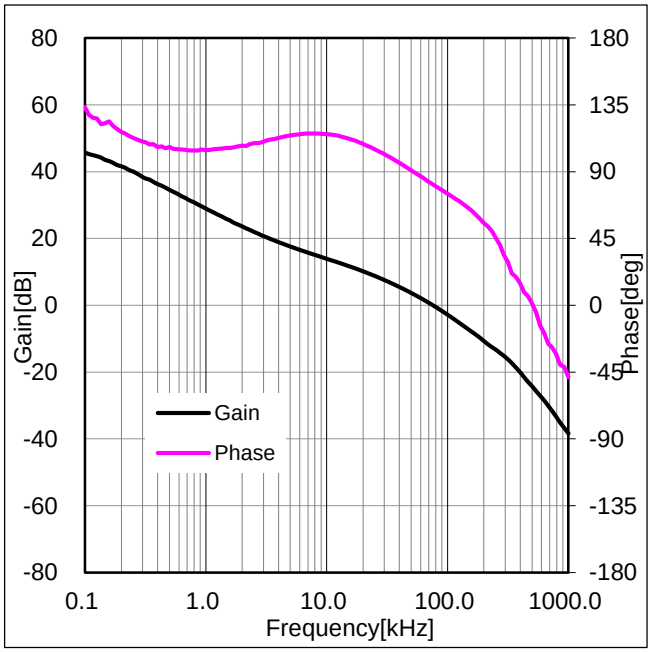

Figure 53. Frequency Characteristics
(I_{OUT}=2A)

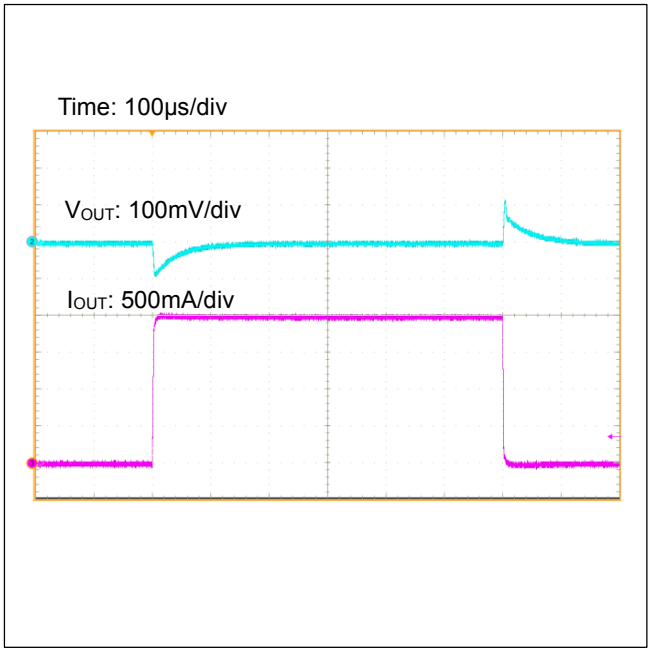

Figure 54. Load Transient Response
(I_{OUT}=0A↔2A)

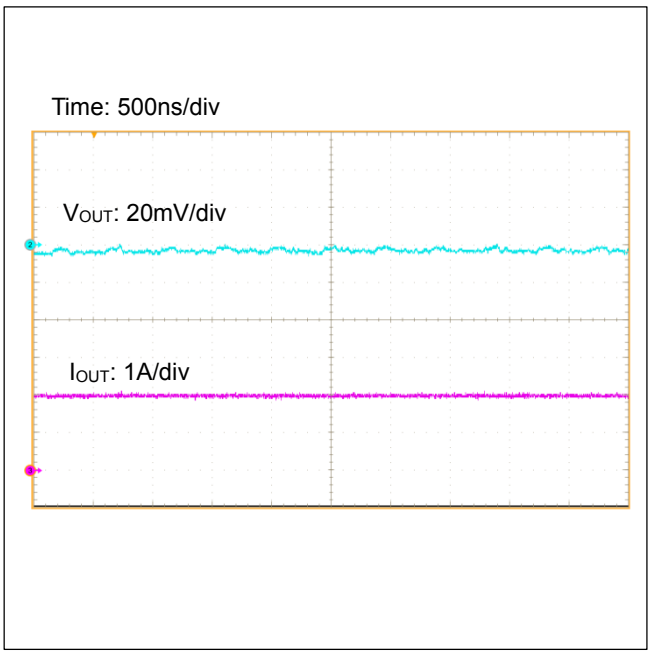

Figure 55. Output Ripple Voltage
(I_{OUT}=2A)

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Application Example 4

Table 9. Specification Example 4

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	5.0V
Output Voltage	V_{OUT}	1.5V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C

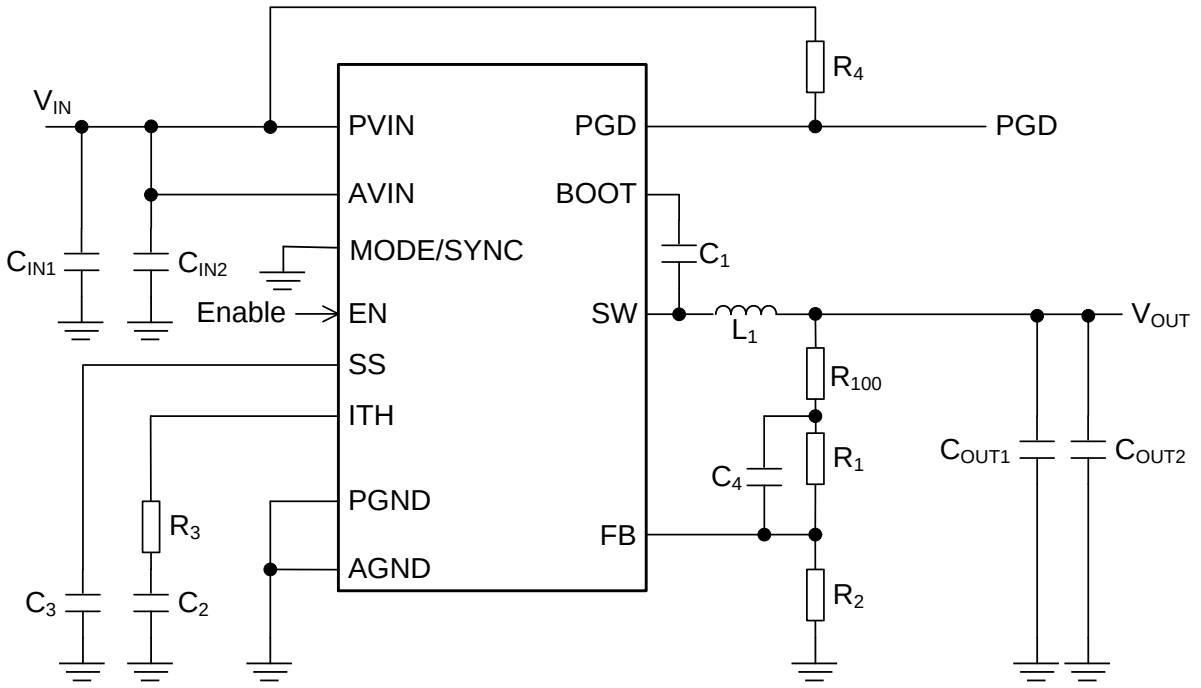

Figure 56. Reference Circuit 4

Table 10. Parts List 4

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		1.0µH	CLF5030NIT-1R0N-D	Inductor	TDK
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	16kΩ, 1%, 1/16W	MCR01MZPF1602	Chip Resistor	ROHM
R_2	1005	18kΩ, 1%, 1/16W	MCR01MZPF1802	Chip Resistor	ROHM
R_3	1005	12kΩ, 1%, 1/16W	MCR01MZPF1202	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	3300pF, X7R, 50V	GCM155R71H332K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 4)

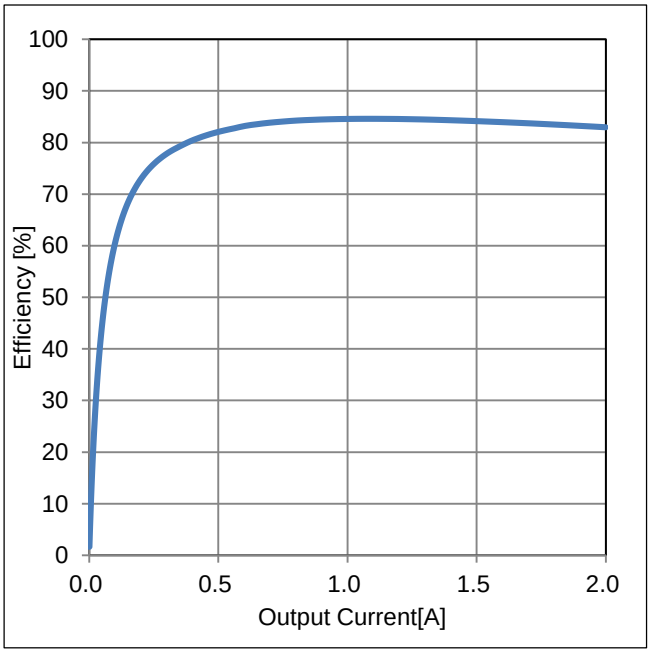

Figure 57. Efficiency vs Output Current

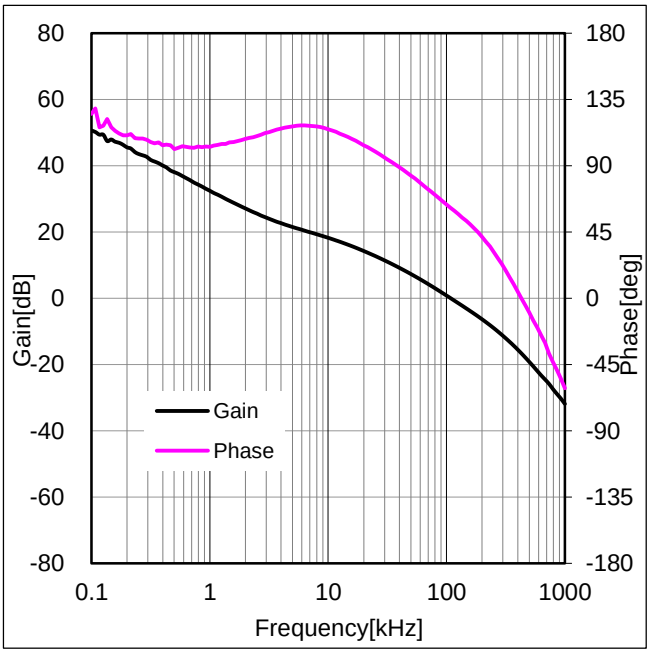

Figure 58. Frequency Characteristics
(I_{OUT} =2A)

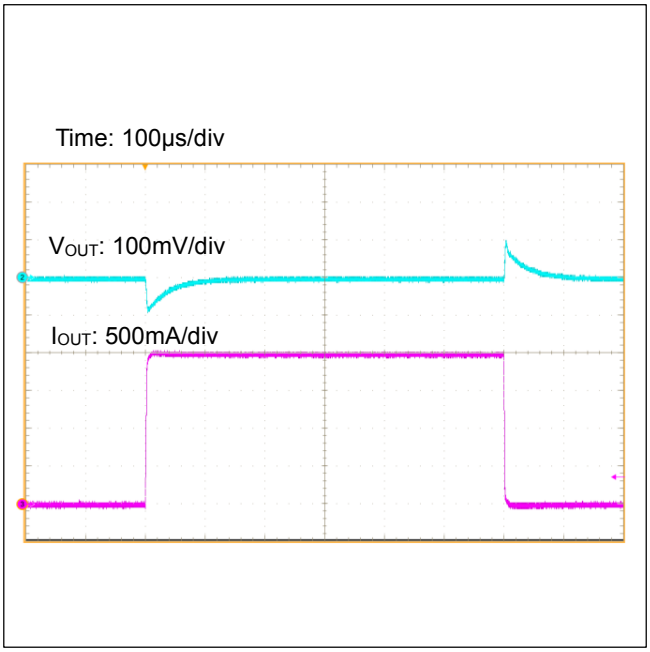

Figure 59. Load Transient Response
(I_{OUT} = 0A↔2A)

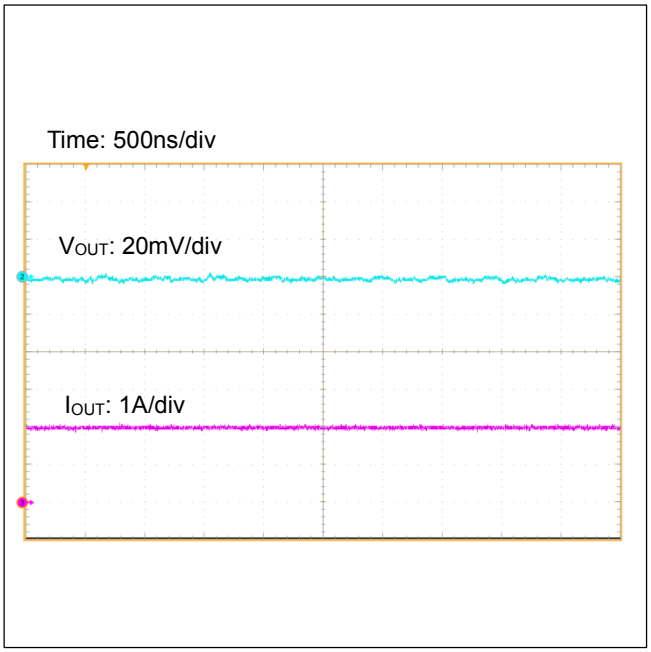

Figure 60. Output Ripple Voltage
(I_{OUT}=2A)

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Application Example 5

Table 11. Specification Example 5

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	5.0V
Output Voltage	V_{OUT}	1.8V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C

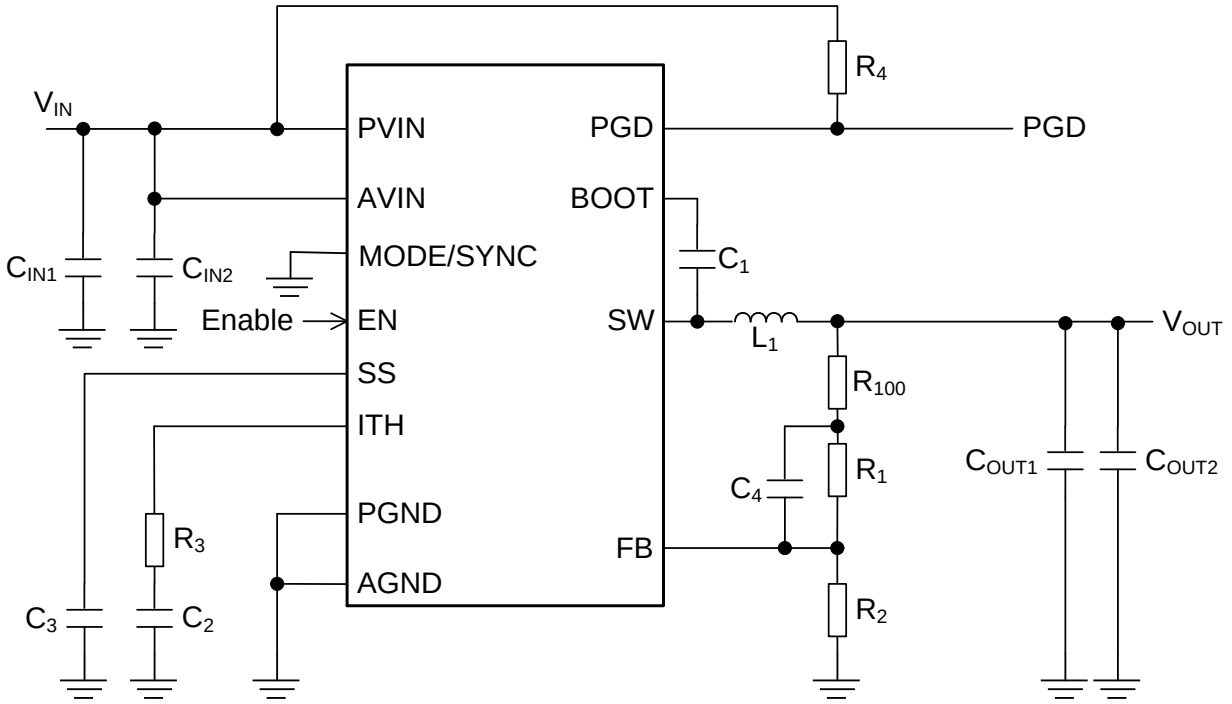

Figure 61. Reference Circuit 5

Table 12. Parts List 5

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		1.0µH	CLF5030NIT-1R0N-D	Inductor	TDK
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	30kΩ, 1%, 1/16W	MCR01MZPF3002	Chip Resistor	ROHM
R_2	1005	24kΩ, 1%, 1/16W	MCR01MZPF2402	Chip Resistor	ROHM
R_3	1005	13kΩ, 1%, 1/16W	MCR01MZPF1302	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	3300pF, X7R, 50V	GCM155R71H332K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 5)

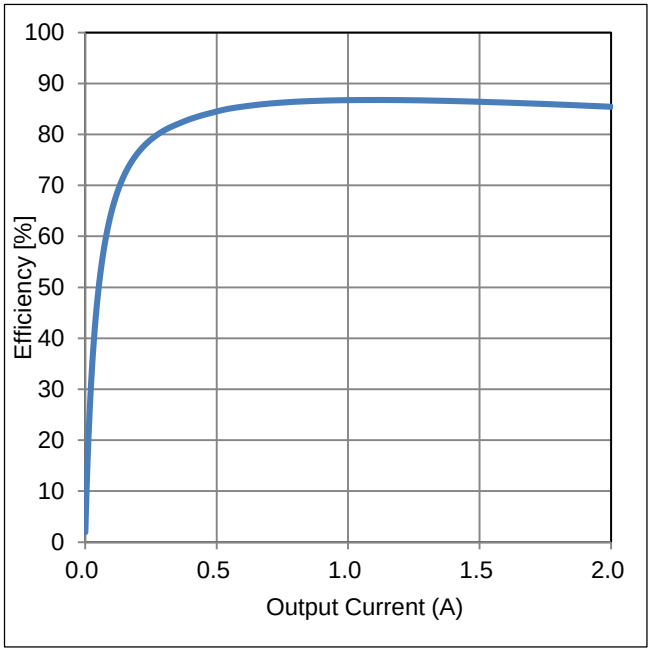

Figure 62. Efficiency vs Output Current

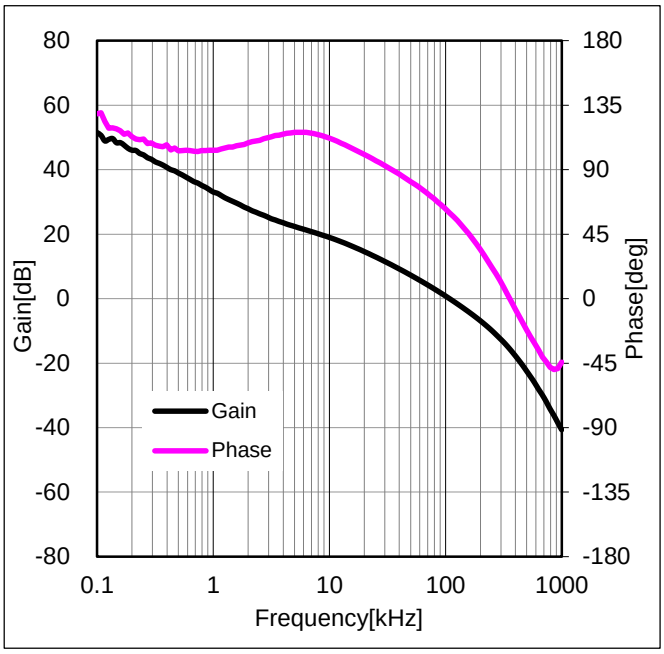

Figure 63. Frequency Characteristics
(I_{OUT}=2A)

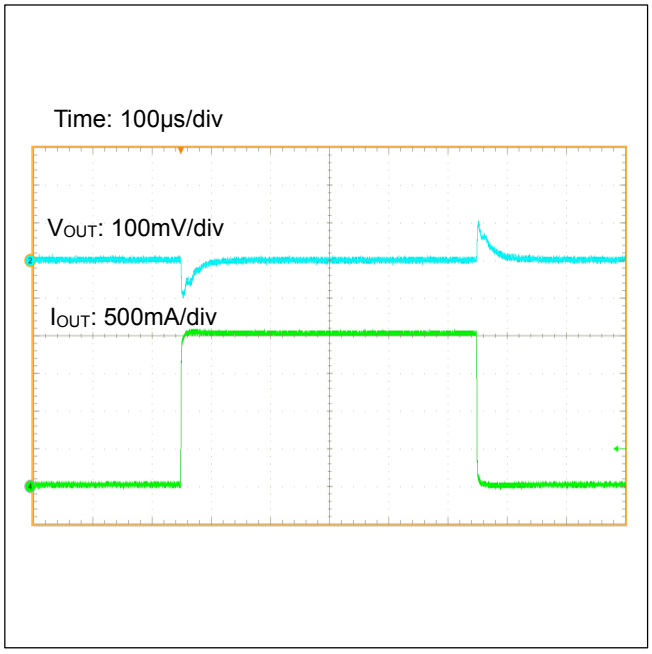

Figure 64. Load Transient Response
(I_{OUT}=0A↔2A)

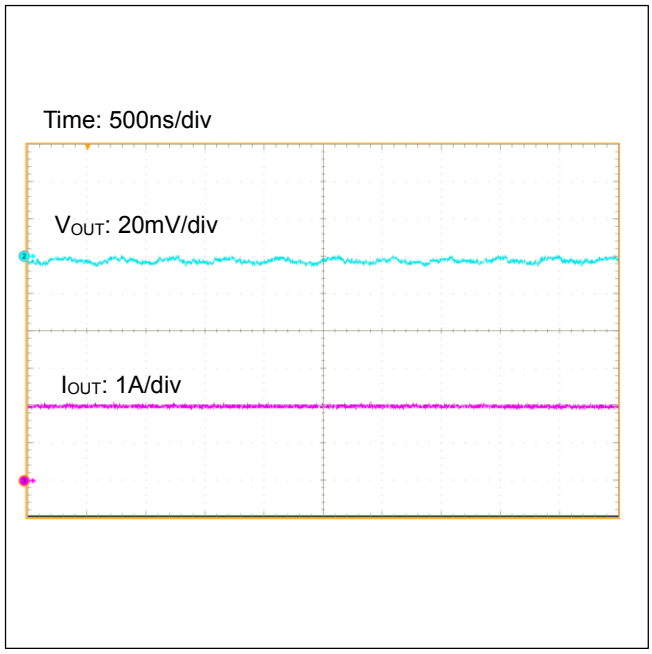

Figure 65. Output Ripple Voltage
(I_{OUT}=2A)

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Application Example 6

Table 13. Specification Example 6

Parameter	Symbol	Example Value
Product Name	IC	BD9S200MUF-C
Supply Voltage	V_{IN}	5.0V
Output Voltage	V_{OUT}	3.3V
Soft Start Time	t_{SS}	1.0ms(Typ)
Maximum Output Current	I_{OUTMAX}	2.0A
Operation Temperature Range	Topr	-40°C to +125°C

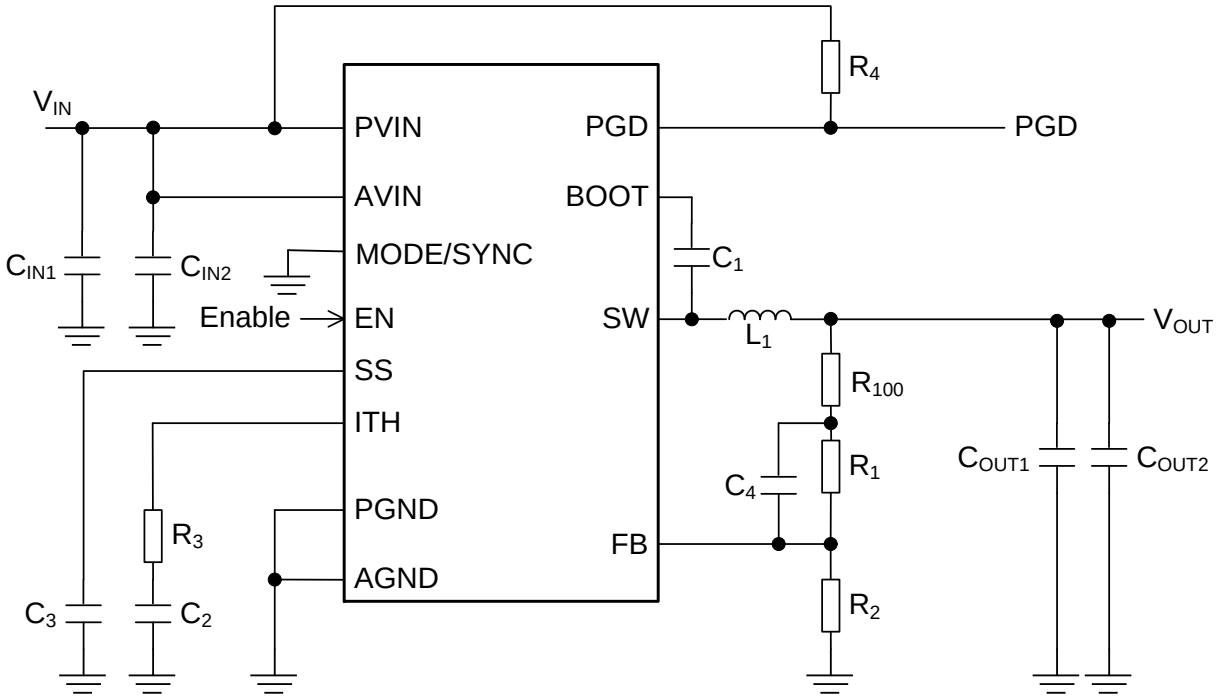

Figure 66. Reference Circuit 6

Table 14. Parts List 6

No	Package	Parameters	Part Name(Series)	Type	Manufacturer
L_1		1.0µH	CLF5030NIT-1R0N-D	Inductor	TDK
C_{OUT1}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{OUT2}	3216	22µF, X7R, 6.3V	GCM31CR70J226K	Ceramic Capacitor	Murata
C_{IN1}	2012	10µF, X7R, 10V	GCM21BR71A106K	Ceramic Capacitor	Murata
C_{IN2}	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
R_{100}	-	SHORT	-	-	-
R_1	1005	75kΩ, 1%, 1/16W	MCR01MZPF7502	Chip Resistor	ROHM
R_2	1005	24kΩ, 1%, 1/16W	MCR01MZPF2402	Chip Resistor	ROHM
R_3	1005	20kΩ, 1%, 1/16W	MCR01MZPF2002	Chip Resistor	ROHM
R_4	1005	100kΩ, 1%, 1/16W	MCR01MZPF1003	Chip Resistor	ROHM
C_1	1005	0.1µF, X7R, 16V	GCM155R71C104K	Ceramic Capacitor	Murata
C_2	1005	2200pF, X7R, 50V	GCM155R71H222K	Ceramic Capacitor	Murata
C_3	-	-	-	-	-
C_4	-	-	-	-	-

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Characteristic Data (Application Examples 6)

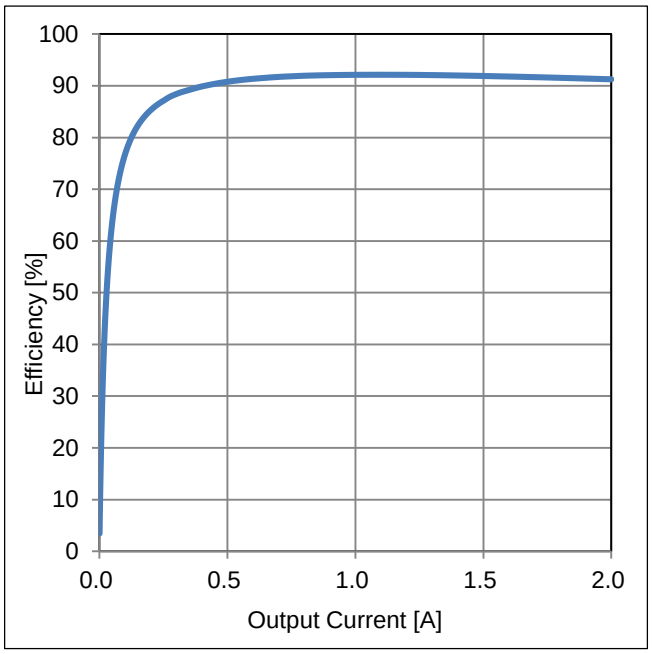

Figure 67. Efficiency vs Output Current

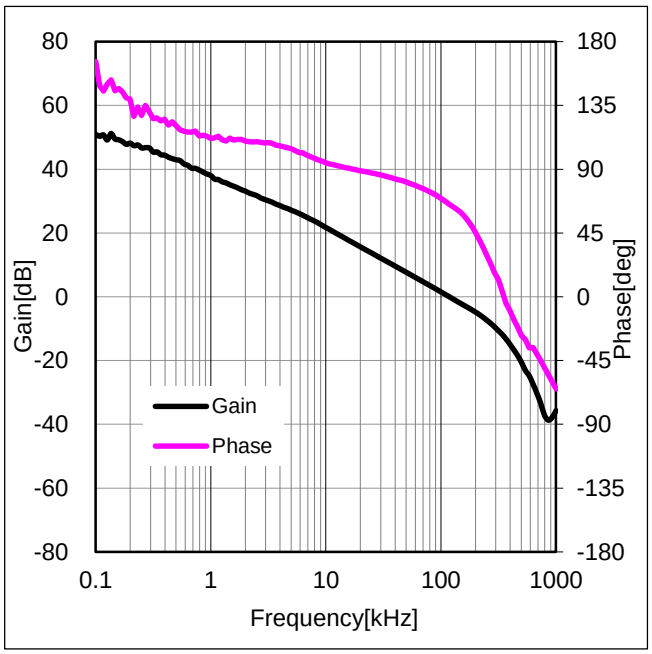

Figure 68. Frequency Characteristics
(I_{OUT}=2A)

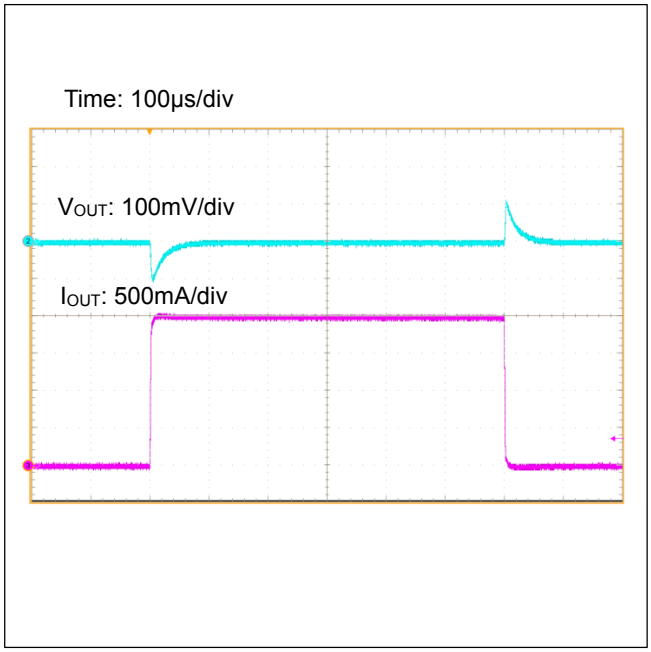

Figure 69. Load Transient Response
(I_{OUT}=0A↔2A)

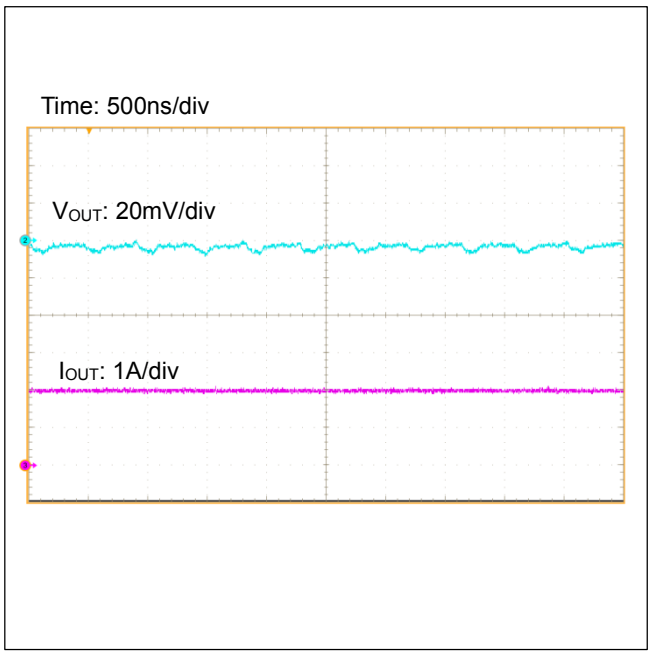

Figure 70. Output Ripple Voltage
(I_{OUT}=2A)

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PCB Layout Design

PCB layout design for DC/DC converter is as important as the circuit design. Appropriate layout can avoid various problems concerning power supply circuit. Figure 71-a to 71-c show the current path in a buck DC/DC converter circuit. The Loop 1 in Figure 71-a is a current path when H-side switch is ON and L-side switch is OFF, the Loop 2 in Figure 71-b is when H-side switch is OFF and L-side switch is ON. The thick line in Figure 71-c shows the difference between Loop1 and Loop2. The current in thick line change sharply each time the switching element H-side and L-side switch change from OFF to ON, and vice versa. These sharp changes induce a waveform with harmonics in this loop. Therefore, the loop area of thick line that is consisted by input capacitor and IC should be as small as possible to minimize noise. For more details, refer to application note of switching regulator series “PCB Layout Techniques of Buck Converter”.

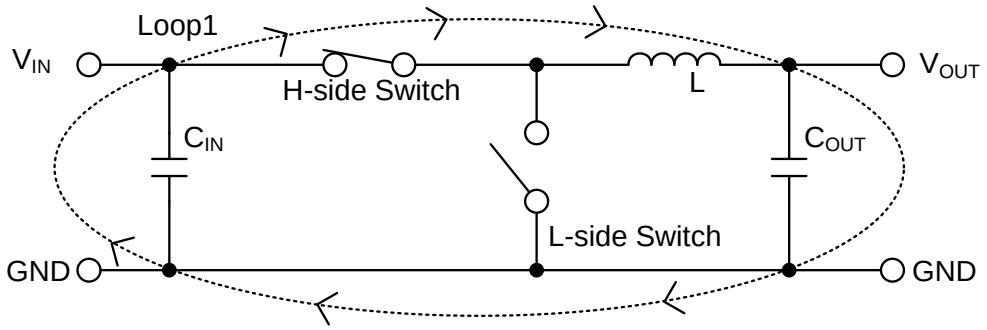

Figure 71-a. Current Path when H-side Switch = ON, L-side Switch = OFF

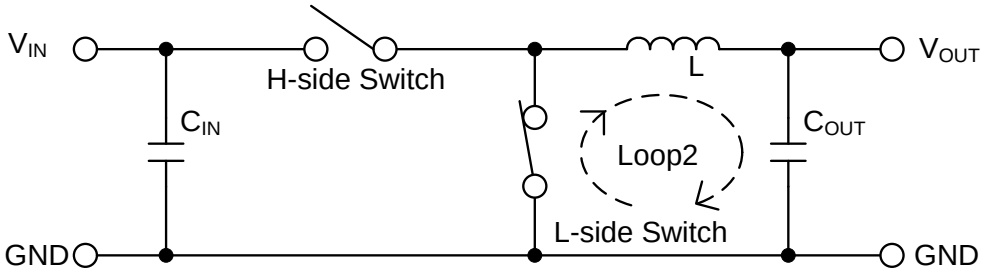

Figure 71-b. Current Path when H-side Switch = OFF, L-side Switch = ON

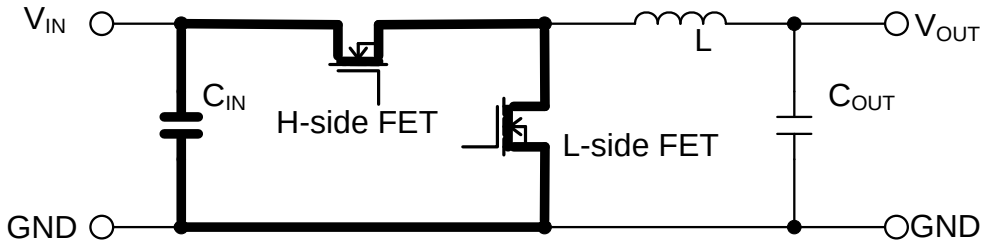

Figure 71-c. Difference of Current and Critical Area in Layout

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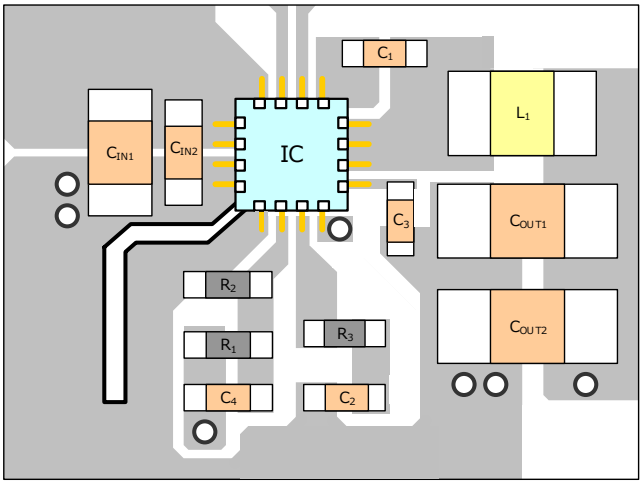
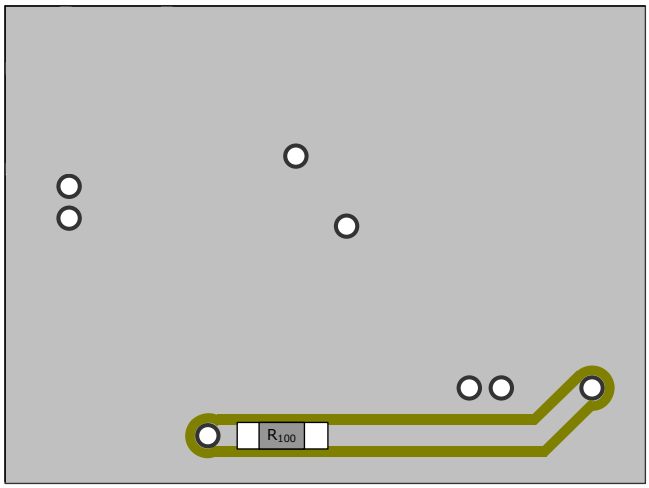
PCB Layout Design – continued

When designing the PCB layout, please pay extra attention to the following points:

- Connect the input capacitor as close as possible to the PVIN pin on the same plane as the IC.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the inductor pattern as thick and as short as possible.
- R_1 and R_2 shall be located as close as possible to the FB pin and the wiring between R_1 and R_2 to the FB pin shall be as short as possible.
- Provide lines connected to FB and ITH far from the SW nodes.
- When using the external synchronization function, there is concern that the ITH node might be affected by noise. Therefore, place the ITH node as far as possible from the external clock input node.
- Influence from the switching noise can be minimized, by isolating Power (Input and Output Capacitor) GND and Reference (FB, ITH) GND.
- R_{100} is provided for the measurement of feedback frequency characteristics (optional). By inserting a resistor into R_{100}, it is possible to measure the frequency characteristics of feedback (phase margin) using FRA etc. R_{100} is short-circuited for normal use.



Example of Evaluation Board Layout (Top View)



Example of Evaluation Board Layout (Bottom View)

Figure 72. Example of Evaluation Board Layout

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Power Dissipation

For thermal design, be sure to operate the IC within the following conditions.
(Since the temperatures described hereunder are all guaranteed temperatures, take margin into account.)

1. The ambient temperature Ta is to be 125 °C or less.
2. The chip junction temperature Tj is to be 150 °C or less.

The chip junction temperature Tj can be considered in the following two patterns:

1. To obtain Tj from the package surface center temperature Tt in actual use

$$Tj = Tt + \psi_{JT} \times W \text{ [°C]}$$

2. To obtain Tj from the ambient temperature Ta

$$Tj = Ta + \theta_{JA} \times W \text{ [°C]}$$

Where:

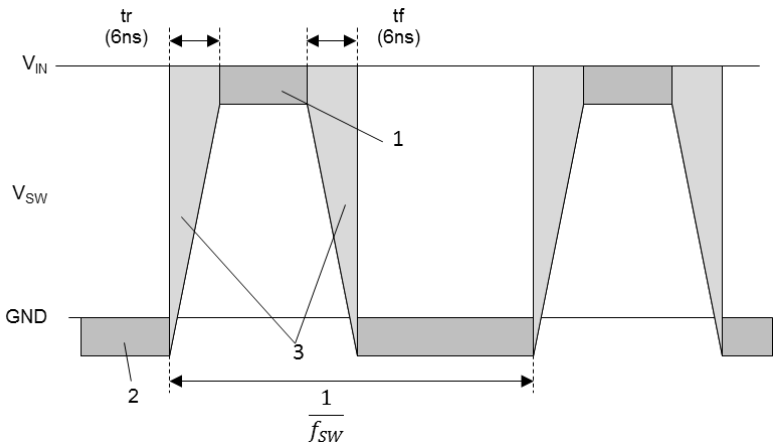
ψ_{JT}	is junction to top characterization parameter (Refer to page 5)
θ_{JA}	is junction to ambient (Refer to page 5)

The heat loss W of the IC can be obtained by the formula shown below:

$$W = R_{ONH} \times {I_{OUT}}^2 \times \frac{V_{OUT}}{V_{IN}} + R_{ONL} \times {I_{OUT}}^2 \left(1 - \frac{V_{OUT}}{V_{IN}}\right) + V_{IN} \times I_{CC} + \frac{1}{2} \times (tr + tf) \times V_{IN} \times I_{OUT} \times f_{SW} \text{ [W]}$$

Where:

R_{ONH}	is the High Side FET ON Resistance (Refer to page 6) [Ω]
R_{ONL}	is the Low Side FET ON Resistance (Refer to page 6) [Ω]
I_{OUT}	is the Output Current [A]
V_{OUT}	is the Output Voltage [V]
V_{IN}	is the Input Voltage [V]
I_{CC}	is the Circuit Current (Refer to page 6) [A]
tr	is the Switching Rise Time [s] (Typ:6ns)
tf	is the Switching Fall Time [s] (Typ:6ns)
f_{SW}	is the Switching Frequency (Refer to page 6) [Hz]



1. $R_{ONH} \times {I_{OUT}}^2$
2. $R_{ONL} \times {I_{OUT}}^2$
3. $\frac{1}{2} \times (tr + tf) \times V_{IN} \times I_O \times f_{SW}$

Figure 73. SW Waveform

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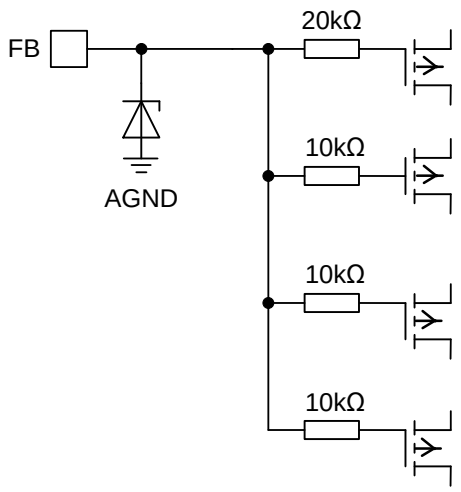
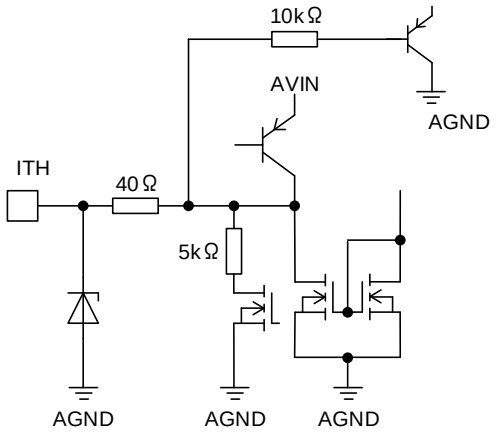
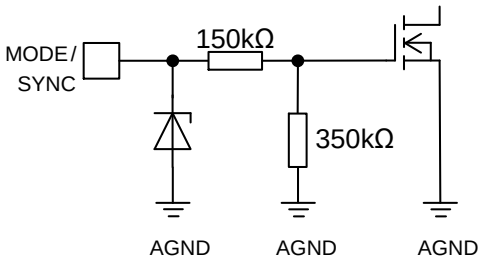
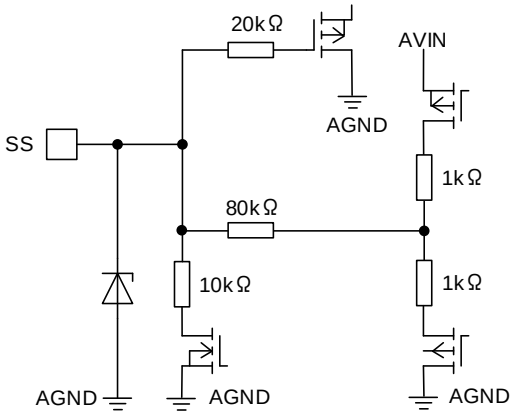
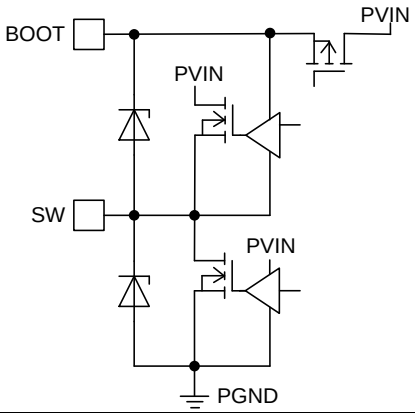
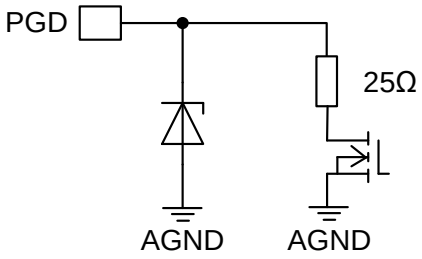
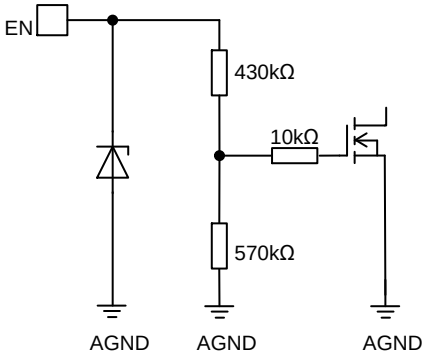
I/O Equivalent Circuits

6. FB	7. ITH
	
8. MODE/SYNC	**9. SS**
	
10.11.12. SW, 13. BOOT	**14. PGD**
	
15. EN	
	

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

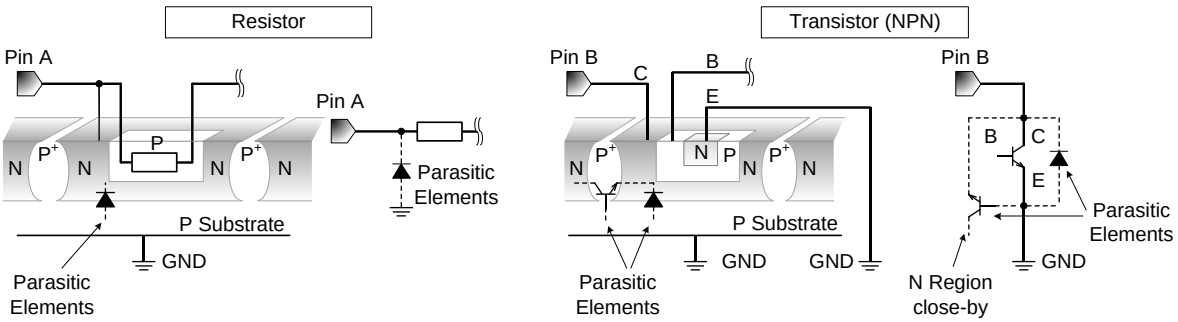

Figure 74. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

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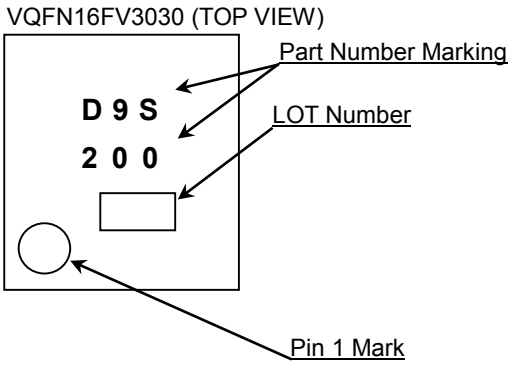
Ordering Information

B D 9 S 2 0 0 M U F	-	C E 2

- Part Number
- Package: VQFN16FV3030
- Product class: C for Automotive applications
- Packaging and forming specification: E2: Embossed tape and reel

Marking Diagrams



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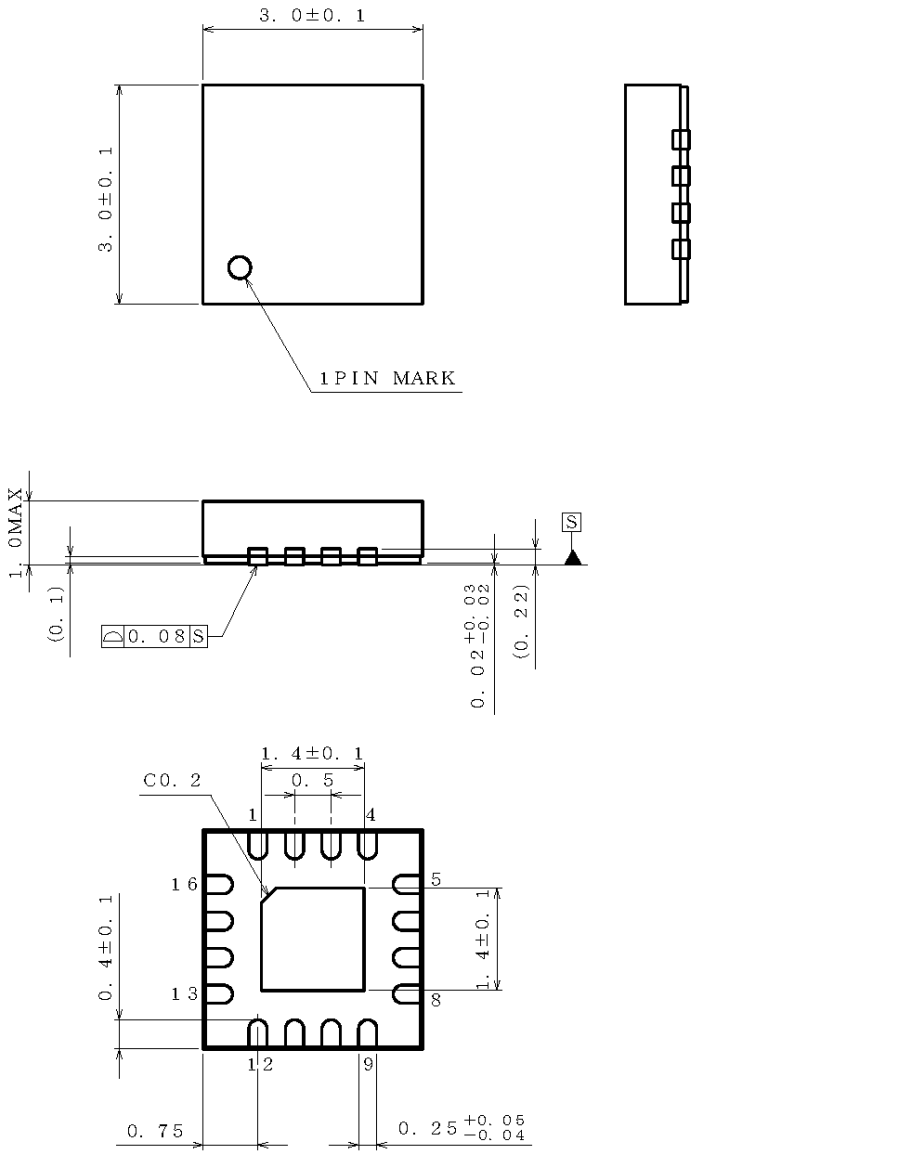
Physical Dimension and Packing Information

Package Name	VQFN16FV3030

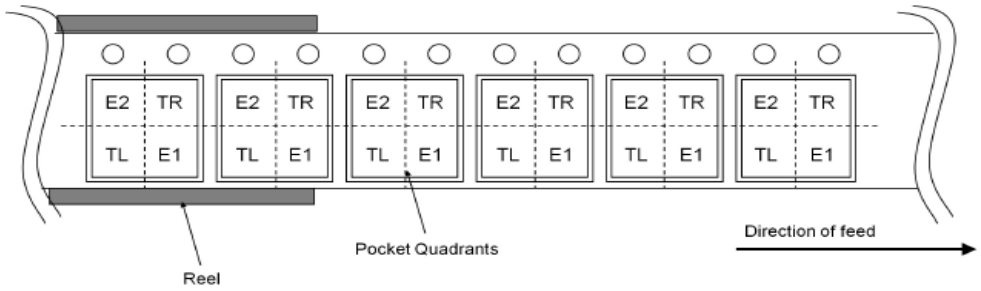


(UNIT : mm)
PKG : VQFN16FV3030
Drawing No. EX396−5001

NOTE : Dimensions in ( ) for reference only.

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
21.Aug.2017	001	New Release
04.Dec.2017	002	Update Operational Notes

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Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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